ADP5310READJ-EVALZ User Guide

UG-824

One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A. • Tel: 781.329.4700 • Fax: 781.461.3113 • www.analog.com

Evaluating the ADP5310 Step-Down Regulator

FEATURES

- 700 nA ultralow quiescent current
- Channel 1: 800 mA maximum load current
- Channel 2: 50 mA maximum load current in hysteresis mode, 300 mA maximum load current in pulse-width modulation (PWM) mode
- Channel 3: low $R_{DS(ON)}$ of 494 mΩ at V_{OUT3} = 2.5 V
- ±1.5% output accuracy over temperature range
- Input voltage range: 2.7 V to 15.0 V
- Integrated high-side and low-side metal-oxide semiconductor field effect transistor (MOSFET)

GENERAL DESCRIPTION

The ADP5310 is a 2-channel synchronous, step-down dc-to-dc regulator with a load switch in a 16-lead TSSOP package. The ADP5310 runs from input voltages of 2.7 V to 15.0 V and requires minimal external components to provide a high efficiency solution with an integrated power switch, synchronous rectifier, and internal compensation.

The ADP5310 evaluation board provides an easy way to evaluate the device. This user guide describes how to quickly set up the board to collect performance data.

Complete information about the ADP5310 is available in the ADP5310 data sheet. It is recommended that the ADP5310 data sheet be consulted in conjunction with this user guide when using the evaluation board.

EVALUATION BOARD CONNECTION DIAGRAM

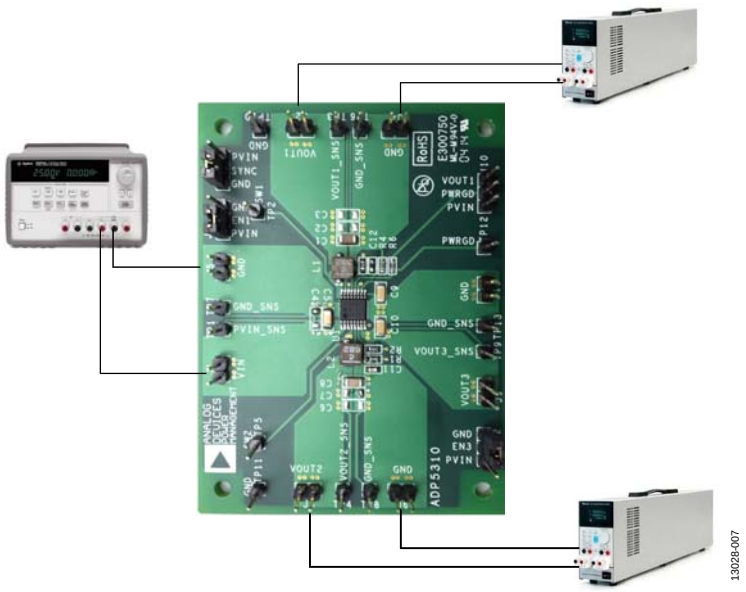

Figure 1.

TABLE OF CONTENTS

REVISION HISTORY

3/2017—Rev. 0 to Rev. A

Changes to Output Voltage Change Section 4
Changes to Table 2 7

4/2015—Revision 0: Initial Version

SETTING UP THE EVALUATION BOARD

POWERING UP THE EVALUATION BOARD

The ADP5310 evaluation board comes fully assembled and tested. Before applying power to the evaluation board, follow the setup procedures in this section.

Jumper Settings

Table 1 describes the jumper settings. Before selecting the jumper settings, make sure that the enable input (ENx) is high.

Table 1. Jumper Settings

Jumper	State or Connection	Function
J8 (EN1)	High	Enable VOUT1
	Low	Disable VOUT1
J10 (PWR GD)	VIN	Pull to VIN
	VOUT1	Pull to VOUT1
J12 (EN3)	High	Enable VOUT3
	Low	Disable VOUT3
J13 (SYNC)	VIN	Channel 2 forced pulse-width modulation (FPWM) mode
	GND	Channel 2 hysteresis mode
	External frequency	Set frequency from 400 kHz to 1.4 MHz

Input Power Source Connection

Before connecting the power source to the ADP5310 evaluation board, make sure the board is turned off. If the input power source includes a current meter, use the meter to monitor the input current as follows:

- Connect the positive (+) terminal of the power source to the VIN terminal (J1) on the evaluation board.
- Connect the negative (−) terminal of the power source to the GND terminal (J5) on the evaluation board.

If the power source does not include a current meter, connect a current meter in series with the input source voltage as follows:

- Connect the positive (+) terminal of the power source to the positive (+) terminal of the current meter.
- Connect the negative (−) terminal of the power source to the GND terminal (J5) on the evaluation board.
- Connect the negative (−) terminal of the current meter to the VIN terminal (J1) on the evaluation board.

Output Load Connection

Before connecting the load to the ADP5310 evaluation board, make sure the board is turned off. If the load includes a current meter or if the current is not measured, connect the load directly to the evaluation board as follows:

- Connect the positive (+) load connection to the VOUT1 terminal (J2), VOUT2 terminal (J3), and VOUT3 terminal (J9) on the evaluation board.
- Connect the negative (−) load connection to the GND terminal (J4, J6, J11) on the evaluation board.

If a current meter is used, connect it in series with the load as follows:

- Connect the positive (+) terminal of the current meter to the VOUT1 terminal (J2), VOUT2 terminal (J3), and VOUT3 terminal (J9) on the evaluation board.
- Connect the negative (−) terminal of the current meter to the positive (+) terminal of the load.
- Connect the negative (−) terminal of the load to the GND terminal (J4, J6, J11) on the evaluation board.

Input and Output Voltmeter Connections

Measure the input and output voltages with voltmeters. Make sure the voltmeters are connected to the appropriate test points on the board. If the voltmeters are not connected to the correct test points, the measured voltages may be incorrect due to the voltage drop across the leads or due to the connections between the board, the power source, and/or the load.

- Connect the positive (+) terminal of the input voltage measuring voltmeter to the TP1 test point on the evaluation board.
- Connect the negative (−) terminal of the input voltage measuring voltmeter to the TP7 test point on the evaluation board.
- Connect the positive (+) terminal of the output voltage measuring voltmeter to the TP3, TP4, and TP9 test points on the evaluation board.
- Connect the negative (−) terminal of the output voltage measuring voltmeter to TP6, TP8, and TP13 test points on the evaluation board.

Power On the Evaluation Board

After the power source and load are connected to the ADP5310 evaluation board, power the board on. If the input power source is higher than 2.7 V, the Channel 1 output voltage rises to 1.8 V, and the Channel 2 output voltage rises to 3.3 V by default.

MEASURING EVALUATION BOARD PERFORMANCE

MEASURING THE SWITCHING WAVEFORM

To observe the switching waveform with an oscilloscope, place the oscilloscope probe tip at the TP2 and TP5 test points with the probe ground connected to ground. Set the oscilloscope to a dc coupling, 5 V/division, 1 µs/division time base. The switching waveform alternates between 0 V and the approximate input voltage.

MEASURING LOAD REGULATION

Test load regulation by increasing the load at the output and measuring the output voltage between the TP3 and TP6 test points, the TP4 and TP8 test points, and the TP9 and TP13 test points.

MEASURING LINE REGULATION

Vary the input voltage and measure the output voltage at a fixed output current. Measure the input voltage between the TP1 and TP7 test points. Measure the output voltage between the TP3 and TP6 test points, the TP4 and TP8 test points, and the TP9 and TP13 test points.

MEASURING EFFICIENCY

Measure the efficiency, η, by comparing the input power with the output power.

$$\eta = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}}$$

To accurately measure the input current of Channel 2, particularly with a lower light load current, set a higher number of power line cycles (NPLC) for the digital multimeters. The longer a signal is integrated, the more accurate the reading result.

MEASURING INDUCTOR CURRENT

Measure the inductor current by removing one end of the inductor from the pad on the evaluation board and using a wire connected between the pad and the inductor. Then use a current probe to measure the inductor current.

MEASURING OUTPUT VOLTAGE RIPPLE

To observe the output voltage ripple, place an oscilloscope probe across the C1, C8, and C10 output capacitors with the probe ground lead placed at the negative (−) capacitor terminal and the probe tip placed at the positive (+) capacitor terminal. Set the oscilloscope to an ac coupling, 10 mV/division, 2 µs/division time base and a 20 MHz bandwidth.

A standard oscilloscope probe has a long wire ground clip. For high frequency measurements, this ground clip picks up high frequency noise and injects it into the measured output ripple.

A simple way to properly measure the output ripple requires removing the oscilloscope probe sheath and wrapping a non-shielded wire around the oscilloscope probe. Keep the ground lengths of the oscilloscope probe as short as possible when measuring the true ripple.

OUTPUT VOLTAGE CHANGE

The output voltage of the ADP5310 evaluation board is preset to 1.8 V and 3.3 V. However, the output voltage can be adjusted using the following equations:

$$V_{OUT1} = 0.8\ \text{V} \times \left(\frac{R3 + R4}{R4}\right)$$

$$V_{OUT2} = 0.8\ \text{V} \times \left(\frac{R1 + R2}{R2}\right)$$

EVALUATION BOARD SCHEMATIC AND ARTWORK

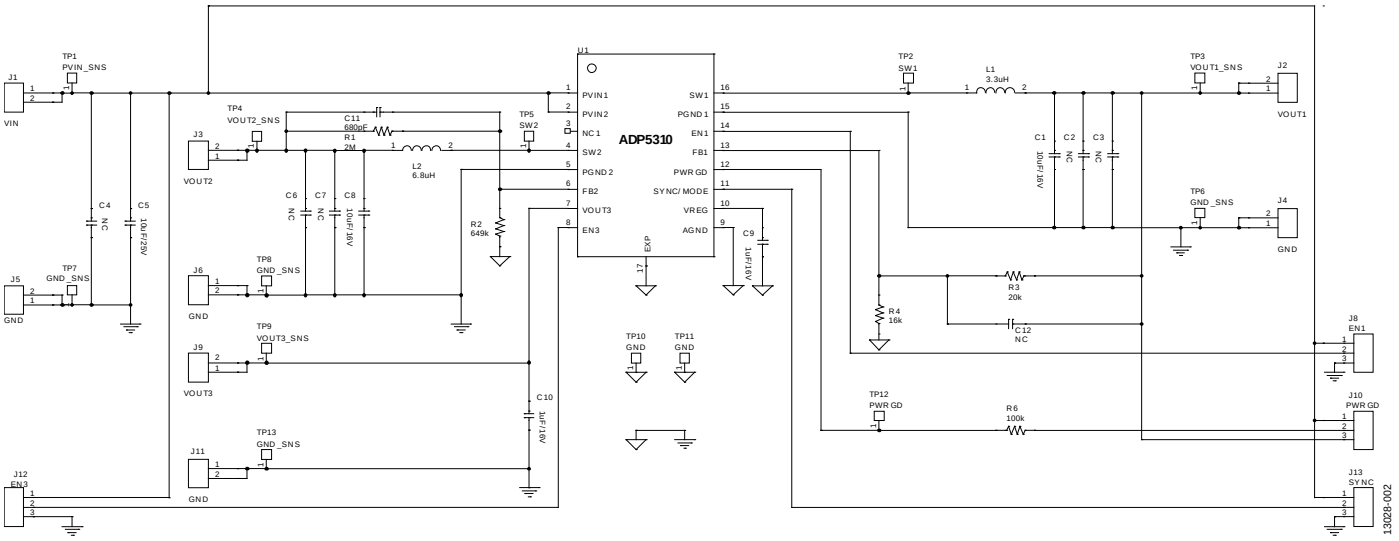

Figure 2. ADP5310 Evaluation Board Schematic

EVALUATION BOARD LAYOUT

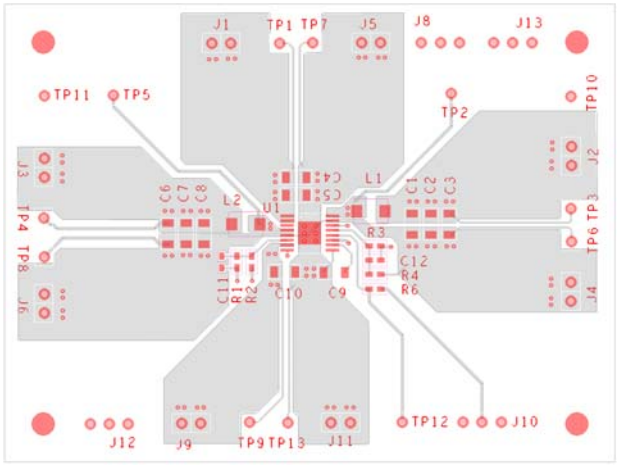

Figure 3. Top Layer

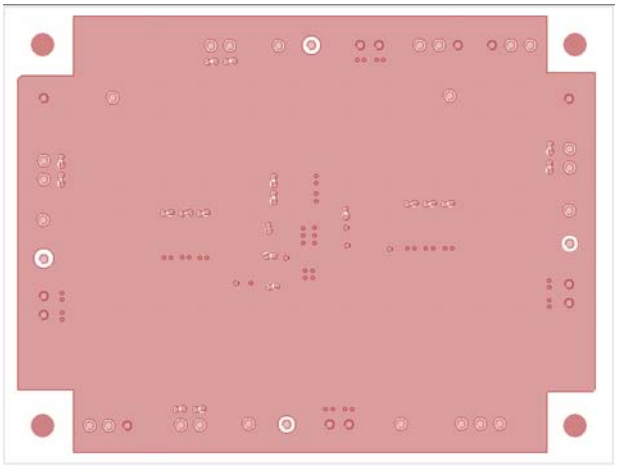

Figure 5. Third Layer

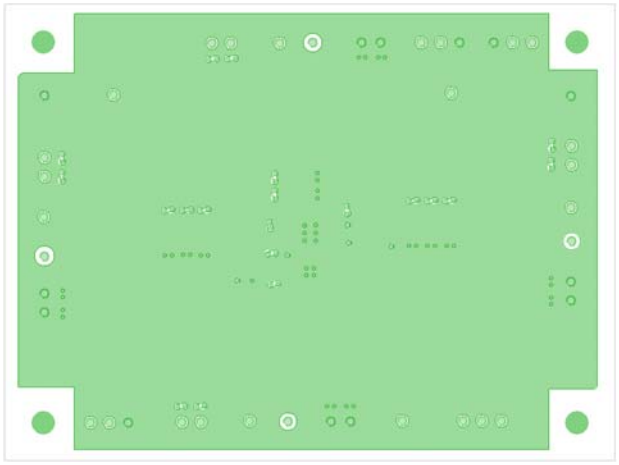

Figure 4. Second Layer

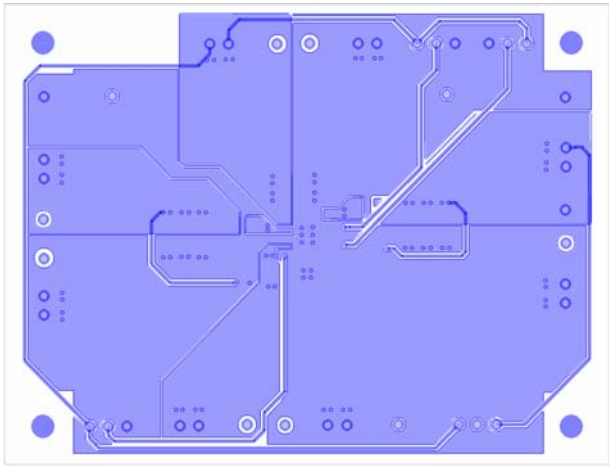

Figure 6. Bottom Layer

ORDERING INFORMATION

BILL OF MATERIALS

Table 2.

Qty	Reference Designator	Description	PCB Footprint	Manufacturer	Part Number
3	C1, C5, C8	10 µF, 25 V	C1206	Murata	GRM31CR61E106MA12L
5	C2, C3, C4, C6, C7	NC	C1206	Not applicable	Not applicable
2	C9, C10	1 µF, 16 V	C1206	Murata	GRM319R71C105KAA3
1	C11	680 pF	R0603	Murata	GRM1885C1H681JA01
1	C12	NC	R0603	Not applicable	Not applicable
1	J1	VIN	SIP2	Harwin	M20-9990245
1	J2	VOUT1	SIP2	Harwin	M20-9990245
1	J3	VOUT2	SIP2	Harwin	M20-9990245
4	J4, J5, J6, J11	GND	SIP2	Harwin	M20-9990245
1	J8	EN1	SIP3	Harwin	M20-9990246
1	J9	VOUT3	SIP2	Harwin	M20-9990245
1	J10	PWRGD	SIP3	Harwin	M20-9990246
1	J12	EN3	SIP3	Harwin	M20-9990246
1	J13	SYNC	SIP3	Harwin	M20-9990246
1	L1	3.3 µH	Inductor, 4.5 mm × 3.3 mm	Coilcraft	XFL4020-332ME
1	L2	6.8 µH	Inductor, 4.5 mm × 3.3 mm	Coilcraft	XAL4030-682ME
1	R1	2 MΩ	R0603	Vishay Dale	CRCW06032M00FKEA
1	R2	649 kΩ	R0603	Vishay Dale	CRCW0603649KFKEA
1	R3	20 kΩ	R0603	Vishay Dale	CRCW060320K0FKEA
1	R4	16 kΩ	R0603	Vishay Dale	CRCW060316K0FKEA
1	R6	100 kΩ	R0603	Vishay Dale	CRCW0603100KFKEA
1	TP1	PVIN_SNS	SIP1	Harwin	M20-9990245
1	TP2	SW1	SIP1	Harwin	M20-9990245
1	TP3	VOUT1_SNS	SIP1	Harwin	M20-9990245
1	TP4	VOUT2_SNS	SIP1	Harwin	M20-9990245
1	TP5	SW2	SIP1	Harwin	M20-9990245
4	TP6, TP7, TP8, TP13	GND_SNS	SIP1	Harwin	M20-9990245
1	TP9	VOUT3_SNS	SIP1	Harwin	M20-9990245
2	TP10, TP11	GND	SIP1	Harwin	M20-9990245
1	TP12	PWRGD	SIP1	Harwin	M20-9990245
1	U1	ADP5310	16-lead TSSOP_EP	Analog Devices, Inc.	ADP5310AREZN-R7

NOTES

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

UG13028-0-3/17(A)