● Structure Silicon Monolithic Integrated Circuit

● Product Name 5x6 dot matrix LED driver for portable device

● Type **BU26507GUL**

● Features

5-channel PMOS SWs and 6-channel current drivers with 1/5 TDMA timing driven sequentially
Automatic Slope function
Automatic Scroll function (8 directions)

● Absolute Maximum Ratings (Ta=25 °C)

Parameter	Symbol	Limits	Unit
Maximum voltage	VMAX	7	V
Power Dissipation (note1)	Pd	790	mW
Operating Temperature Range	Topr	-40 ～ +85	℃
Storage Temperature Range	Tstg	-55 ～ +125	℃

note1) Power dissipation deleting is 7.9mW/ °C , when it's used in over 25 °C.
(ROHM's standard board has been mounted.)
The power dissipation of the IC has to be less than the one of the package

● Operating conditions (VBAT≥VIO, Ta=-40~85 °C)

Parameter	Symbol	Limits	Unit
VBAT input voltage	VBAT	2.7 ～ 5.5	V
VINSW input voltage	VINSW	2.7 ～ 5.5	V
VIO pin voltage	VIO	1.65 ～ 3.3	V

This product isn't designed to protect itself against radioactive rays.

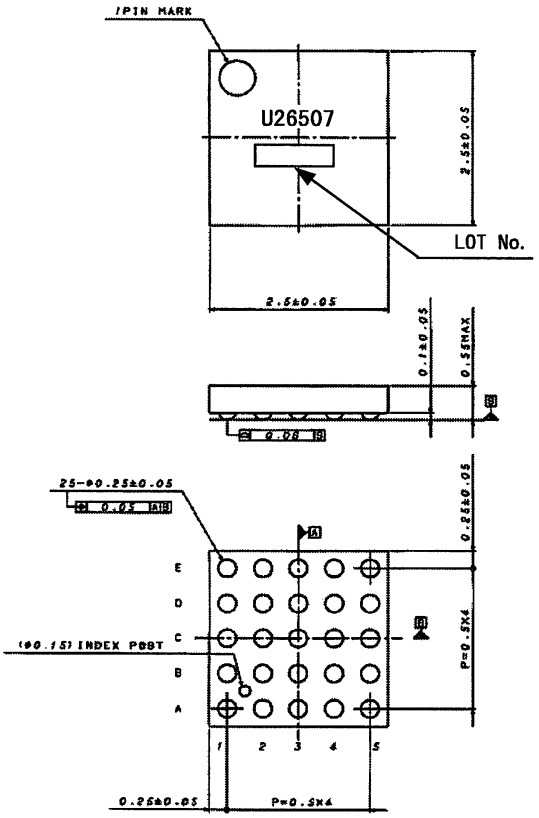
Status of this document
The Japanese version of this document is the formal specification.
A customer may use this translation version only for a reference to help reading the formal version.
If there are any differences in translation version of this document, formal version takes priority.

Application example
· ROHM cannot provide adequate confirmation of patents.
· The product described in this specification is designed to be used with ordinary electronic equipment or devices (such as audio-visual equipment, office-automation equipment, communications devices, electrical appliances, and electronic toys).
Should you intend to use this product with equipment or devices which require an extremely high level of reliability and the malfunction of which would directly endanger human life (such as medical instruments, transportation equipment, aerospace machinery, nuclear-reactor controllers, fuel controllers and other safety devices), please be sure to consult with our sales representative in advance.
· ROHM assumes no responsibility for the use of any circuits described herein, conveys no license under any patent or other right, and makes no representations that the circuits are free from patent infringement.

● Electrical Characteristics (Unless otherwise specified, Ta=25°C, VBAT=3.6V, VINSW=3.6V, VIO=1.8V)

Parameter	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
[Circuit Current]						
VBAT Circuit current 1	IBAT1	-	0	3.0	μA	RESETB=0V, VIO=0V
VBAT Circuit current 2	IBAT2	-	0.5	5.0	μA	RESETB=0V, VIO=1.8V
VBAT Circuit current 3	IBAT3	-	0.8	1.4	mA	When LED1-6 are active with default settings.
[UVLO]						
UVLO Threshold	VUVLO	-	2.1	2.5	V	VBAT falling
UVLO Hysteresis	VHYUVLO	50	-	-	mV	
[LED Driver] (LED1-6)						
Maximum output current	ILEDMax1	-	20.00	-	mA	LED1-6 ,ISET=100kΩ
	ILEDMax2	-	42.50	-	mA	LED1-6 ,ISET=47kΩ
Output current	ILED	-7.0%	10.67	+7.0%	mA	I=10.67mA setting, VLED=1V,ISET=100 kΩ
LED current Matching	ILEDMT	-	-	5	%	ILEDMT= (ILEDMax-ILEDMin)/(ILEDMax+ILEDMin) I=10.67mA setting, VLED=1V
Driver pin voltage range	VLED	0.2	-	VBAT - 1.4	V	ISET=100 kΩ
LED OFF Leak current	ILKLED	-	-	1.0	μA	
[PMOS switch]						
Leak current at OFF	ILEAKP	-	-	1.0	μA	
Resistor at ON	RonP	-	1.0	-	Ω	Isw=60mA, VINSW=4.5V
[OSC]						
OSC frequency	fosc	0.96	1.2	1.44	MHz	
[CE, SYNC, IFMODE]						
L level input voltage	VIL1	-0.3	-	0.25 x VIO	V	
H level input voltage	VIH1	0.75 x VIO	-	VIO +0.3	V	
L level input current	IIL1	-	0	1	μA	
H level input current	IIH1	-	0	1	μA	
[SDA, SCL]						
L level input voltage	VIL2	-0.3	-	0.25 x VIO	V	
H level input voltage	VIH2	0.75 x VIO	-	VIO +0.3	V	
Input hysteresis	Vhys	0.05 x VIO	-	-	V	
L level output voltage (for SDA pin)	VOL2	0	-	0.3	V	IOL=3mA
Input current	Iin1	-3	-	3	μA	Input voltage = from (0.1 x VIO) to (0.9 x VIO)
[RESETB]						
L level input voltage	VIL3	-0.3	-	0.25 x VIO	V	
H level input voltage	VIH3	0.75 x VIO	-	VIO +0.3	V	
Input current	Iin2	-	0	1	μA	Input voltage = from (0.1 x VIO) to (0.9 x VIO)
[CLKIO(OUTPUT)]						
L level output voltage	VOL1	-	-	0.4	V	IOL=2mA
H level output voltage	VOH1	0.75 x VIO	-	-	V	IOH=-2mA
[CLKIO(INPUT)]						
L level input voltage	VIL4	-0.3	-	0.25 x VIO	V	
H level input voltage	VIH4	0.75 x VIO	-	VIO +0.3	V	
Input current	Iin3	-	3.6	10	μA	input voltage=1.8V

● Package outline drawing

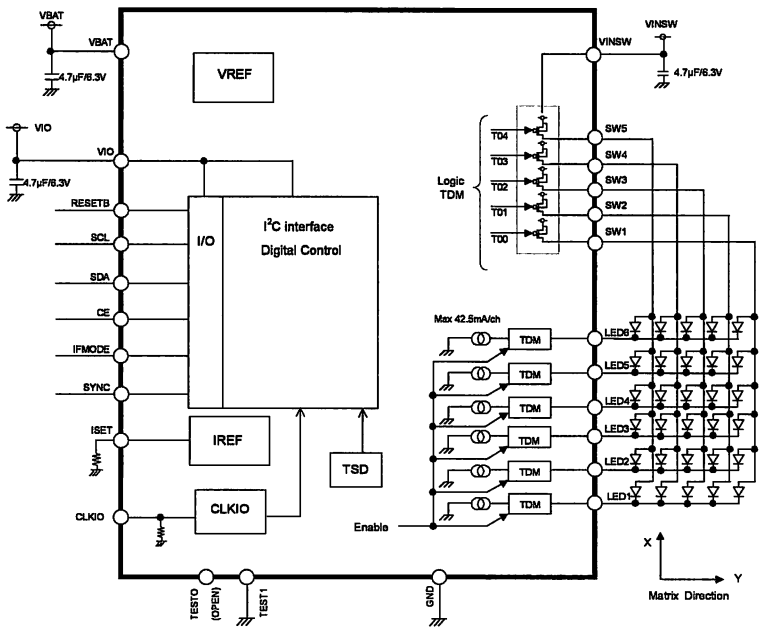


VCSP50L2 (Unit:mm)

● Terminals

No	Ball No.	Pin Name
1	D5	VINSW
2	A1	VBAT
3	C1	VIO
4	D2	RESETB
5	E2	SCL
6	E3	SDA
7	D1	CE
8	C2	IFMODE
9	D3	SYNC
10	B2	ISET
11	B1	CLKIO
12	C3	TESTO
13	E1	TEST1
14	A4	GND
15	A2	LED1
16	B3	LED2
17	A3	LED3
18	B4	LED4
19	B5	LED5
20	A5	LED6
21	C5	SW1
22	C4	SW2
23	D4	SW3
24	E5	SW4
25	E4	SW5

●Block diagram



● Cautions on use

(1) Absolute Maximum Ratings
An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Power supply and ground line
Design PCB pattern to provide low impedance for the wiring between the power supply and the ground lines. Pay attention to the interference by common impedance of layout pattern when there are plural power supplies and ground lines. Especially, when there are ground pattern for small signal and ground pattern for large current included the external circuits, please separate each ground pattern. Furthermore, for all power supply pins to ICs, mount a capacitor between the power supply and the ground pin. At the same time, in order to use a capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(3) Ground voltage
Make setting of the potential of the ground pin so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no pins are at a potential lower than the ground voltage including an actual electric transient.

(4) Short circuit between pins and erroneous mounting
In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between pins or between the pin and the power supply or the ground pin, the ICs can break down.

(5) Operation in strong electromagnetic field
Be noted that using ICs in the strong electromagnetic field can malfunction them.

(6) Input pins
In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input pin. Therefore, pay thorough attention not to handle the input pins, such as to apply to the input pins a voltage lower than the ground respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input pins a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(7) External capacitor
In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

(8) Thermal shutdown circuit (TSD)
This LSI builds in a thermal shutdown circuit (TSD). When junction temperatures become detection temperature or higher, the thermal shutdown circuit operates and turns a switch OFF. The thermal shutdown circuit, which is aimed at isolating the LSI from thermal runaway as much as possible, is not aimed at the protection or guarantee of the LSI. Therefore, do not continuously use the LSI with this circuit operating or use the LSI assuming its operation.

(9) Thermal design
Perform thermal design in which there are adequate margins by taking into account the permissible dissipation (Pd) in actual states of use. And please care about the Maximum ratings and ASO of the Output's Transistor.

(10) About the pin for the test, the un-use pin
Prevent a problem from being in the pin for the test and the un-use pin under the state of actual use. Please refer to a function manual and an application notebook. And, as for the pin that doesn't specially have an explanation, ask our company person in charge.

(11) About the rush current
For ICs with more than one power supply, it is possible that rush current may flow instantaneously due to the internal powering sequence and delays. Therefore, give special consideration to power coupling capacitance, width of power wiring, width of ground wiring, and routing of wiring.

(12) About the function description or application note or more
The function description and the application notebook are the design materials to design a set. So, the contents of the materials aren't always guaranteed. Please design application by having fully examination and evaluation include the external elements.

- Jisso Information -

Package : VCSP50L2

(A table of contents)

1. Structure and materials

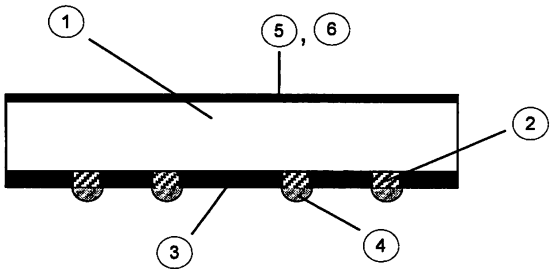


Fig. 1 Structure

No.	Item	Materials
1	Die	Silicon
2	Cu Post	Cu
3	Mold Compound	Epoxy Resin
4	Ext. terminal	Sn-3Ag-0.5Cu Solder
5	Mold Compound	Polyamide-imide Resin
6	Marking	Laser Marking

Dehydrated weight : 6.3mg

2. Tape and Reel information

2. 1. Packing specification

Tape	Embossed carrier tape
Quantity	3,000pcs/Reel
Direction of feed	E2 (See Fig. 2)

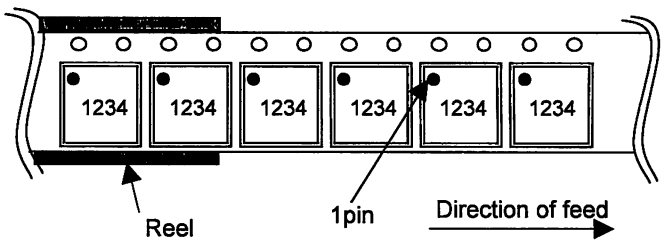


Fig. 2 Typical Tape and Reel configuration

2. 2. Tape and Reel specification

2. 2. 1. Tape and reel dimensions (See the table on page 2/4)

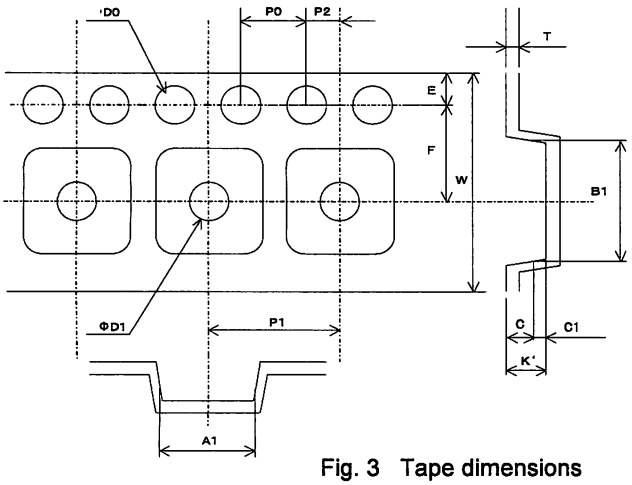


Fig. 3 Tape dimensions

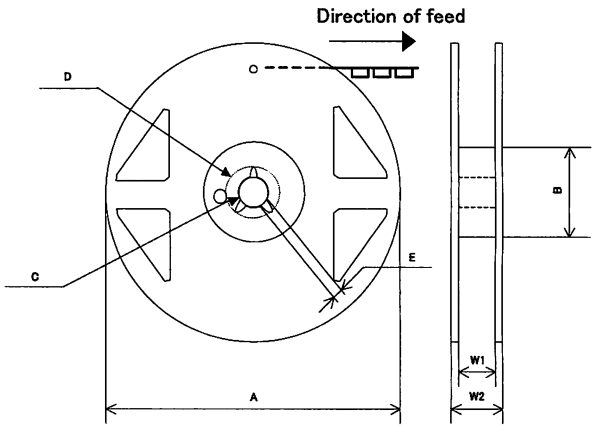


Fig. 4 Reel dimensions

(Tape dimensions)

A1	B1	C	C1	D0	D1	E	F	K'	P0	P1	P2	T	W
2.80 ±0.1	2.80 ±0.1	(0.75)	(0.10)	φ1.5 +0.1 -0	φ0.5 ±0.1	1.75 ±0.1	3.5 ±0.1	0.85 ±0.1	4.0 ±0.1	4.0 ±0.1	2.0 ±0.1	0.3 ±0.05	8.0 ±0.3

(Reel dimensions)

A	B	C	D	E	W1	W2
φ180 +0 -1.5	60 MIN	φ13.0 ±0.2	φ20.2 MIN	1.5 MIN	9.0 +1.0 -0	11.4 ±1.0

(Unit : mm)

2. 3. Leader and Trailer

2. 3. 1. Leader

No component pockets are 100 pockets(400mm) or more.

2. 3. 2. Trailer

No component pockets are 40 pockets(160mm) or more.

Tape is free from reel.

2. 4. Label for Reel and Box

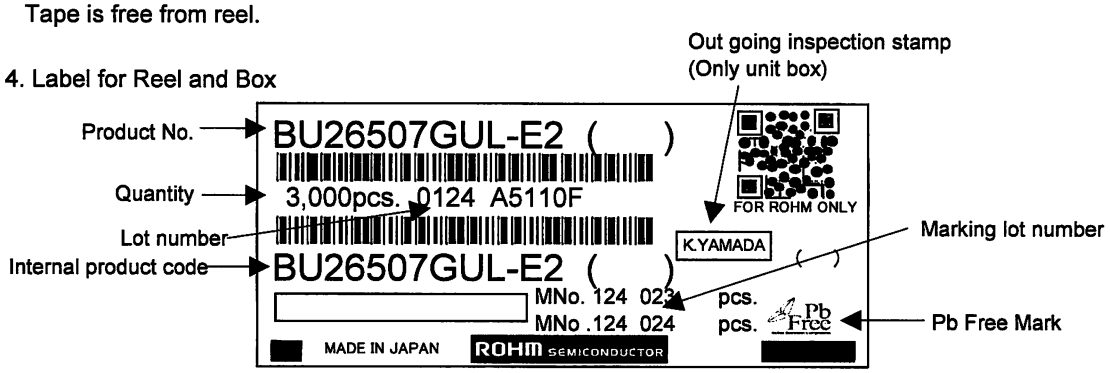


Fig. 5 Label example

2. 5. Packing style

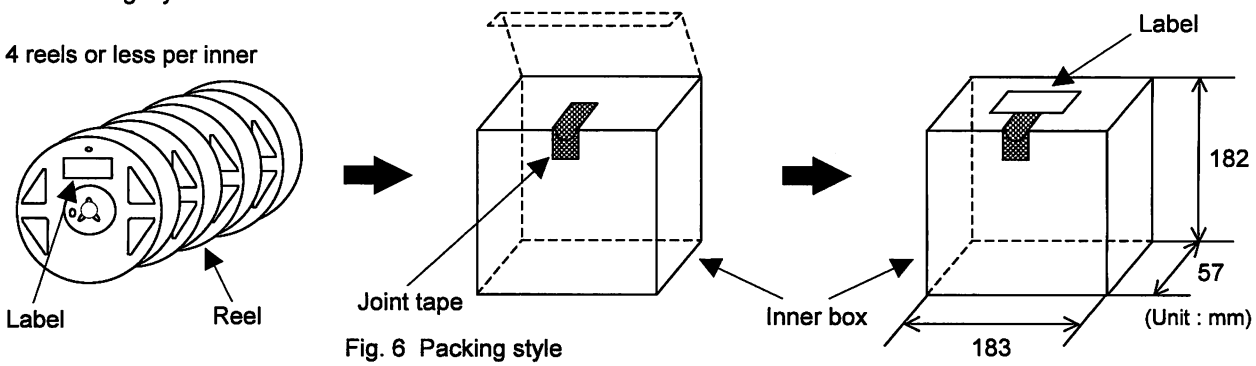
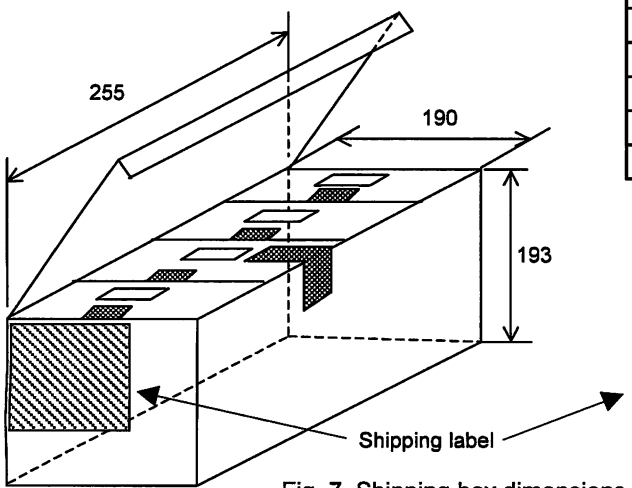


Fig. 6 Packing style

2. 6. Shipping style

4 unit boxes or less per shipping box.



(Unit : mm)

<Ex.>

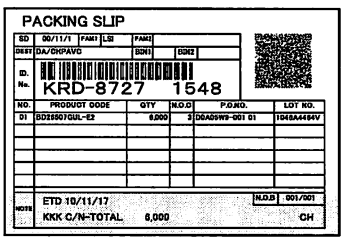


Fig. 7 Shipping box dimensions and shipping style

2.7. Packing materials

Item	Material	Antistatic
Embossed carrier tape	PS	Yes
Cover tape	PET + PE	Yes
Reel	PS	Yes
Unit box	Cardboard	None
Shipping box	Cardboard	None

2. 8. Others

2. 8. 1. Peelback strength

Cover tape peelback strength is 0.2 to 0.7N.

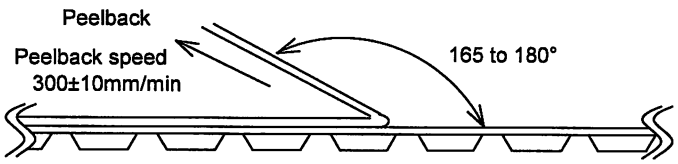


Fig. 8 Test method

2. 8. 2. Missing ICs

(1) No consecutive dropouts.

(2) A maximum 0.1% of specified number of products in each packing may be missing.

3. Storage conditions

3. 1. Storage environment

Recommended storage conditions are as follows :

-Temperature : 5 to 30°C

-Humidity : 40 to 70% RH

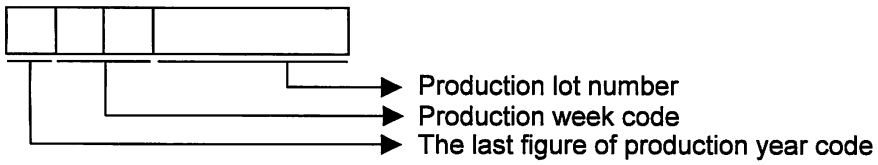
3. 2. Storage period

-Specified storage period : 1 year

3. 3. Specified storage period until soldering

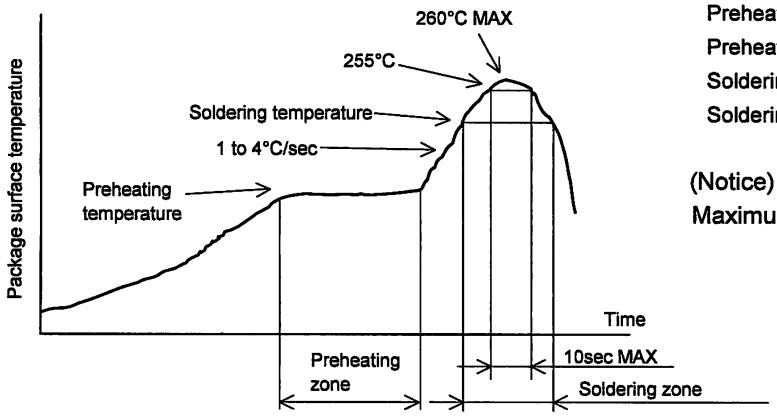
This package dose not require additional drying treatment as long as the moisture condition at the mounting process is within our recommended mounting condition.

4. Marking lot number



5. Soldering conditions

5. 1. Recommended temperature profile for reflow



Preheating temperature ; 130°C to 190°C
Preheating zone ; 120sec MAX
Soldering temperature ; 220°C to 230°C
Soldering zone ; 60sec MAX

(Notice)
Maximum 3-times soldering

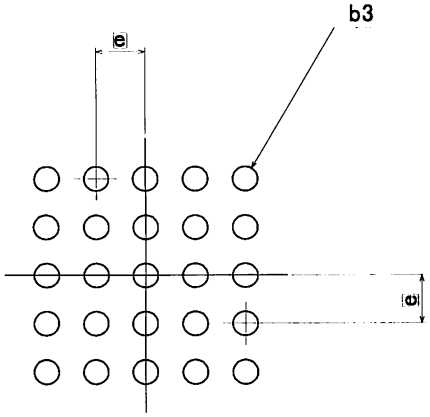
5. 2. About mounting with Sn-Pb solder paste.

Mounting with Sn-Pb solder paste is not recommended because it has a possibility of reducing reliability to connect with Sn-3.0Ag-0.5Cu solder balls.

5. 3. The wave soldering method is not supported.

5. 4. Partial heat supply method (by soldering iron) is not supported.

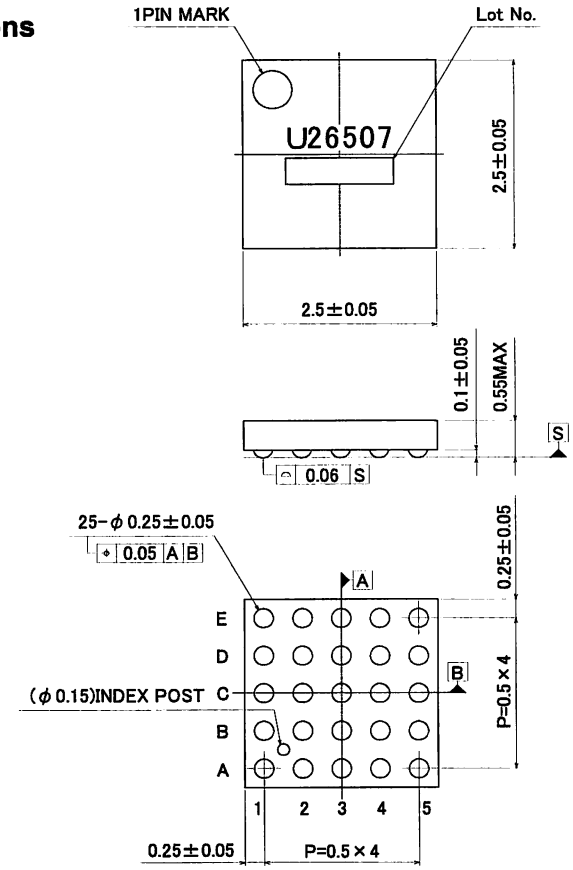
6. Footprint dimensions (Optimize footprint dimensions to the board design and soldering condition)



Symbol	Reference Value
e	0.50
b3	Φ0.25

(Unit : mm)

7. External dimensions



(Unit : mm)

8. Precautions

8. 1. Caution for handling

Silicon substrate surface is exposing to the side of this package.
Therefore, please pay careful attention to chip and crack, and handle without touching the side of package.

8. 2. Regarding the underfill material

In some case, the underfill material is applied in order to reinforce the solder junction of package.
Since there is a case that solder joint reliability may deteriorate according to the resin material or coating condition, please evaluate it sufficiently for its application. In term of the coating condition,
it is preferable that there is an enough material beyond the each four sides of package.

<Preferable example>

(There is a Underfill resin evenly at each four sides.)

<Non preferable example>

(There is little Underfill resin at one or two sides.)