19-5271; Rev 1; 5/10

MAX3639 Evaluation Kit

Evaluates: MAX3639

General Description

The MAX3639 evaluation kit (EV kit) is a fully assembled and tested demonstration board that simplifies evaluation of the MAX3639 low-jitter, wide-frequency range, clock generator. The EV kit includes an on-board 25MHz crystal and switches for selecting different modes of operation. The reference inputs and clock outputs use SMA connectors and are AC-coupled to simplify connection to test equipment.

EV Kit Contents

- **MAX3639 EV Kit Board**

Features

- **Fully Assembled and Tested**
- **On-Board 25MHz Crystal**
- **Switches for Selecting Modes of Operation**
- **SMA Connectors and AC-Coupled Clock I/Os**

Ordering Information

PART	TYPE
MAX3639EVKIT+	EV Kit

+Denotes lead(Pb)-free and RoHS compliant.

Component List

DESIGNATION	QTY	DESCRIPTION
C1–C10, C14, C15, C16, C18–C24, C27–C32, C34–C37	30	0.1µF ±10% ceramic capacitors (0402)
C11	1	2.2µF ±10% ceramic capacitor (0603)
C12	1	0.1µF ±10% ceramic capacitor (0603)
C13	1	33µF ±10% tantalum capacitor (B case) AVX TAJB336K010R
C17	1	27pF ±10% ceramic capacitor (0402)
C25	1	33pF ±10% ceramic capacitor (0402)
C26	1	10µF ±10% ceramic capacitor (0603)
C33	1	3pF ±10% ceramic capacitor (0402)
J1–J9, J11, J13–J24	22	SMA connectors, edge-mount, tab contact Johnson 142-0701-851
J10, J12	2	Test points Keystone 5000
L1, L4, L5, L8, L9, L11, L13, L16, L17, L20, L21, L24, L25, L28, L29, L32, L35, L36	18	Ferrite beads (0402) Murata BLM15HD102SN1
L2, L3, L6, L7, L10, L12, L14, L15, L18, L19, L22, L23, L26, L27, L30, L31, L33, L34	18	4.7µH ±10% inductors (0805) Murata LQM21NN4R7K10
R1–R10, R12, R15–R18, R20, R21, R22	18	150Ω ±1% resistors (0402)
R11	1	49.9Ω ±1% resistor (0402)
R13	1	10.5Ω ±1% resistor (0402)
R14	1	33.2Ω ±1% resistor (0402)
R19	1	499Ω ±1% resistor (0402)
S1–S17	17	Switches, SP3T, slide ALPS SSS211900
S18–S21	4	Switches, SPDT, slide E-Switch EG1218
TP1, TP2	2	Test points Keystone 5000
U1	1	Clock generator (48 TQFN-EP*) Microsemi MAX3639ETM+
U2	1	25MHz crystal NDK EXS00A-AT00429
—	1	PCB: MAX3639 EVALUATION BOARD+, REV B

**EP = Exposed pad.*

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Quick Start

1) Set the switches to the following settings to generate a 156.25MHz LVDS output from the 25MHz crystal reference:

   IN_SEL = XO

   PLL_BP = LOW

   DM = LOW

   DP1 = LOW, DP0 = HIGH

   DF1 = LOW, DF0 = LOW

   DA1 = HIGH, DA0 = LOW

   DB1 = HIGH, DB0 = LOW

   DC1 = HIGH, DC0 = LOW

   QA_CTRL1 = LVDS

   QA_CTRL2 = DISABLED

   QB_CTRL = DISABLED

   QC_CTRL = DISABLED

   QA_TERM1 = LVDS

   QA_TERM2 = LVDS

   QB_TERM = LVDS

   QC_TERM = LVDS

2) Connect a +3.3V supply to VCC (J10) and GND (J12). Set the supply current limit to 500mA.

3) Using SMA cables, connect QA0 (J11) and $\overline{QA0}$ (J13) to a phase noise analyzer or scope. Terminate all unused enabled outputs, QA1 (J14), $\overline{QA1}$ (J15), QA2 (J16), and $\overline{QA2}$ (J17).

Detailed Description

The MAX3639 EV kit simplifies evaluation by providing the hardware needed to evaluate all the MAX3639 functions. Table 1 contains functional descriptions for the switches. Table 2 provides the divider settings for various frequency configurations.

LVCMOS Clock Input

The LVCMOS clock input, CIN, is AC-coupled at the SMA connector and has an on-board 50Ω termination. For optimal performance it is important to use a low-jitter square-wave clock source. Clock signals should be applied to CIN only when the switch IN_SEL is set to CIN.

Differential Clock Input

The differential clock input, DIN, is AC-coupled at the SMA connectors and has an internal 100Ω differential termination. For optimal performance it is important to use a low-jitter, differential, square-wave clock source. Clock signals should be applied to DIN only when the switch IN_SEL is set to DIN.

LVDS/LVPECL Clock Outputs

The LVDS/LVPECL clock outputs (QA[4:0], QB[2:0], QC) are configured using switches S14–S21. Each output has an on-board bias-T, which provides DC bias when configured as LVPECL and AC-coupling for direct connection to 50Ω-terminated test equipment. Unused outputs should be disabled (using switches S14–S17) or have 50Ω terminations placed on the SMA connectors. For optimal jitter measurements, a balun is recommended for differential to single-ended conversion when connected to single-ended test equipment such as a phase noise analyzer. See Figure 1 for the measurement setup.

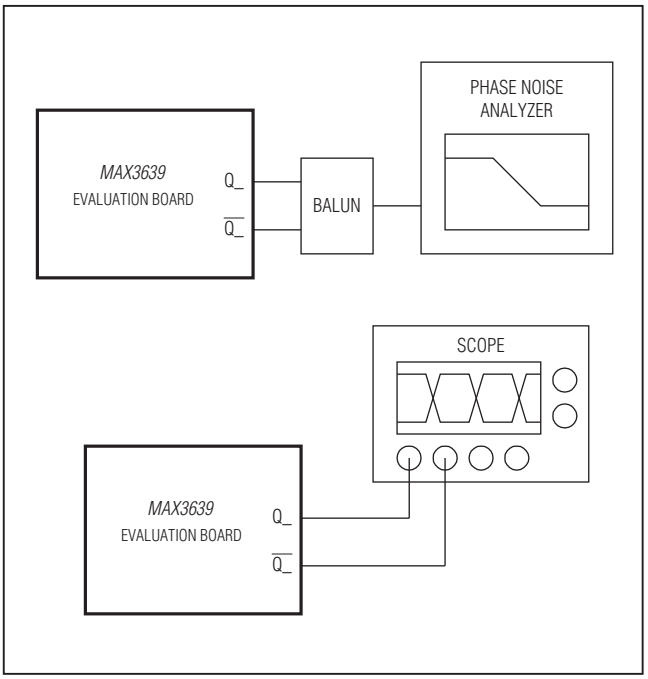

Figure 1. Measurement Setup

LVCMOS Clock Output

The LVCMOS clock output, QCC, has a 500Ω series load resistor and is AC-coupled at the SMA connector. This output can be connected to 50Ω-terminated test equipment, or a high-Z (1MΩ) scope probe. If connected to 50Ω test equipment, the output swing at the termination is approximately 275mV$_{P-P}$.

Table 1. Switch Descriptions

COMPONENT	NAME	FUNCTION
S1	IN_SEL	Selects input reference clock source. DIN = Differential input DIN, $\overline{DIN}$ CIN = LVCMOS input CIN XO = Crystal reference (25MHz on-board)
S2	PLL_BP	Selects PLL bypass mode. HIGH = All outputs PLL bypass OPEN = C output bank PLL bypass LOW = All outputs PLL enabled
S3	DM	Selects input divider M. See Table 2.
S4, S5	DP1, DP0	Selects VCO prescale divider P. See Table 2.
S6, S7	DF1, DF0	Selects feedback divider F. See Table 2.
S8, S9	DA1, DA0	Selects output divider A. See Table 2.
S10, S11	DB1, DB0	Selects output divider B. See Table 2.
S12, S13	DC1, DC0	Selects output divider C. See Table 2.
S14	QA_CTRL1	Selects QA[2:0] output interface (LVPECL, LVDS, or DISABLED).
S15	QA_CTRL2	Selects QA[4:3] output interface (LVPECL, LVDS, or DISABLED).
S16	QB_CTRL	Selects QB[2:0] output interface (LVPECL, LVDS, or DISABLED).
S17	QC_CTRL	Selects QC and QCC output interface. LVPECL = QC output LVPECL, QCC output LVCMOS DISABLED = QC and QCC disabled LVDS = QC output LVDS, QCC output LVCMOS
S18	QA_TERM1	Selects QA[2:0] output termination. Provides DC path to GND for QA[2:0] bias-Ts when switched to LVPECL. DC path to GND is open when switched to LVDS.
S19	QA_TERM2	Selects QA[4:3] output termination. Provides DC path to GND for QA[4:3] bias-Ts when switched to LVPECL. DC path to GND is open when switched to LVDS.
S20	QB_TERM	Selects QB[2:0] output termination. Provides DC path to GND for QB[2:0] bias-Ts when switched to LVPECL. DC path to GND is open when switched to LVDS.
S21	QC_TERM	Selects QC output termination. Provides DC path to GND for QC bias-Ts when switched to LVPECL. DC path to GND is open when switched to LVDS.

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Table 2. Divider Settings for Various Frequency Configurations

INPUT FREQUENCY (MHz)	INPUT DIVIDER	FEEDBACK DIVIDER		VCO FREQUENCY (MHz)	PRESCALE DIVIDER		OUTPUT DIVIDER		OUTPUT FREQUENCY (MHz)	APPLICATIONS
	DM	DF1	DF0		DP1	DP0	DA1 DB1 DC1	DA0 DB0 DC0		
15.36	LOW	OPEN	LOW	3686.4	LOW	LOW	OPEN	OPEN	737.28*	Wireless Base Station: WCDMA, cdma2000®, LTE, TD_SCDMA, WiMAX™, GSM
							LOW	LOW	368.64	
30.72	LOW	HIGH	OPEN				LOW	HIGH	245.76	
							HIGH	LOW	184.32	
61.44	HIGH	HIGH	OPEN				HIGH	OPEN	122.88	
							OPEN	HIGH	92.16	
122.88	OPEN	HIGH	OPEN				LOW	OPEN	61.44	
							OPEN	OPEN	30.72**	
15.36	LOW	LOW	OPEN	3686.4	LOW	HIGH	OPEN	OPEN	614.4*	
19.2	LOW	HIGH	HIGH				LOW	LOW	307.2	
30.72	LOW	LOW	HIGH				LOW	HIGH	204.8	
38.4	LOW	HIGH	LOW				HIGH	LOW	153.6	
61.44	HIGH	LOW	HIGH				HIGH	HIGH	122.88	
76.8	HIGH	HIGH	LOW				HIGH	OPEN	102.4	
122.88	OPEN	LOW	HIGH				OPEN	HIGH	76.8	
153.6	OPEN	HIGH	LOW				LOW	OPEN	51.2	
30.72	LOW	HIGH	HIGH	3932.16	HIGH	LOW	LOW	LOW	491.52	
61.44	HIGH	HIGH	HIGH				HIGH	LOW	245.76	
122.88	OPEN	HIGH	HIGH				OPEN	HIGH	122.88	
							OPEN	LOW	61.44	
13	LOW	HIGH	HIGH	3774	LOW	OPEN	OPEN	OPEN	416*	GSM
26	LOW	HIGH	LOW				HIGH	LOW	104	
52	HIGH	HIGH	LOW				OPEN	HIGH	52	
							OPEN	LOW	26	
25	LOW	LOW	LOW	3750	LOW	HIGH	OPEN	OPEN	625*	Ethernet
31.25	LOW	LOW	HIGH				LOW	LOW	312.5	
62.5	HIGH	LOW	HIGH				HIGH	LOW	156.25	
125	OPEN	LOW	HIGH							
156.25	OPEN	HIGH	LOW				HIGH	HIGH	125	
26.04166	LOW	HIGH	OPEN							
25	LOW	OPEN	HIGH	3750	LOW	LOW	LOW	HIGH	250	
31.25	LOW	HIGH	OPEN				HIGH	LOW	187.5	
62.5	HIGH	HIGH	OPEN				HIGH	HIGH	150	
125	OPEN	HIGH	OPEN				HIGH	OPEN	125	
							LOW	OPEN	62.5	

**Output divider settings applicable only for A and B output banks.*

***Output divider settings applicable only for C output bank.*

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WiMAX is a trademark of WiMAX Forum.

Table 2. Divider Settings for Various Frequency Configurations (continued)

INPUT FREQUENCY (MHz)	INPUT DIVIDER	FEEDBACK DIVIDER		VCO FREQUENCY (MHz)	PRESCALE DIVIDER		OUTPUT DIVIDER		OUTPUT FREQUENCY (MHz)	APPLICATIONS
	DM	DF1	DF0		DP1	DP0	DA1 DB1 DC1	DA0 DB0 DC0		
26.5625	LOW	HIGH	OPEN	3825	LOW	HIGH	LOW	LOW	318.75	FC-SAN
							LOW	HIGH	212.5	
							HIGH	LOW	159.375	
							HIGH	OPEN	106.25	
							LOW	OPEN	53.125	
19.44	LOW	HIGH	HIGH	3732.48	LOW	HIGH	OPEN	OPEN	622.08*	SONET/SDH, STM-N
38.88	LOW	HIGH	LOW				LOW	LOW	311.04	
155.52	OPEN	HIGH	LOW				HIGH	LOW	155.52	
							OPEN	HIGH	77.76	
							OPEN	LOW	38.88	
33.3	LOW	HIGH	OPEN	4000	HIGH	HIGH	LOW	LOW	400	Server, FB-DIMM, Network Processor, DDR/ QDR Memory, PCIe®, SATA
							LOW	HIGH	266.67	
66.7	HIGH	HIGH	OPEN				HIGH	LOW	200	
133.3	OPEN	HIGH	OPEN				HIGH	OPEN	133.333	
25	LOW	HIGH	HIGH				OPEN	HIGH	100	
50	HIGH	HIGH	HIGH				LOW	OPEN	66.67	
100	OPEN	HIGH	HIGH				OPEN	LOW	50	
33.3	LOW	OPEN	HIGH	4000	HIGH	LOW	LOW	LOW	500	
66.7	HIGH	OPEN	HIGH				LOW	HIGH	333.33	
133.3	OPEN	OPEN	HIGH				HIGH	LOW	250	
25	LOW	LOW	OPEN				HIGH	HIGH	200	
50	HIGH	LOW	OPEN							
100	OPEN	LOW	OPEN				HIGH	OPEN	166.67	
31.25	LOW	HIGH	HIGH							
62.5	HIGH	HIGH	HIGH				OPEN	HIGH	125	
125	OPEN	HIGH	HIGH							
20	LOW	LOW	LOW	4000	OPEN	OPEN	OPEN	OPEN	500*	
40	HIGH	LOW	LOW				LOW	LOW	250	
80	OPEN	LOW	LOW				LOW	HIGH	166.67	
25	LOW	LOW	HIGH				HIGH	LOW	125	
50	HIGH	LOW	HIGH				HIGH	HIGH	100	
100	OPEN	LOW	HIGH							
15.625	LOW	HIGH	HIGH				OPEN	HIGH	62.5	
31.25	LOW	HIGH	LOW							
62.5	HIGH	HIGH	LOW				OPEN	LOW	31.25	
125	OPEN	HIGH	LOW							

**Output divider settings applicable only for A and B output banks.*

***Output divider settings applicable only for C output bank.*

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Table 2. Divider Settings for Various Frequency Configurations (continued)

INPUT FREQUENCY (MHz)	INPUT DIVIDER	FEEDBACK DIVIDER		VCO FREQUENCY (MHz)	PRESCALE DIVIDER		OUTPUT DIVIDER		OUTPUT FREQUENCY (MHz)	APPLICATIONS
	DM	DF1	DF0		DP1	DP0	DA1 DB1 DC1	DA0 DB0 DC0		
32.76	LOW	HIGH	OPEN	3931.2	HIGH	HIGH	HIGH	OPEN	131.04	Microwave Radio Link
							LOW	OPEN	65.52	
20.82857	LOW	HIGH	HIGH	3999.084	HIGH	OPEN	OPEN	OPEN	666.514*	OTU1, 10Gbps SONET with FEC
41.6571	LOW	HIGH	LOW				LOW	LOW	333.257	
							HIGH	LOW	166.6285	
25.78125	LOW	LOW	LOW	3867.1875	HIGH	OPEN	OPEN	OPEN	644.53125*	10Gbps Ethernet with FEC
							HIGH	LOW	161.1328125	
27.392578	LOW	HIGH	OPEN	3944.531232	HIGH	OPEN	OPEN	OPEN	657.421872*	10Gbps FC
							HIGH	LOW	164.355468	
20.916	LOW	HIGH	HIGH	4015.95949	HIGH	OPEN	OPEN	OPEN	669.3265*	OTU2, 10Gbps SONET with Digital Wrapper
41.8329	LOW	HIGH	LOW				LOW	LOW	334.66	
							HIGH	LOW	167.33	

**Output divider settings applicable only for A and B output banks.*

***Output divider settings applicable only for C output bank.*

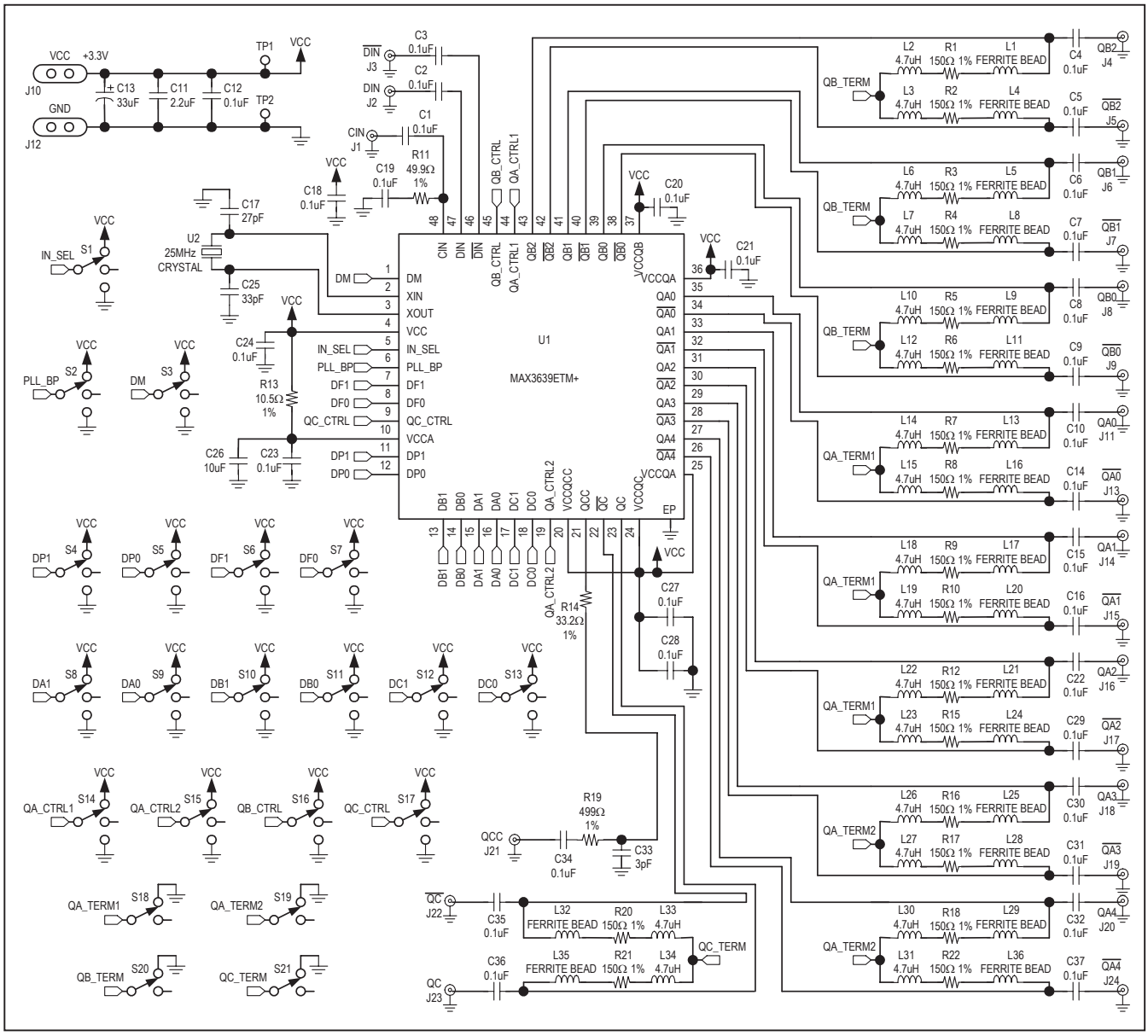

Figure 2. MAX3639 EV Kit Schematic

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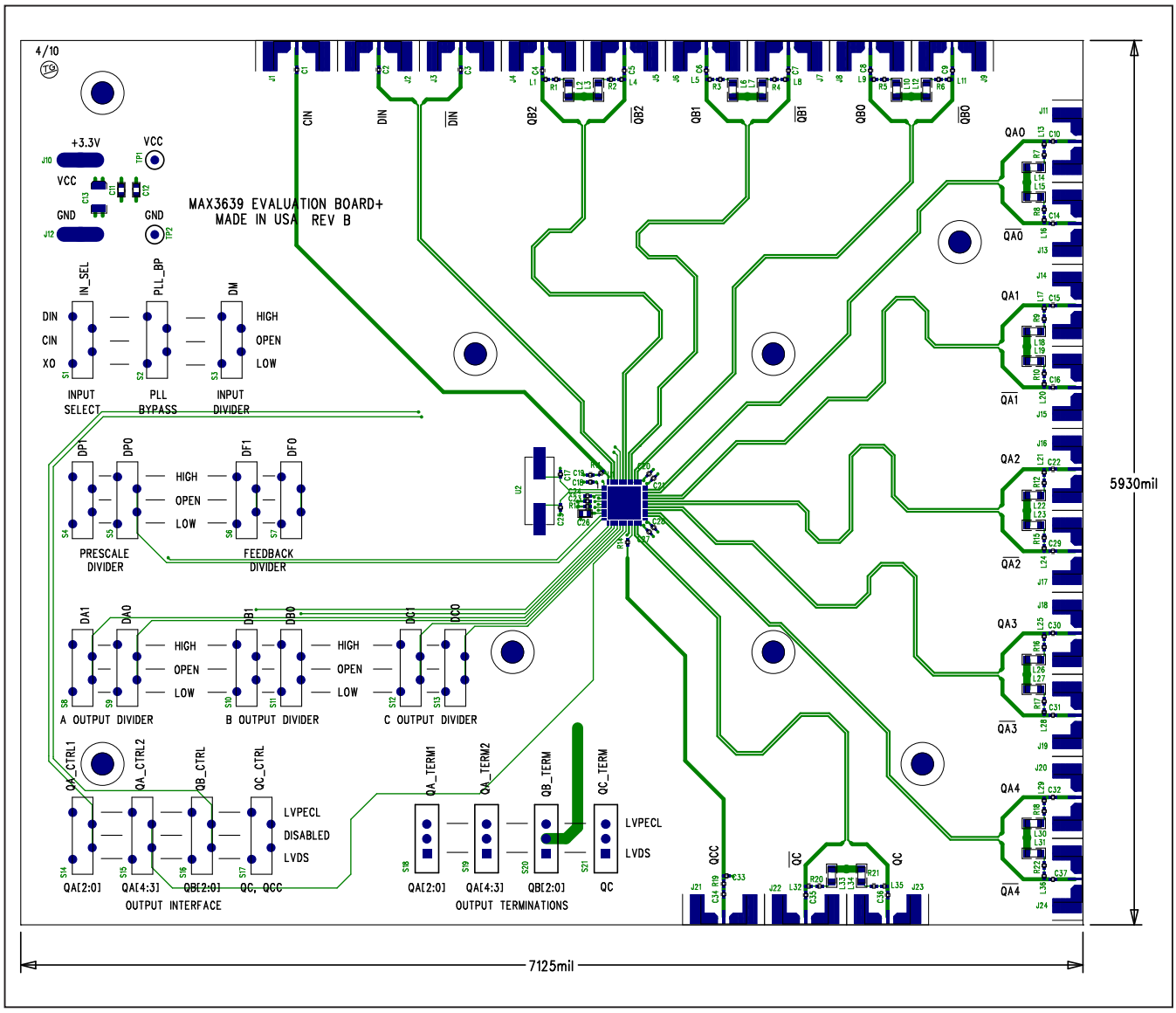

Figure 3. MAX3639 EV Kit Component Placement Guide—Component Side

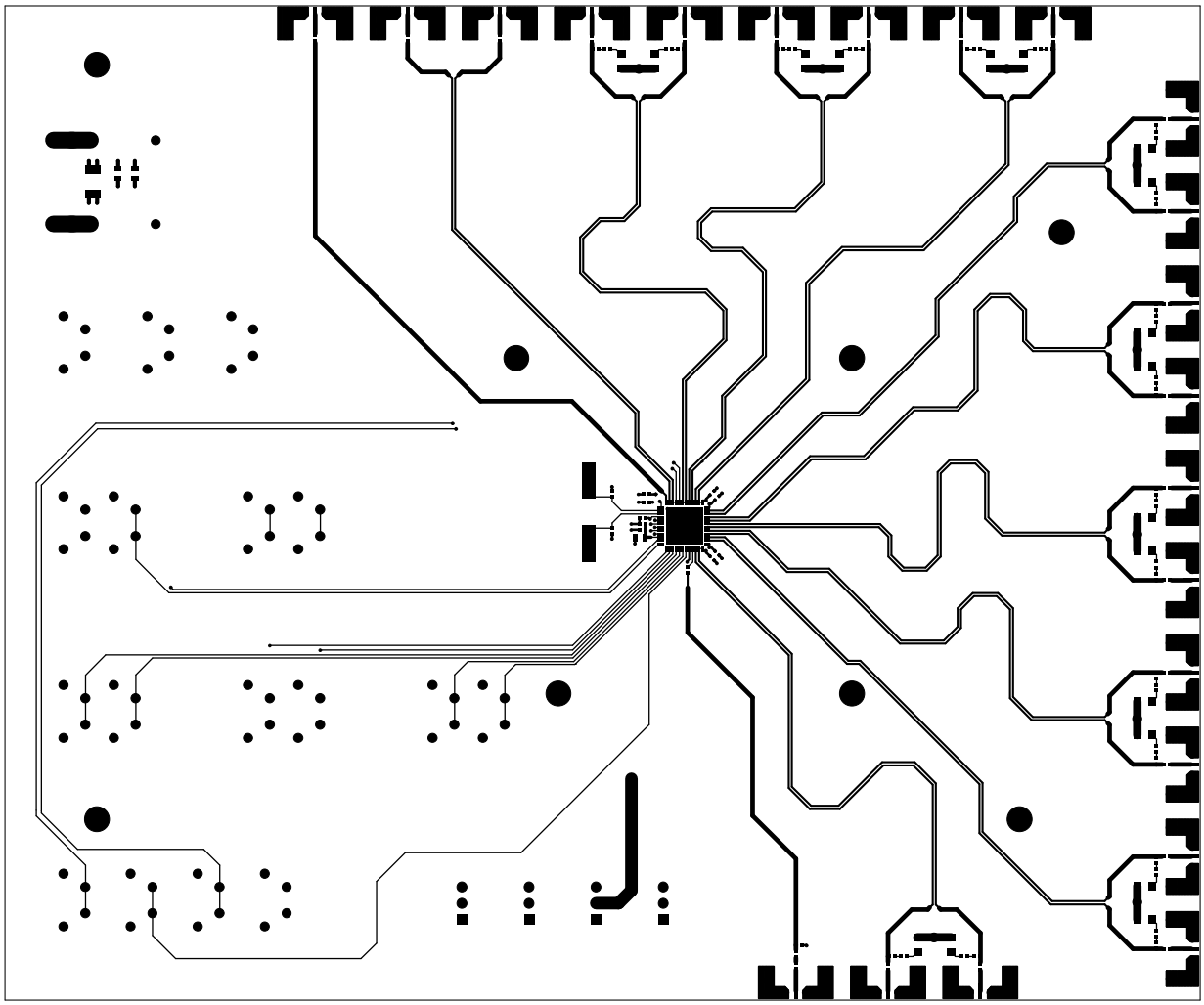

Figure 4. MAX3639 EV Kit PCB Layout—Component Side

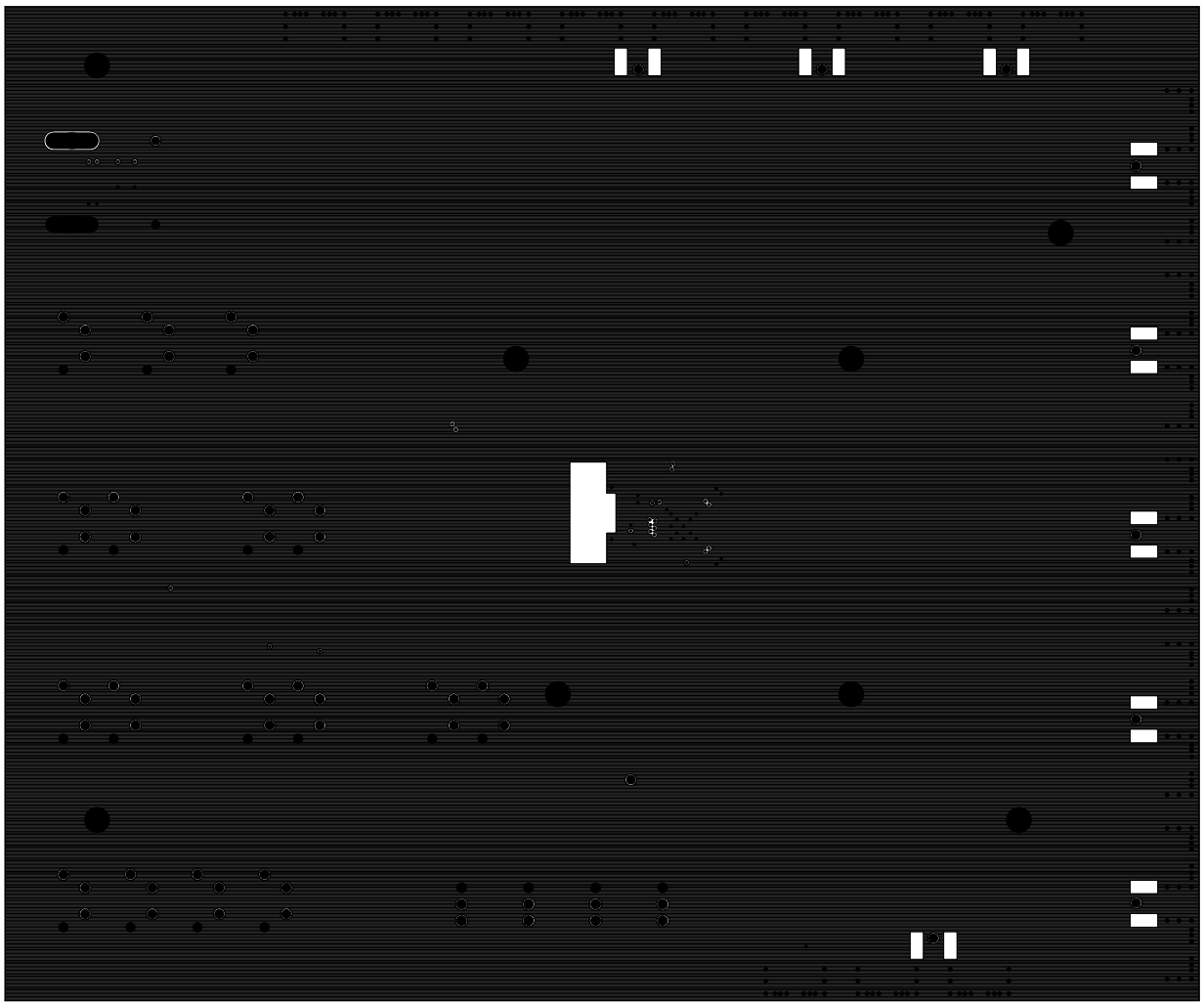

Figure 5. MAX3639 EV Kit PCB Layout—Ground Plane

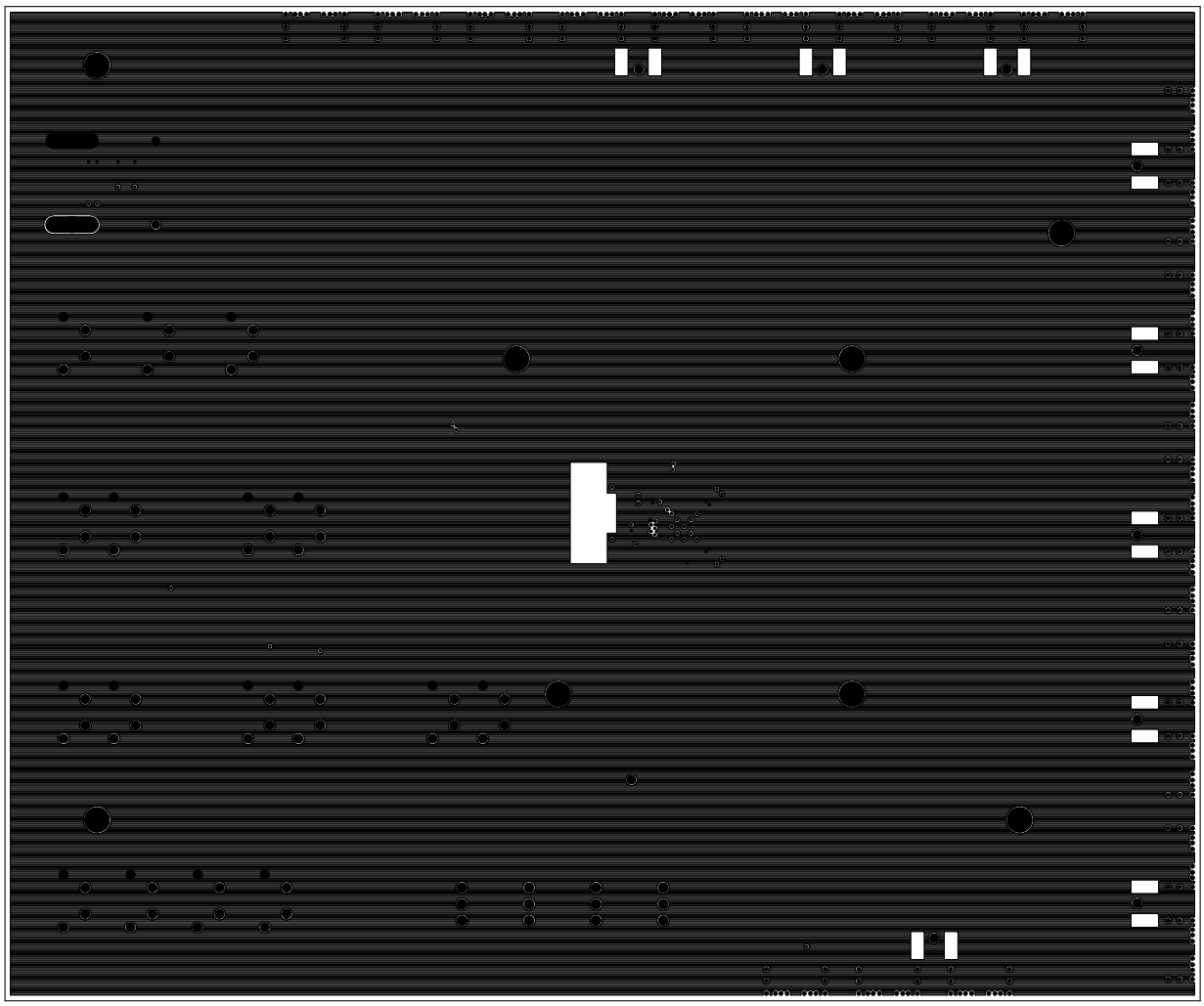

Figure 6. MAX3639 EV Kit PCB Layout—Power Plane

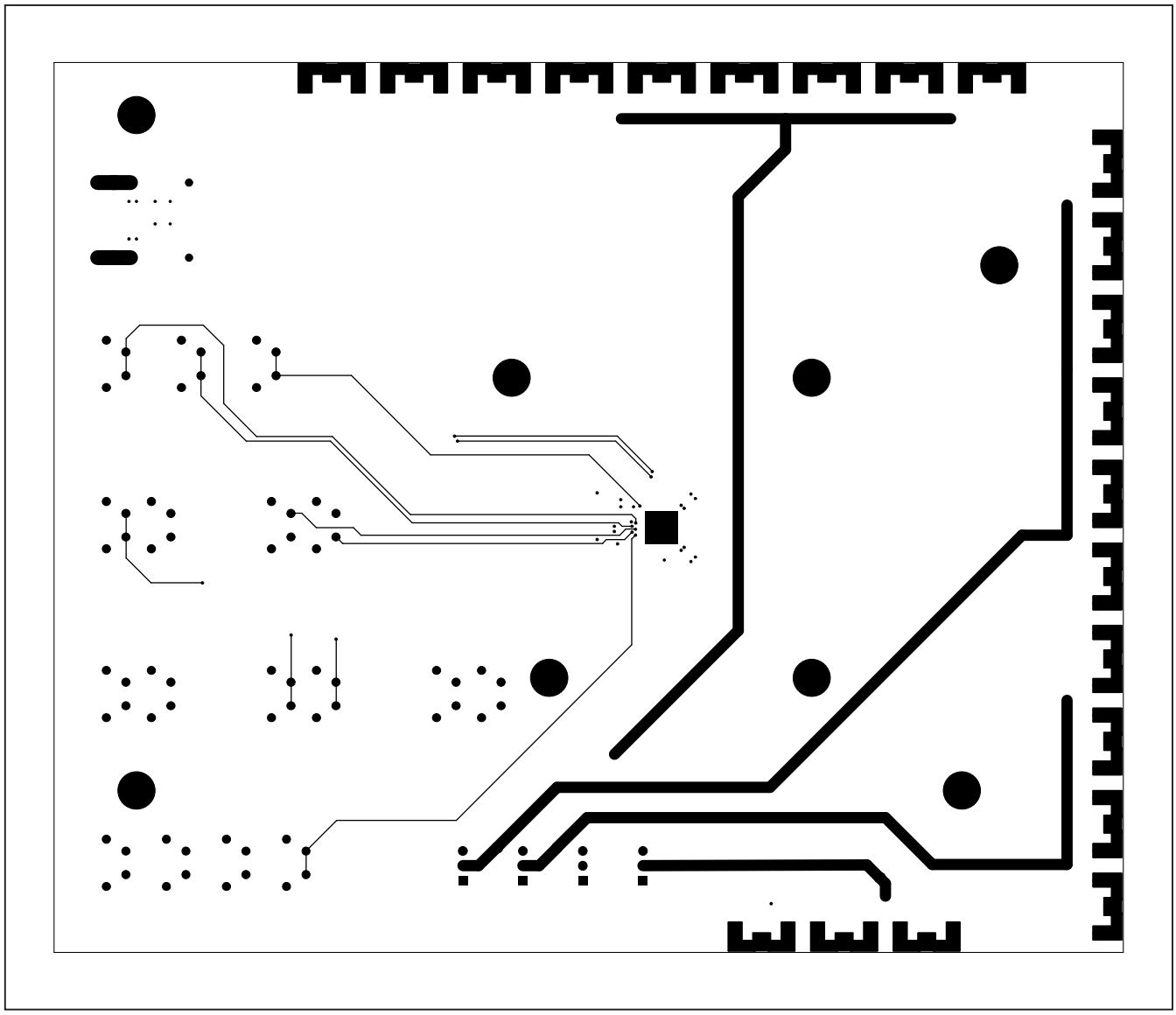

Figure 7. MAX3639 EV Kit PCB Layout—Solder Side

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/10	Initial release	—
1	5/10	Changed R13 from 10.0Ω to 10.5Ω in the *Component List* and Figure 2; corrected the label for L28 in Figure 2	1, 7

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