UG0617
User Guide
RTG4 FPGA Development Kit

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Power Matters.™

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 5.0

Removed information about the manufacturing test and renamed Chapter 8 as Software Installation, page 42.

1.2 Revision 4.0

The following is a summary of the changes made in revision 4.0 of this document.

- Information about the jumper settings required for programming the device using FlashPro4 was updated. The concerned section is deleted.

1.3 Revision 3.0

The following is a summary of the changes made in revision 3.0 of this document.

- The procedure for measuring 1.2 V current sensing during normal operation was updated. For more information, see 1.2 V Current Sensing for Normal Operation, page 11 (SAR 75660).

1.4 Revision 2.0

The following is a summary of the changes made in revision 2.0 of this document.

- The J34 and J12 FMC connector pinouts were updated. For more information, see Table 15, page 25 and Table 16, page 31 (SAR 75871).
- The specifications for the Marvell PHY were updated. For more information, see Marvell PHY (88E1340S), page 18 (SAR 74316).
- The clock oscillator specifications were updated. For more information, see Clock Oscillator, page 21 (SAR 77521).
- The kit contents were updated. For more information, see Kit Contents, page 2 (SAR 79281).
- The RTG4 Development Kit Block Diagram was updated. For more information, see Figure 1, page 3 (SAR 80330).

1.5 Revision 1.0

Revision 1.0 was the first publication of this document.

2 Introduction

The Microsemi RTG4™ Field Programmable Gate Array (FPGA) Development Kit provides designers with an evaluation and development platform for applications such as data transmission, serial connectivity, bus interface, and high-speed designs using the RTG4 devices. The development board features an RT4G150 device offering 151,824 logic elements in a ceramic package with 1,657 pins.

The RTG4 Development Board includes two 1 GB Double Data Rate 3 (DDR3) memories and two 1 GB of SPI flash memories. The board also has several standard and advanced peripherals, such as PCIe x4 edge connector, two FMC connectors for using several off-the-shelf daughter cards, USB, Philips interintegrated circuit (I^2C), gigabit Ethernet port, serial peripheral interface (SPI), and UART. A high-precision operational amplifier circuitry on the board helps measure the device core power consumption. A FlashPro programmer is embedded on the board, which allows RTG4 FPGA programming through the JTAG interface.

2.1 Kit Contents

The following table lists the contents of the RTG4 Development Kit.

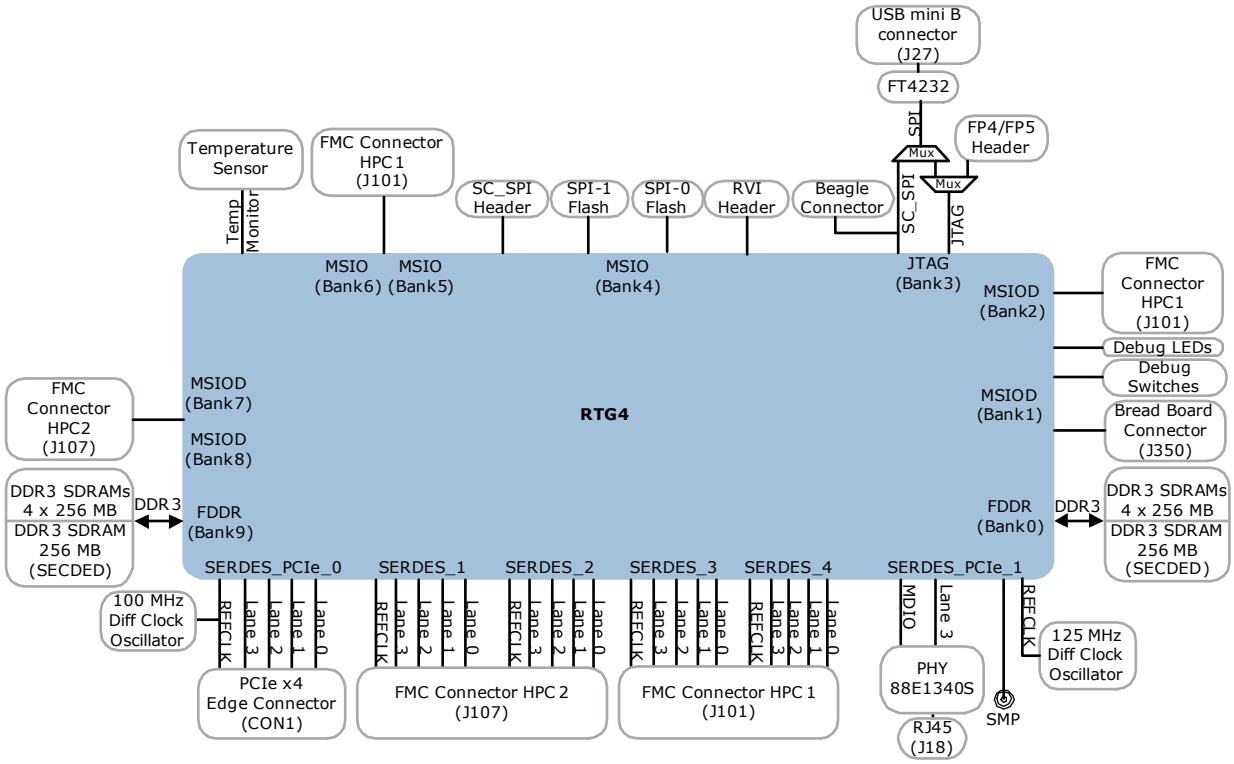
Table 1 • **Kit Contents**

Item	Quantity
RTG4 Development Board with one RT4G150 PROTO FPGA in either a CB1657 or CG1657 package	1
USB A-male to micro-B male cable, three feet long 28/28AWG USB 2	1
USB A to mini-B cable	1
12 V, 5 A AC power adapter	1
Quickstart card	1

2.2 Block Diagram

The following figure shows the RTG4 Development Kit block diagram.

Figure 1 • **RTG4 Development Kit Block Diagram**



2.3 Web Resources

More information about the RTG4 Development Kit is available at *http://www.microsemi.com/products/fpga-soc/design-resources/dev-kits/rtg4-development-kit*.

2.4 Board Description

The RTG4 Development Kit offers a full-featured 150,000 logic element (LE) RTG4 FPGA. The board integrates the following features on a single chip:

- Radiation-tolerant, flash-based FPGA fabric.
- Industry standard 4-input lookup table-based (LUT) FPGA fabric with integrated math blocks.
- High-performance SerDes.
- Integrated hard DDR3 memory controllers with error correction.
- Static random-access memory (SRAM).
- Programmable read-only memory (µPROM).

The RTG4 Development Kit has as the following standard interfaces:

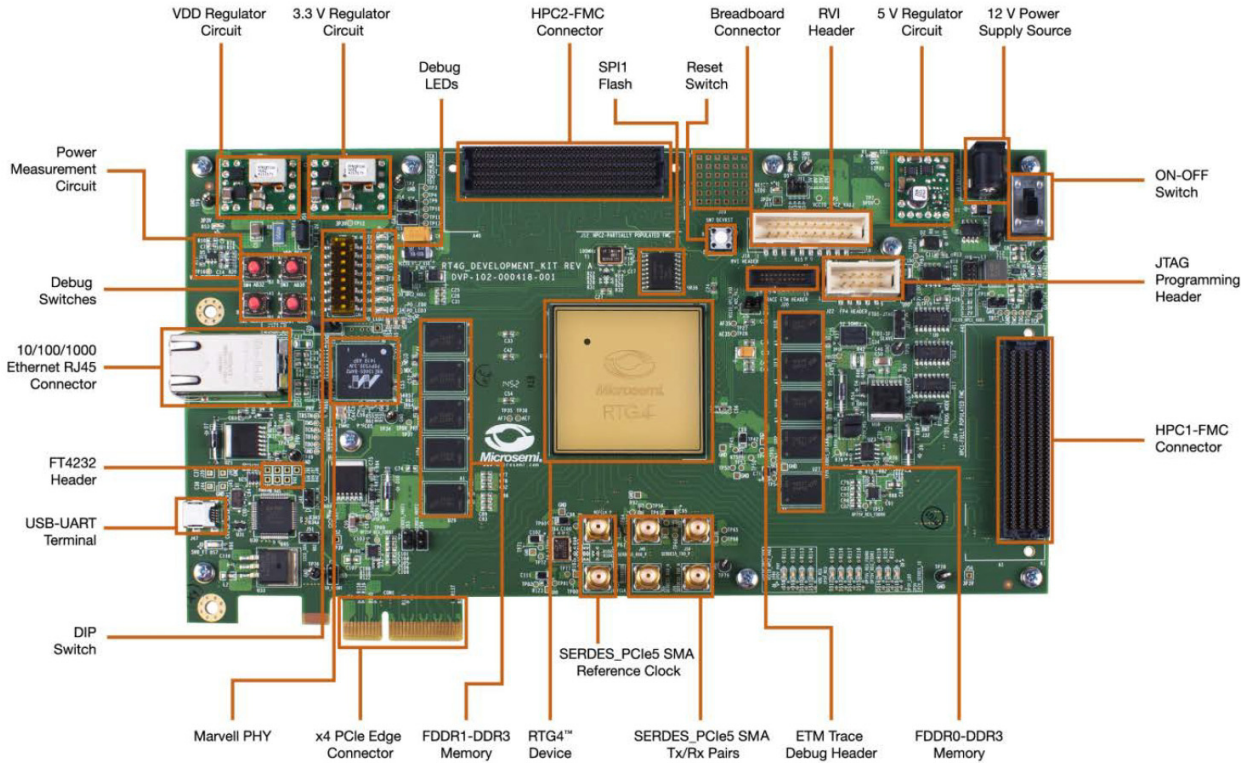
- Two independent 1 GB DDR3 synchronous dynamic random access memory (SDRAM).
- Two independent 1 GB SPI flash memories.
- PCIe (Gen1) x1 interface accessible through SMA cables.
- PCIe x4 edge connector.
- One pair SMA connectors for testing the full-duplex SerDes channel.
- Two FMC connectors with HPC pin-out for expansion.
- RJ45 interface for 10/100/1000 Ethernet.
- USB micro-AB connector.
- Headers for SPI and GPIOs.
- FTDI programmer interface to program the external SPI flash.

- JTAG programming interface.
- RVI header for application programming and debug.
- FlashPro4 or FlashPro5 programming header and embedded FlashPro5 programmer.
- Dual in-line package (DIP) switches for user application.
- Push-button switches and LEDs for demo purposes.
- Current measurement test points.

The unused MSIO signals are routed to the on-board FMC connectors and unused MSIOD signals are routed to bread board connector (J10) space.

The following figure shows the RTG4 Development Board.

Figure 2 • **RTG4 Development Board**



2.5 Board Key Components

The following table lists key components of the RTG4 Development Board.

Table 2 • **RTG4 Development Board Components**

Name	Description
RTG4 FPGA	Microsemi RT4G150 device in a ceramic package with 1,657 pins.
DDR3 synchronous dynamic random access memory (SDRAM)	8 × 256 MB (256 MB Micron DDR3 memories MT41K256M8DA-125 IT:K) for storing data. 2 × 256 MB (512 MB Micron DDR3 memory MT41K256M8DA-125 IT:K) for storing the ECC bits.
SPI Flash	2 gigabit (2 ×1 Gigabit) SPI flash Micron N25Q00AA13GSF40G chips connected to the MSIO pins of the RTG4 FPGA.
Ethernet	RJ45 connector (Ethernet jack with magnetics) interfacing with a Marvell 10/100/1000 BASE-T PHY chip 88E1304S in Serial Gigabit Media Independent Interface (SGMII) mode, interfacing with the Ethernet port of the RTG4 device (on-chip MAC and external PHY).

Table 2 • **RTG4 Development Board Components**

Name	Description
RVI Header	RVI header for application programming and debug from Keil ULINK or IAR J-Link.
Embedded FlashPro5	Embedded FlashPro5 for RTG4 programming and debugging with Microsemi tools.
Future Technology Devices International (FTDI) programmer	FTDI programmer interface (J47) to program the external SPI flash. An FTDI chip is also used to change the JTAG_SEL signal (high or low) remotely for switching between the RVI header and JTAG mode.
Embedded trace macro (ETM) cell header	ETM header for debug.
PCIe edge connector	PCI Express edge connector with four lanes.
Light-emitting diodes (LEDs)	Eight active-low LEDs connected to some of the user I/Os for debugging/ testing.
Push-button reset	Active-low push-button system reset for the RTG4 device.
Push-button and DIP switches	Four active-low push-button switches and one DIP switch for test and navigation.
FMC connectors	Two FMC connectors to connect the external daughter boards. Connector array socket 400 pins (40 × 10), 1.27 mm pitch. The SerDes pins and unused user MSIO/MSIOD are routed from the RTG4 device to the J34 and J12 connectors.
Chip	A simple three-pin voltage monitor and power-on reset that holds reset for 150 ms for stabilization after the power returns to tolerance.
OSC-100	100 MHz clock oscillator (differential output) used for SERDES_PCIe_0 interface.
OSC-100	100 MHz clock oscillator (differential output) connected to RTG4 pins AB37 and AB3.
OSC-125	125 MHz clock oscillator (differential output) used for SERDES_PCIe_1 interface.
OSC-50	50 MHz single-ended clock source connected to RTG4 pin AA39 (MSIOD73PB1/GB12_23/CCC_NE0_CLKI2).
FT4232H	USB-to-quad serial ports in various configurations.
TPS3808G09DBVR	A supervisory circuit that monitors system core voltage, asserting an open-drain reset signal when the sense voltage drops below a preset threshold or when the manual reset (MR) pin drops to a logical low.
LM99CIMM	A remote diode temperature sensor with a two-wire System Management Bus (SMBus) serial interface connected to pin AK31 - Temp Monitor.
HTST-110-01-L-DV	RVI header J18.

3 Installation and Settings

This section provides information about the software and hardware settings for the RTG4 Development Kit.

3.1 Software Installation

Download and install the latest Microsemi Libero® System-on-Chip (SoC) software from the Microsemi website and obtain a Platinum license, which is not included in the RTG4 Development Kit. Libero v11.4 or later installer has FlashPro5 drivers. For instructions on how to install the Libero software and SoftConsole, see *Libero Software Installation and Licensing Guide*.

For instructions on how to download and install Microsemi DirectCores, SGCores, and driver firmware cores, see *Installing IP Cores and Drivers User Guide*. In order to design with Microsemi FPGAs and SoC, these IP cores must be installed on the PC where Libero SoC is installed while designing with Microsemi FPGAs and SoCs.

3.2 Hardware Settings

This section provides information about default jumper settings, switches, LEDs, and DIP switches for the RTG4 Development Kit.

3.2.1 Default Jumpers Settings

Connect the jumpers with the default settings specified in the following table to evaluate the pre-programmed demo design.

Table 3 • **Jumper Settings**

Jumper	Description	Pin	Default Settings
Power Supply			
J16	Jumper to select the RTG4 core voltage VDD_REG to 1.2 V	Pin 1-2 for 1.0 V core voltage. Core supply 1.0 V operation is not supported.	Open
		Pin 2-3 for 1.2 V core voltage.	Closed
J19	Jumper to select the voltage levels for MSIO-FMC connector (VCCIO_HPC1_VADJ) to 3.3 V, 2.5 V, 1.8 V, 1.5 V, or 1.2 V	Pin 1-2 for 3.3 V.	Closed
		Pin 3-4 for 2.5 V.	Open
		Pin 5-6 for 1.8 V.	Open
		Pin 7-8 for 1.5 V.	Open
		Pin 9-10 for 1.2 V.	Open
J11	Jumper to select the voltage levels for MSIOD-FMC connector (VCCIO_HPC2_VADJ) to 2.5 V or 1.8 V or 1.5 V or 1.2 V	Pin 1-2 for 2.5 V.	Closed
		Pin 3-4 for 1.8 V.	Open
		Pin 5-6 for 1.5 V.	Open
		Pin 7-8 for 1.2 V.	Open
J26	Jumper to short VCCIO_HPC1_VIO_B_M2C_FMC supply to 2P5	Two-pin header.	Closed
J21	Jumper to short VCCIO_HPC2_VIO_B_M2C_FMC supply to VCCIO_HPC2_VADJ	Two-pin header.	Closed

Table 3 • **Jumper Settings *(continued)***

Jumper	Description	Pin	Default Settings
Power Supply			
J17	Jumper to select either SW6 input or ENABLE_FT4232 signal from FT4232H chip	Pin 1-2 for SW6 selection.	Closed
		Pin 2-3 for Enable_FT4232 signal control.	Open
J23	Jumper to short VPP with 3P3V_LDO	Two-pin header.	Closed
J33	Jumper for SERDES VDDIO	Pin 1-2.	Closed
		Pin 3-4.	Closed
Marvell PHY			
J28	Jumper to select either PHY_CONFIG1 or M2S_PHY_CONFIG1 for Global hardware configuration CONFIG[1]	Pin 1-2 to connect CONFIG [1] to P2_LED[2] pin of 88E1340S.	Open
		Pin 2-3 to connect CONFIG [1] to RTG4-B31 pin MSIO328PB4.	Open
J31	Jumper to short AC test points for debugging (It is recommended not to connect, refer to Marvell PHY Datasheet)	Two-pin header.	Open
Programming			
J32	JTAG selection jumper to select between JTAG programming mode or FTDI programming mode	Pin 1-2 for embedded FlashPro5 JTAG programming.	Closed
		Pin 2-3 for external FlashPro4 programming header.	Open
		Pin 2-4 for JTAG_SEL pin to DD1 signal of FT4232H chip.	Open
J27	Jumper to select FTDI JTAG/SPI slave programming	Pin 1-2 for FTDI JTAG programming.	Closed
		Pin 2-3 for FTDI SPI Slave programming.	Open
J51	Jumper to short BD2 and BD1 pins of FT4232 chip	Two-pin header.	Open
J46	Jumper to control the signal “ENABLE_FT4232” through FTDI chip	Two-pin header.	Open

For locations of various jumpers and test points on the RTG4 Development Board, see Figure 19, page 39.

3.2.2 LEDs

The following table lists the power supply and Ethernet LEDs.

Table 4 • **LEDs**

LED	Description
DS12	VDD_REG supply
DS13	1P5V_REG supply
DS14	0P75V_REG_FDDR0 supply
DS15	0P75V_REG_FDDR1 supply

Table 4 • **LEDs *(continued)***

LED	Description
DS8	VCCIO_HPC1_VADJ supply
DS9	VCCIO_HPC2_VADJ supply
DS10	1P8V supply
DS11	1P0V_PHY supply
DS16	3P3V_LDO supply
DS17	2P5V supply
DS18	1P2V_SERDES_IO supply
DS3	3P3V supply
DS2	5P0V supply
DS1	12P0V supply
DS7	VCC_BUS supply
DS5	Power supply connected to parallel LED output port 0 (P0_LED[0]) of Marvell PHY
DS4	Power supply connected to parallel LED output port 0 (P0_LED[2]) of Marvell PHY
DS6	Power supply connected to parallel LED output port 0 (P0_LED[3]) of Marvell PHY

3.2.3 Test Points

The following table lists USB, ground, and other test points.

Table 5 • **Test Points**

Test Point	Description
TP1, TP2, TP76	GND
TP14	VDD_REG
TP7	5 V
TP12	3.3 V
TP19	3P3V_LDO
TP30	2P5V
TP59	1.5 V
TP57	0.75 V (FDDR0)
TP69	0.75 V (FDDR1)
TP18	VCCIO_HPC1_VAD
TP5	VCCIO_HPC2_VAD
TP43	1.8 V
TP37	PHY 1.0 V
TP48	1P2V_SERDES_IO

3.3 Power Sources

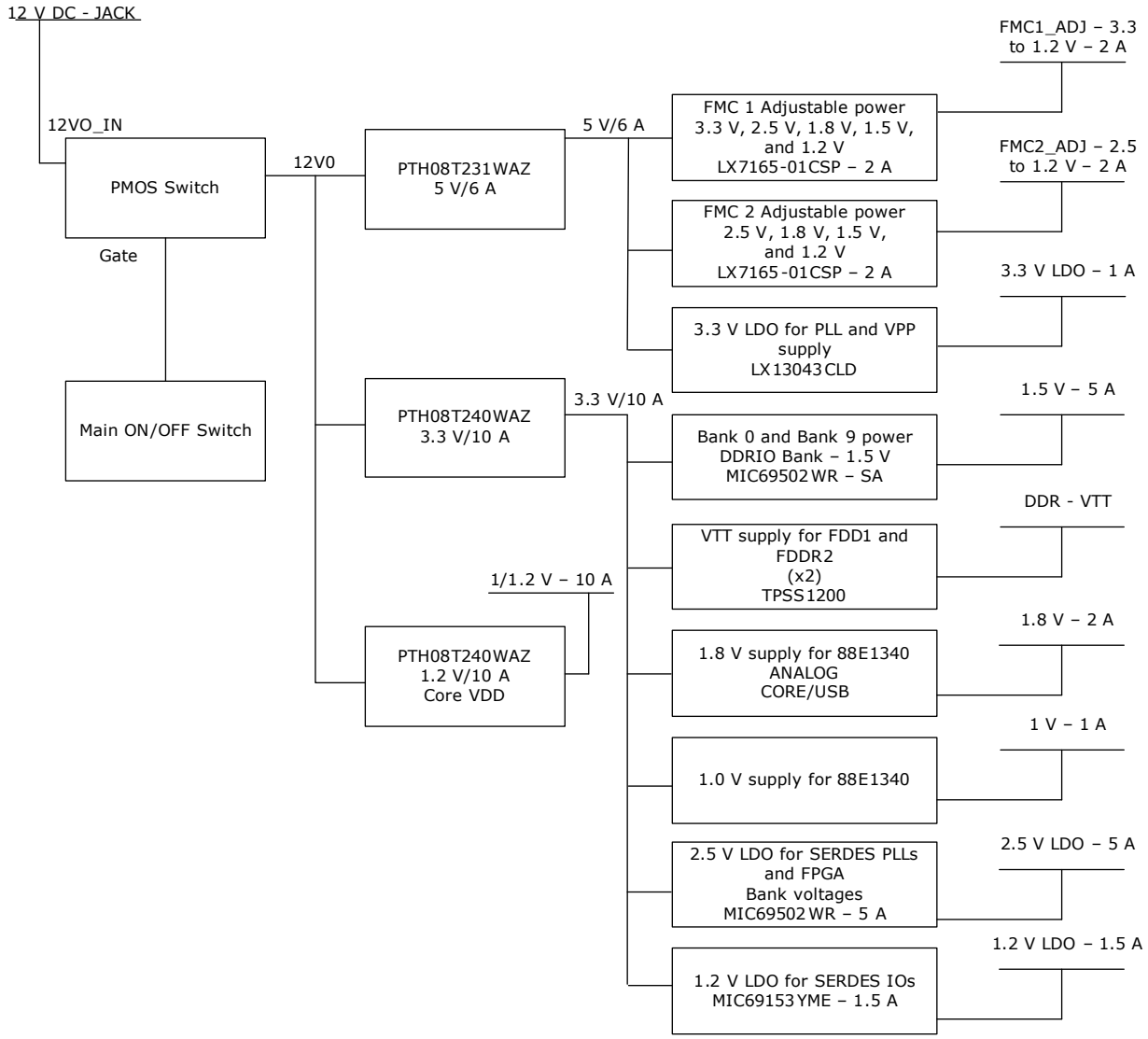
The following table lists the key power supplies required for normal operation of the RTG4 Development Kit.

Table 6 • **I/O Voltage Rails**

RTG4 Bank	I/O Rail	Voltage
Bank0	1P5V_REG	1.5 V
Bank1	2P5V	2.5 V
Bank2	VCCIO_HPC1_VIO_B_M2C_FMC	1.5 V
Bank3	3P3V	3.3 V
Bank4	3P3V	3.3 V
Bank5	VCCIO_HPC1_VADJ	3.3 V, 2.5 V, 1.8 V, 1.5 V, or 1.2 V
Bank6	VCCIO_HPC1_VADJ	3.3 V, 2.5 V, 1.8 V, 1.5 V, or 1.2 V
Bank7	VCCIO_HPC2_VIO_B_M2C_FMC	2.5 V, 1.8 V, 1.5 V, or 1.2 V
Bank8	VCCIO_HPC2_VADJ	2.5 V, 1.8 V, 1.5 V, or 1.2 V
Bank9	1P5V_REG	2.5 V
VDD	VDD_REG	1.2 V or 1.0 V
VPP	VPP	3.3 V
VREF0	0P75V_VTT_REF_FDDR0	0.75 V
VREF9	0P75V_VTT_REF_FDDR1	0.75 V
SERDES_VDDI	2P5V	2.5 V
VDDPLL	3P3V_LDO	3.3 V

The following figure shows the voltage rails (12 V, 5 V, 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, 1.0 V, and 0.75 V) available in the RTG4 Development Kit.

Figure 3 • **Voltage Rails in the RTG4 Development Kit**



4 Key Components Description and Operation

This section describes the key component interfaces of the RTG4 Development Kit. For device datasheets, see *http://www.microsemi.com/products/fpga-soc/design-resources/dev-kits/rtg4-development-kit*.

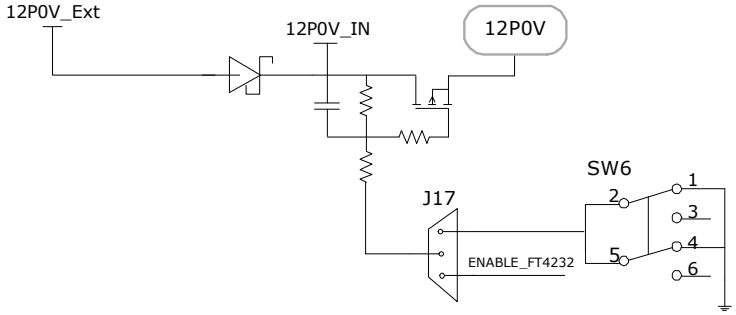
4.1 Powering Up the Board

The RTG4 Development Board is powered using a 12 V external DC jack (12P0V_Ext), as shown in the following figure.

To power up the board:

1. Connect the 12 V power supply brick to the **J9** to supply power to the board.
2. Switch ON the **SW6** power supply switch.

Figure 4 • **Powering Up the Board**



4.2 Current Measurement

This section provides information about current sensing in various modes.

4.2.1 1.2 V Current Sensing for Normal Operation

For applications that require current measurement, high-precision operational amplifier circuitry (U5 with gain 5) is provided on the board to measure the output voltage at the **TP16** test point.

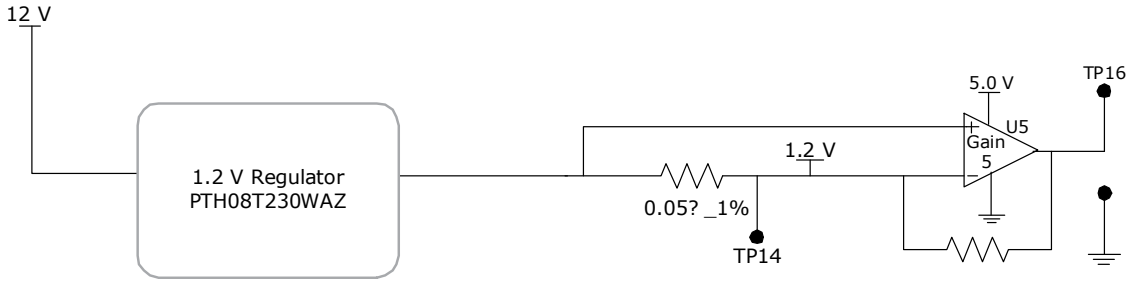
The following steps describe how to measure the core power.

1. Measure the output voltage (V_{out}) at TP16.
2. I = V_{out}/(5*0.05), where 5 is the gain of the operational amplifier U5 and 0.05 is the current sense resistor value in ohms.
3. P = VI, where V is voltage at TP14 and I is voltage at TP16*4.
4. Therefore, core power consumed (P) = V(TP14)*V(TP16)*4.

For example, when the voltage measured across TP16 is 0.5 V, the core power consumed is 2.4 W.

The following figure shows the on-board core power measurement circuity.

Figure 5 • **Core Power Measurement**



4.3 Memory Interface

RTG4 fabric I/Os are provided for the FDRR_E and FDDR_W memories shown in the following figure.

4.3.1 FDDR_E and FDDR_W—DDR3 SDRAM

Each FDDR is provided with four chips of 256 MB DDR3 memory as flexible volatile memory for storing user data. A chip with 256 MB DDR3 memory is provided for ECC. The single-error correction and double-error detection (SECDED) feature can be enabled using ECC. The DDR3 interface is implemented in Bank2.

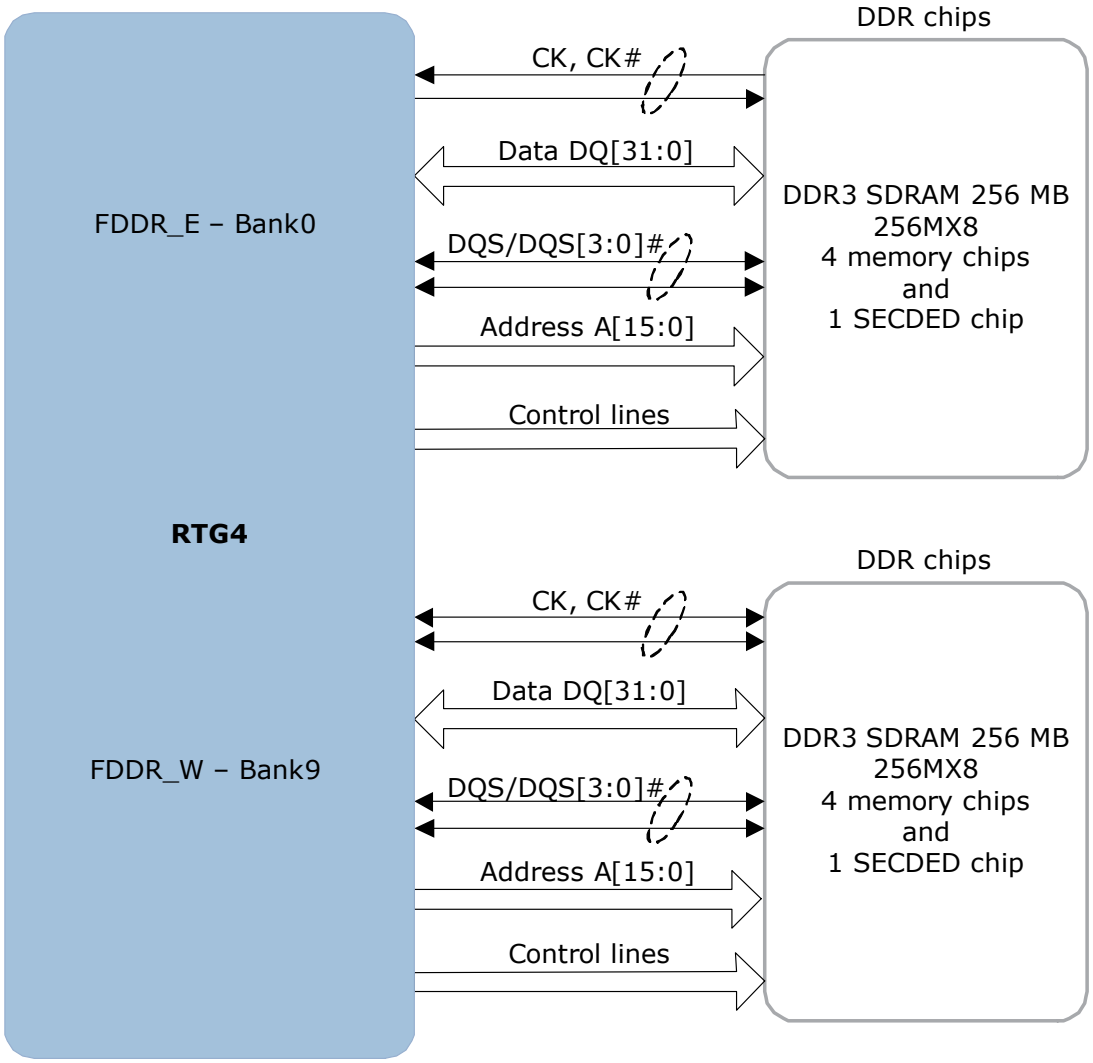
The following list describes features of the memory interface:

- MT41K256M8: 32 Meg × 8 × 8 banks
- Density: 256 MB
- Clock rate: 333 MHz
- Data rate: DDR3, 666 MHz
- Total capacity: 1 GB from four chips

Note: For more information, see the Board Level Schematics document (provided separately).

The following figure shows the memory interface of the RTG4 Development Board.

Figure 6 • **Memory Interface**



Note: DDR3 chip supports single bit error correction and dual bit error detection.

4.4 SerDes Interface

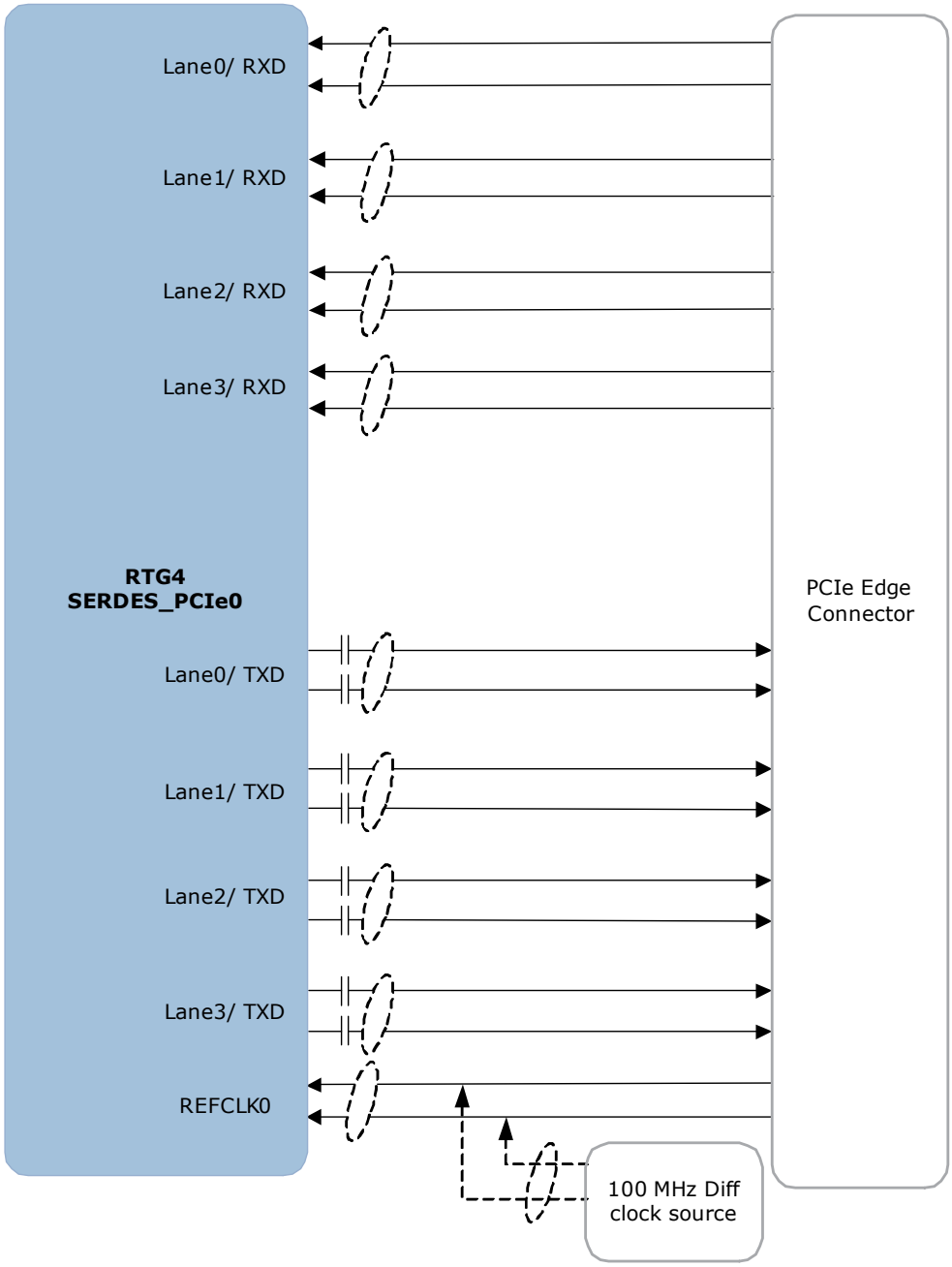
The RT4G150 FPGA device on the RTG4 Development Kit has 24 SerDes lanes. The SerDes block can be accessed using the PCIe edge connector, high-speed SMA connectors, and on-board FMC connectors.

4.4.1 SERDES PCIe0 Interface

The SERDES PCIe 0 interface (lanes 0/1/2/3) are directly routed to the PCIe connector. The reference clock is directly routed from the PCIe connector and optionally from the 100 MHz differential clock source.

The following figure shows the SERDES PCIe0 interface of the RTG4 Development Board.

Figure 7 • **SERDES_PCIe0 Interface**



TXD pairs are capacitively coupled to the RTG4 device. Series AC-coupling capacitors are used to set the common-mode voltage.

Mount R365 and R363 (remove R370 and R361) to source the clock from the100 MHz differential oscillator to the reference clock.

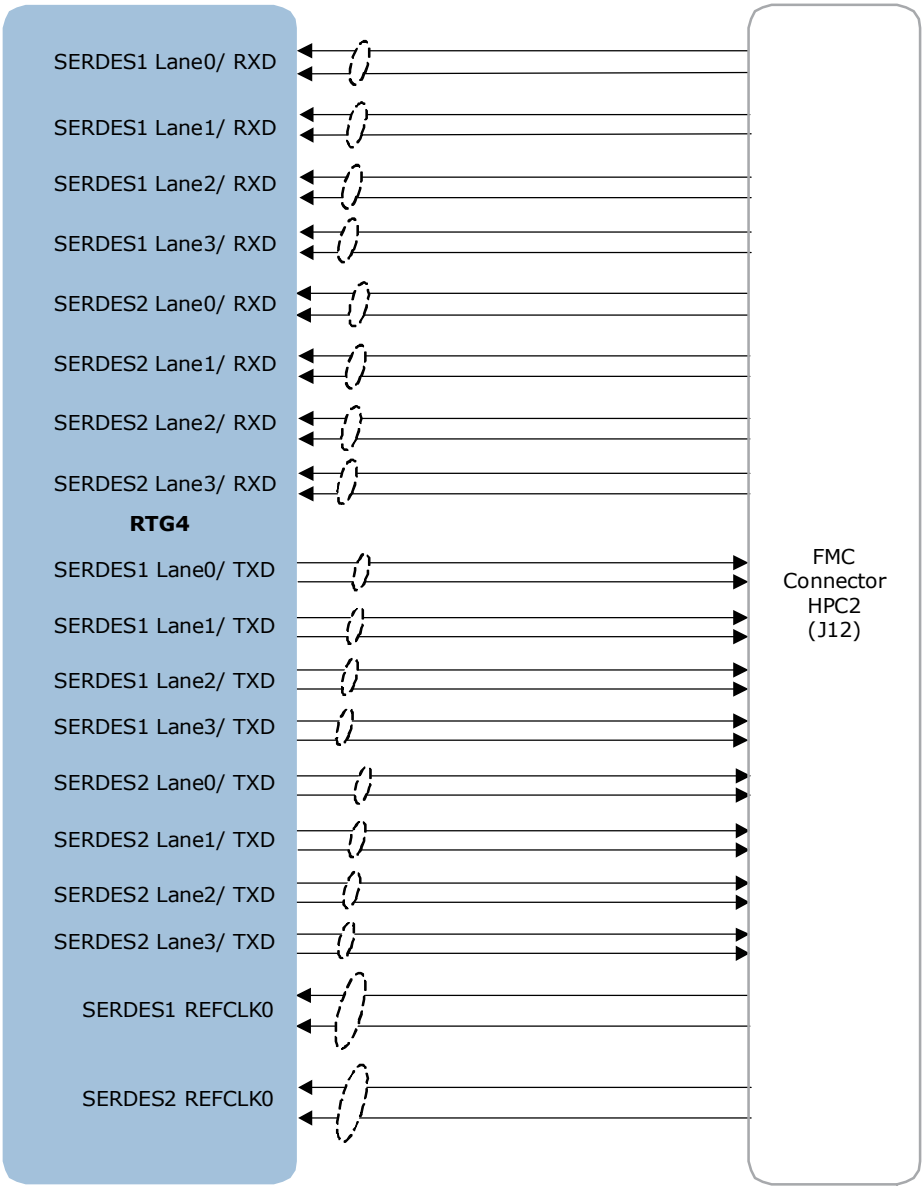
For more information, see the Board Level Schematics document (provided separately).

4.4.2 SERDES1 and SERDES2 Interfaces

The SERDES1 and SERDES2 interfaces (lanes 0/1/2/3) are routed to the FMC connector J12. Reference clocks of the SERDES1 and SERDES2 interfaces are routed from the FMC connector.

The following figure shows the SERDES1 and SERDES1 interfaces of the RTG4 Development Board.

Figure 8 • **SERDES1 and SERDES2 Interfaces**



According to the VITA-57 standard, series capacitors should be placed on the daughter board for TXD and RXD pins.

For more information, see the Board Level Schematics document (provided separately).

The following table lists the J34 pinout of the SERDES3 and SERDES4 interfaces.

Table 7 • **SERDES1 and SERDES2 Interfaces—J12 Pinout**

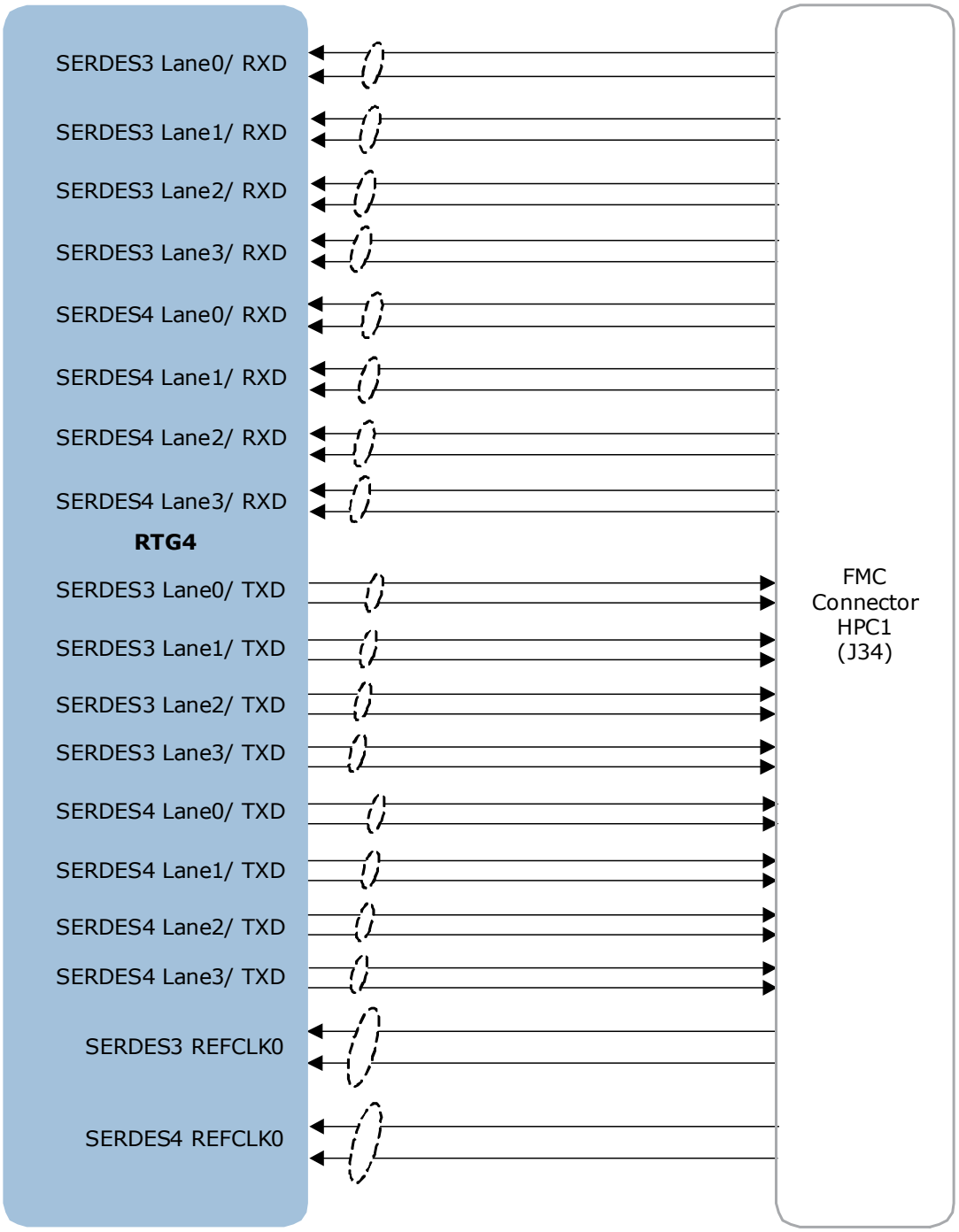
FMC Pin Number-J12	FMC Net Name	RTG4 Pin Number	RTG4 Pin Name
A2	HPC2_SERDES1_RXD1_P	AY11	SERDES_1_RXD1_P
A3	HPC2_SERDES1_RXD1_N	BA11	SERDES_1_RXD1_N
A6	HPC2_SERDES1_RXD2_P	AV12	SERDES_1_RXD2_P
A7	HPC2_SERDES1_RXD2_N	AW12	SERDES_1_RXD2_N
A10	HPC2_SERDES1_RXD3_P	AY13	SERDES_1_RXD3_P
A11	HPC2_SERDES1_RXD3_N	BA13	SERDES_1_RXD3_N
A14	HPC2_SERDES2_RXD0_P	AY15	SERDES_2_RXD0_P
A15	HPC2_SERDES2_RXD0_N	BA15	SERDES_2_RXD0_N
A18	HPC2_SERDES2_RXD1_P	AV16	SERDES_2_RXD1_P
A19	HPC2_SERDES2_RXD1_N	AW16	SERDES_2_RXD1_N
A22	HPC2_SERDES1_TXD1_P	AU11	SERDES_1_TXD1_P
A23	HPC2_SERDES1_TXD1_N	AT11	SERDES_1_TXD1_N
A26	HPC2_SERDES1_TXD2_P	AU13	SERDES_1_TXD2_P
A27	HPC2_SERDES1_TXD2_N	AT13	SERDES_1_TXD2_N
A30	HPC2_SERDES1_TXD3_P	AW14	SERDES_1_TXD3_P
A31	HPC2_SERDES1_TXD3_N	AV14	SERDES_1_TXD3_N
A34	HPC2_SERDES2_TXD0_P	AU15	SERDES_2_TXD0_P
A35	HPC2_SERDES2_TXD0_N	AT15	SERDES_2_TXD0_N
A38	HPC2_SERDES2_TXD1_P	AU17	SERDES_2_TXD1_P
A39	HPC2_SERDES2_TXD1_N	AT17	SERDES_2_TXD1_N
B12	HPC2_SERDES2_RXD3_P	AY19	SERDES_2_RXD3_P
B13	HPC2_SERDES2_RXD3_N	BA19	SERDES_2_RXD3_N
B16	HPC2_SERDES2_RXD2_P	AY17	SERDES_2_RXD2_P
B17	HPC2_SERDES2_RXD2_N	BA17	SERDES_2_RXD2_N
B20	HPC2_SERDES2_REFCLK0_P	AR16	SERDES_2_REFCLK_P
B21	HPC2_SERDES2_REFCLK0_N	AP16	SERDES_2_REFCLK_N
B32	HPC2_SERDES2_TXD3_P	AU19	SERDES_2_TXD3_P
B33	HPC2_SERDES2_TXD3_N	AT19	SERDES_2_TXD3_N
B36	HPC2_SERDES2_TXD2_P	AW18	SERDES_2_TXD2_P
B37	HPC2_SERDES2_TXD2_N	AV18	SERDES_2_TXD2_N
C2	HPC2_SERDES1_TXD0_P	AU9	SERDES_1_TXD0_P
C3	HPC2_SERDES1_TXD0_N	AT9	SERDES_1_TXD0_N
C6	HPC2_SERDES1_RXD0_P	AV10	SERDES_1_RXD0_P
C7	HPC2_SERDES1_RXD0_N	AW10	SERDES_1_RXD0_N
D4	HPC2_SERDES1_REFCLK0_P	AR12	SERDES_1_REFCLK_P
D5	HPC2_SERDES1_REFCLK0_N	AP12	SERDES_1_REFCLK_N

4.4.3 SERDES3 and SERDES4 Interfaces

The SERDES3 and SERDES4 interfaces (lanes 0/1/2/3) are routed to the FMC connector J34. Reference clocks of the SERDES3 and SERDES4 interfaces are routed from the FMC connector.

The following figure shows the SERDES3 and SERDES4 interfaces of the RTG4 Development Board.

Figure 9 • **SERDES3 and SERDES4 Interfaces**



According to the VITA-57 standard, series capacitors should be placed on the daughter board for TXD and RXD pins.

For more information, see the Board Level Schematics document (provided separately).

The following table lists the J34 pinout of the SERDES3 and SERDES4 interfaces.

Table 8 • **SERDES3 and SERDES4 Interfaces—J34 Pinout**

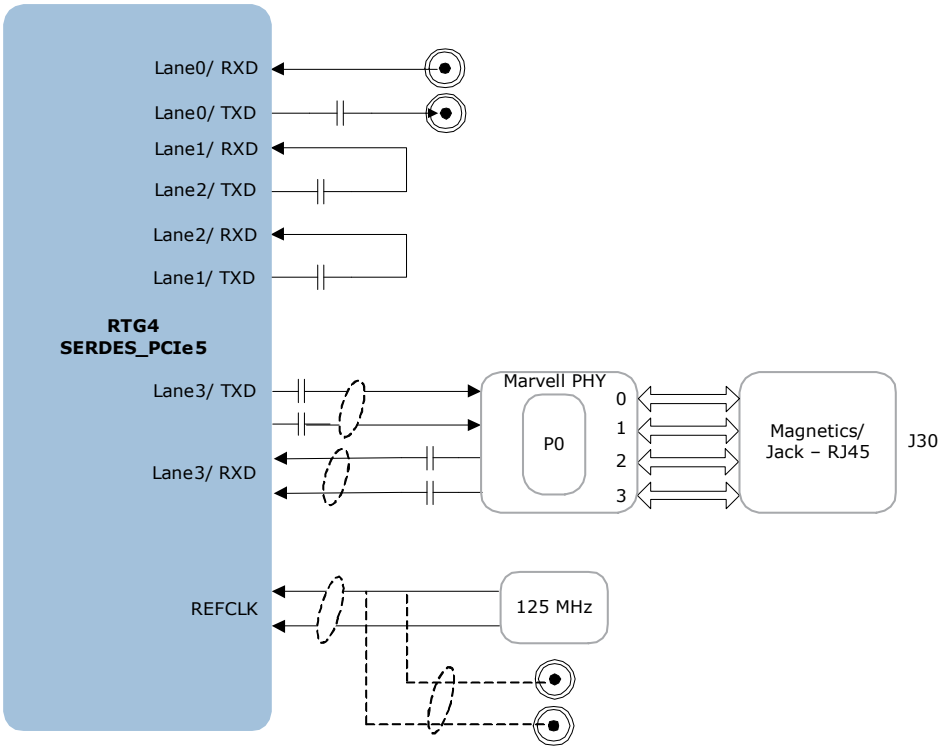
FMC Pin Number-J34	FMC Net Name	RTG4 Pin Number	RTG4 Pin Name
A2	HPC1_SERDES3_RXD1_P	BA25	SERDES_3_RXD1_P
A3	HPC1_SERDES3_RXD1_N	AY25	SERDES_3_RXD1_N
A6	HPC1_SERDES3_RXD2_P	AW26	SERDES_3_RXD2_P
A7	HPC1_SERDES3_RXD2_N	AV26	SERDES_3_RXD2_N
A10	HPC1_SERDES3_RXD3_P	BA27	SERDES_3_RXD3_P
A11	HPC1_SERDES3_RXD3_N	AY27	SERDES_3_RXD3_N
A14	HPC1_SERDES4_RXD0_P	BA29	SERDES_4_RXD0_P
A15	HPC1_SERDES4_RXD0_N	AY29	SERDES_4_RXD0_N
A18	HPC1_SERDES4_RXD1_P	AW30	SERDES_4_RXD1_P
A19	HPC1_SERDES4_RXD1_N	AV30	SERDES_4_RXD1_N
A22	HPC1_SERDES3_TXD1_P	AV24	SERDES_3_TXD1_P
A23	HPC1_SERDES3_TXD1_N	AW24	SERDES_3_TXD1_N
A26	HPC1_SERDES3_TXD2_P	AT25	SERDES_3_TXD2_P
A27	HPC1_SERDES3_TXD2_N	AU25	SERDES_3_TXD2_N
A30	HPC1_SERDES3_TXD3_P	AT27	SERDES_3_TXD3_P
A31	HPC1_SERDES3_TXD3_N	AU27	SERDES_3_TXD3_N
A34	HPC1_SERDES4_TXD0_P	AW28	SERDES_4_TXD0_N
A35	HPC1_SERDES4_TXD0_N	AV28	SERDES_4_TXD0_P
A38	HPC1_SERDES4_TXD1_P	AT29	SERDES_4_TXD1_P
A39	HPC1_SERDES4_TXD1_N	AU29	SERDES_4_TXD1_N
B12	HPC1_SERDES4_RXD3_P	AW32	SERDES_4_RXD3_P
B13	HPC1_SERDES4_RXD3_N	AV32	SERDES_4_RXD3_N
B16	HPC1_SERDES4_RXD2_P	BA31	SERDES_4_RXD2_P
B17	HPC1_SERDES4_RXD2_N	AY31	SERDES_4_RXD2_N
B20	HPC1_SERDES4_REFCLK0_P	AP30	SERDES_4_REFCLK_P
B21	HPC1_SERDES4_REFCLK0_N	AR30	SERDES_4_REFCLK_N
B32	HPC1_SERDES4_TXD3_P	AT33	SERDES_4_TXD3_P
B33	HPC1_SERDES4_TXD3_N	AU33	SERDES_4_TXD3_N
B36	HPC1_SERDES4_TXD2_P	AT31	SERDES_4_TXD2_P
B37	HPC1_SERDES4_TXD2_N	AU31	SERDES_4_TXD2_N
C2	HPC1_SERDES3_TXD0_P	AT23	SERDES_3_TXD0_P
C3	HPC1_SERDES3_TXD0_N	AU23	SERDES_3_TXD0_N
C6	HPC1_SERDES3_RXD0_P	BA23	SERDES_3_RXD0_P
C7	HPC1_SERDES3_RXD0_N	AY23	SERDES_3_RXD0_N
D4	HPC1_SERDES3_REFCLK0_P	AP26	SERDES_3_REFCLK_P
D5	HPC1_SERDES3_REFCLK0_N	AR26	SERDES_3_REFCLK_N

4.4.4 SERDES PCIe5 Interface

Lane 0 is connected to the SMA connectors, Lane 1 (RXD) is connected to Lane 2 (TXD), Lane 2 (RXD) is connected to Lane 1 (TXD), and Lane 3 (TXD and RXD) is connected to the Marvell PHY device of Port 0. The reference clock is connected from the 125 MHz differential clock oscillator and optionally connected from the SMA connectors.

The following figure shows the SERDES PCIe5 interface of the RTG4 Development Board.

Figure 10 • **SERDES_PCIe5 Interface**



For more information, see the Board Level Schematics document (provided separately).

4.5 Marvell PHY (88E1340S)

The RTG4 Development Kit uses the on-board Marvell Alaska PHY device (88E1340S) for Ethernet communications at 100 Mbps or 1000 Mbps. The 88E1340S device has four independent gigabit Ethernet transceivers, but the board uses only one transceiver. The transceiver performs all the physical layer functions for 100BASE-TX and 1000BASE-T full- or half-duplex Ethernet on a CAT5 twisted-pair cable. The PHY device is connected to a user-provided Ethernet cable through an RJ45 connector with built-in magnetics.

The 88E1340S device supports the quad SGMII for direct connection to a RTG4 chip (see Figure 11, page 19).

It is configured through the CONFIG [3:0] and CLK_SEL [1:0] pins.

The CLK_SEL [1:0] pin is used to select the reference clock input option. On the board, the status of the CLK_SEL0 and CLK_SEL1 pins is high. REF_CLK is a 25 MHz reference differential clock input (Y3). It consists of LVDS differential inputs with a 100 Ω differential internal termination resistor.

- RCLK—Gigabit recovered clock
- SCLK—25 MHz synchronous input reference clock

Expected reference clock (REF_CLK) specifications:

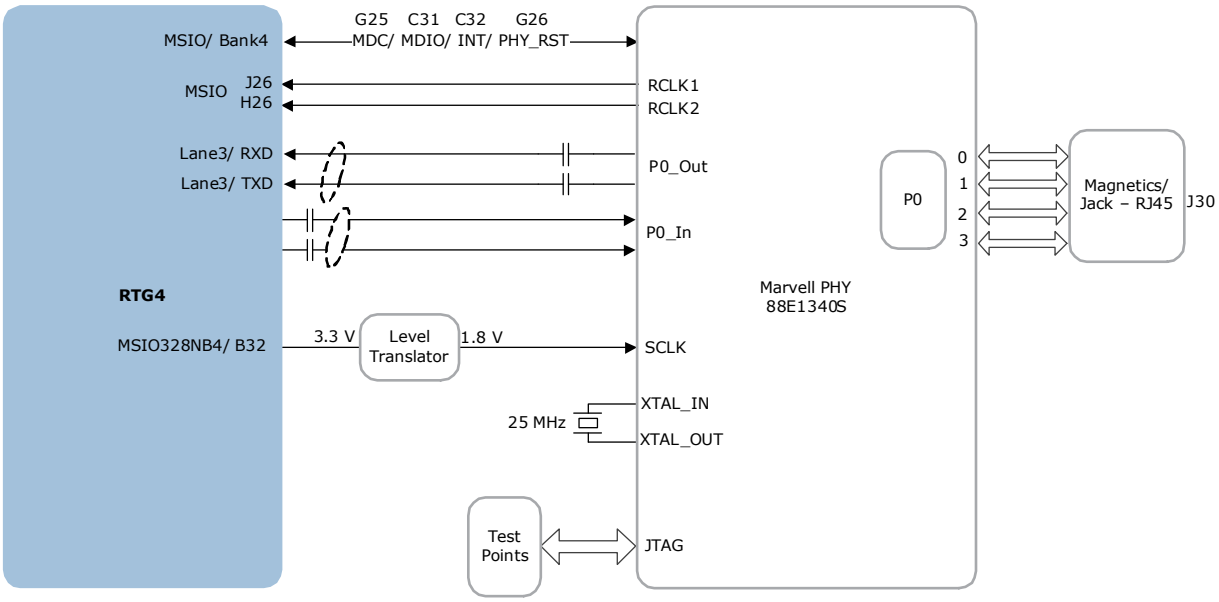
- Voltage level: 3.3 (± 0.3) V
- Differential LVDS

- Symmetry: 50% (± 10%)
- Rise/Fall Time: 1 ns Max—20% to 80% of supply (3.3 V)
- Output Voltage Levels: 0 = 0.90 minimum, 1.10 typical and 1 = 1.43 typical, 1.60 maximum

- Differential Output Voltage: 247 mV minimum, 454 mV maximum

The following figure shows the RTG4 Marvell PHY interface.

Figure 11 • **RTG4 Marvell PHY Interface**



For more information, see the Board Level Schematics document (provided separately).

4.6 Programming

RTG4 FPGAs support multiple programming interfaces and can address a wide range of platform requirements. An RTG4 device can be programmed through the JTAG and SPI interfaces.

The dedicated programming SPI port can operate in SPI slave mode.

For more information about SPI programming, see *RTG4 Programming Guide*.

The following figure shows the programming interface of the RTG4 Development Board.

Figure 12 • **Programming Interface**

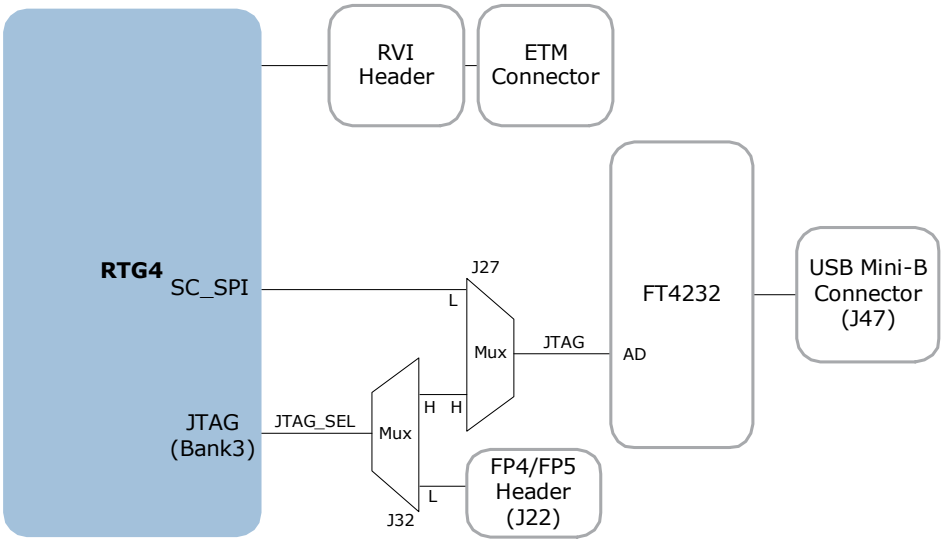


Table 9 • **Programming Jumper Selection**

J27	J32	Description
X	L	FP4 JTAG programming (Connect Programmer to J22 header)
H	H	FTDI JTAG programming
L	X	FTDI SPI slave programming

JTAG/FTDI programming (J32): JTAG_SEL is used to switch between embedded FlashPro5 FTDI JTAG programming (high) and external FlashPro4 JTAG programming (low). JTAG_SEL can be enabled through the JTAG_SEL_FTDI signal from the FTDI chip (short pins 2-4 in J32).

FTDI JTAG/SPI slave programming: Jumper J27 is used to switch between FTDI JTAG (high) and FTDI SPI slave programming (low).

RVI header: A 10 × 2 RVI header is provided on the board for debugging. This header allows plugging in the Keil ULINK debugger or IAR J-Link debugger to easily debug or configure the Cortex-M3 processor during board power-up.

FlashPro4 programming header (J22): The RTG4 device on this Development Kit can be programmed using a FlashPro4 programmer. In addition, SoftConsole uses FlashPro4 for software debugging.

For more information, see the Board Level Schematics document (provided separately).

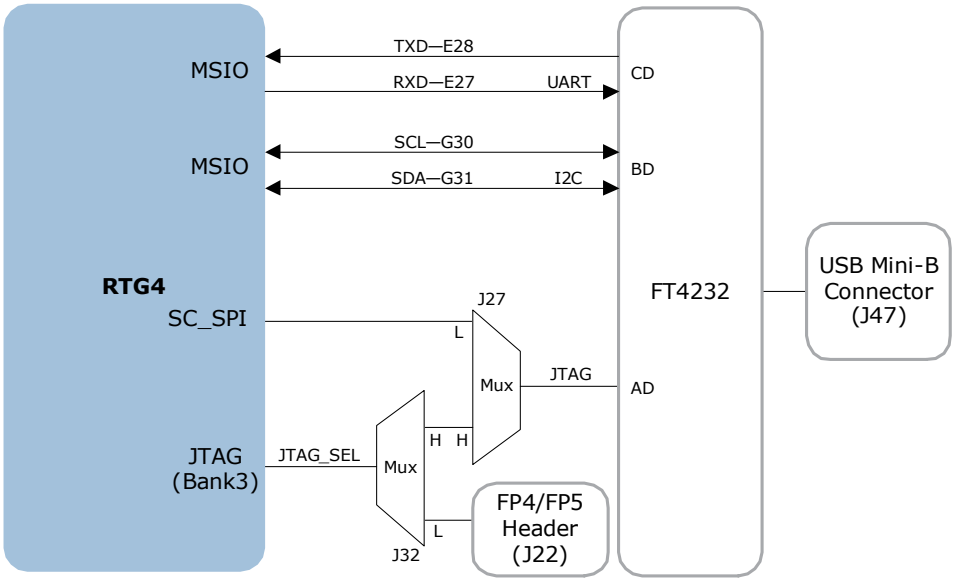
4.7 FTDI Interface

The FT4232H chip is a USB 2.0 high-speed (480 Mbps) to UART/MPSSE interface with the following key features:

- Single-chip USB-to-quad serial ports in various configurations
- Entire USB protocol handled on the chip without requiring USB-specific firmware programming
- USB 2.0 high-speed (480 Mbps) and full-speed (12 Mbps) compatibility
- Two MPSSEs on channel A and channel B to simplify synchronous serial protocol (USB to JTAG, I^2C, SPI, or bit-bang) design
- Fully assisted hardware handshaking and X-On or X-Off software handshaking
- +1.8 V (chip core) and +3.3 V I/O interfacing with +5 V tolerance

The following figure shows the FTDI interface of the RTG4 Development Board.

Figure 13 • **FTDI Interface**



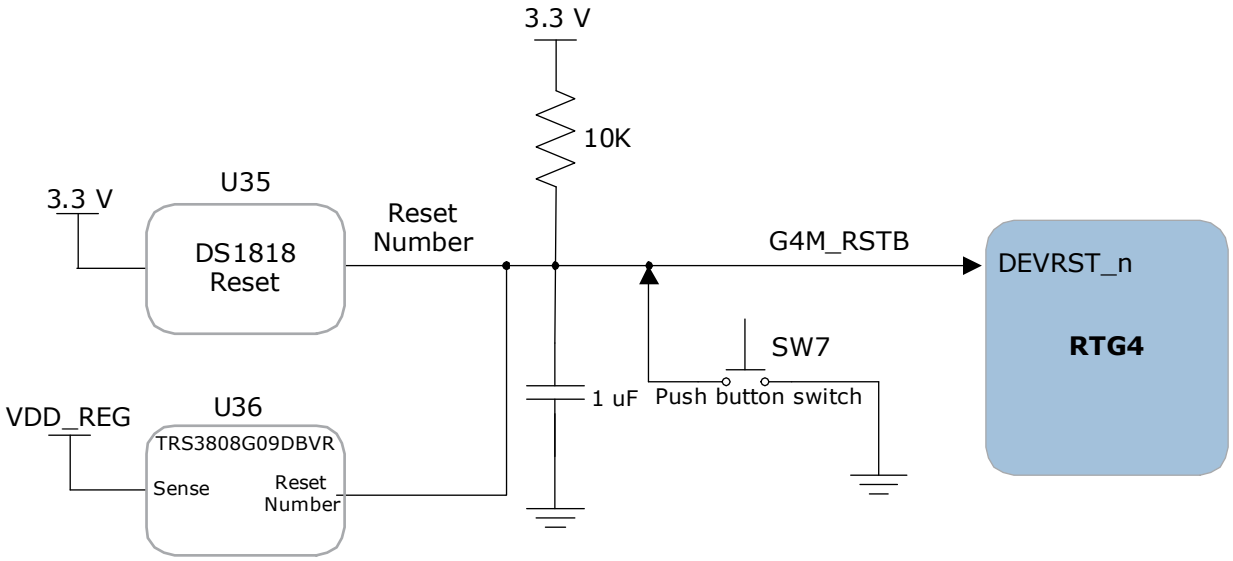
4.8 System Reset

The M2S_RSTB signal (active-low) is generated by the SW7 push-button switch, U35 chip (DS1818), or U22 chip (TPS3808G09). DEVRST_N is an input-only reset pad that allows assertion of a full reset to the chip at any time.

DS1818 maintains reset until 150 ms after the 3.3 V supply returns to intolerance. The TPS3808G09DBVR device monitors the voltage at the VDD_REG terminal. If the voltage at this terminal sense-drops below the threshold voltage of 0.9 V, the G4M_RSTB signal is asserted.

The following figure shows the system reset interface of the RTG4 Development Board.

Figure 14 • **System Reset Interface**



For more information, see the Board Level Schematics document (provided separately).

4.9 Clock Oscillator

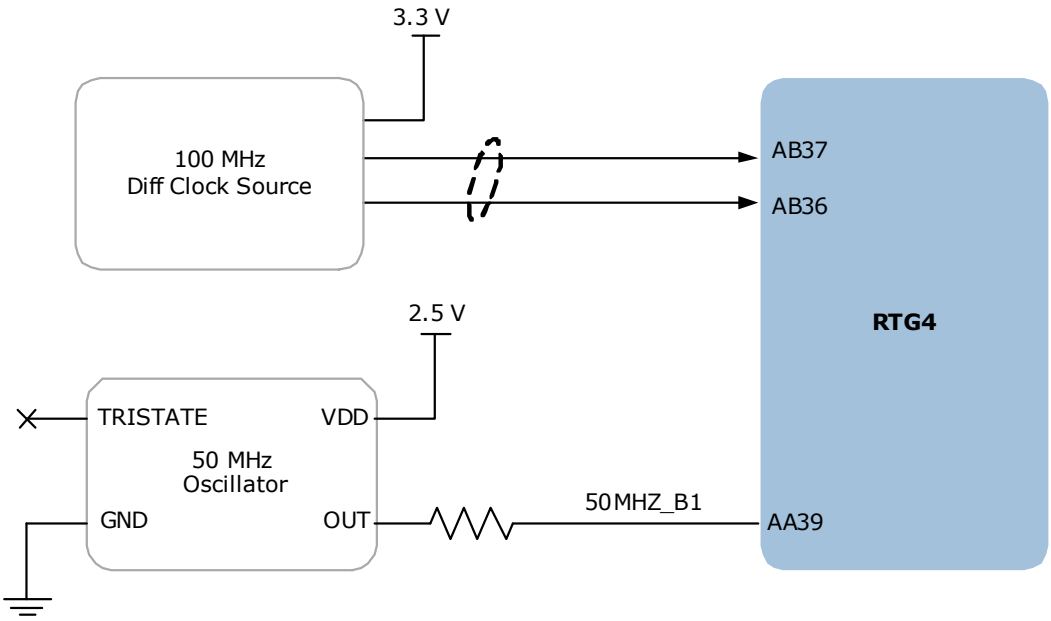
A 50 MHz clock oscillator (LVCMOS) with an accuracy of ±50 ppm is available on the board, as listed in the following table and shown in the following figure. This clock oscillator is connected to the FPGA fabric to provide a system reference clock.

An on-chip RTG4 PLL can be configured to generate a wide range of high-precision clock frequencies.

Table 10 • **50 MHz Clock**

RTG4 Development Kit Pin	RTG4 Package Pin Number	RTG4 Device Pin Name
50MHZ_B1	AA39	MSIOD73PB1/GB12_23/CCC_NE0_CLKI2

Figure 15 • **50 MHz and 100 MHz Clock Oscillators**



A 100 MHz LVDS clock oscillator operating at 3.3 V with an accuracy of ±50 ppm is available on the board, as shown in the previous figure and listed in the following table. This clock oscillator is connected to the FPGA fabric AB37 and AB36 pins.

Note: Both clock sources drive the same CCC_NE0. To use both clock sources at a time and avoid a compile error, configure one CCC pin as fabric input and use regular routing resources for the clock signal.

Table 11 • **100 MHz Clock**

RTG4 Development Kit Pin	RTG4 Package Pin Number	RTG4 Device Pin Name
OSC_100MHZ_P_B1	AB37	MSIOD74PB1/GB12_23/CCC_NE0_CLKI3
OSC_100MHZ_N_B1	AB36	MSIOD74NB1

For more information, see the Board Level Schematics document (provided separately).

4.10 User Interface

The RTG4 Development Board has user LEDs as well as push-button switches.

4.10.1 User LEDs

The board has eight-active high LEDs connected to the RTG4 device that can be used to debug applications. The following table lists the on-board user LEDs.

Table 12 • **LEDs**

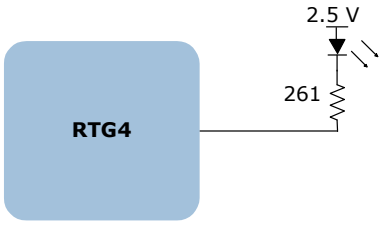
RTG4 Development Kit Pin	RTG4 Package Pin Number	RTG4 Device Pin Name
LED1	W35	MSIOD62PB1
LED2	W34	MSIOD46PB1
LED3	V30	MSIOD47PB1
LED4	W33	MSIOD46NB1

Table 12 • **LEDs *(continued)***

RTG4 Development Kit Pin	RTG4 Package Pin Number	RTG4 Device Pin Name
LED5	T33	MSIOD38PB1
LED6	U35	MSIOD41NB1
LED7	R36	MSIOD37PB1
LED8	T34	MSIOD38NB1

The following figure shows the LED interface of the RTG4 Development Board.

Figure 16 • **LED Interface**



For more information, see the Board Level Schematics document (provided separately).

4.10.2 Push-Button Switches

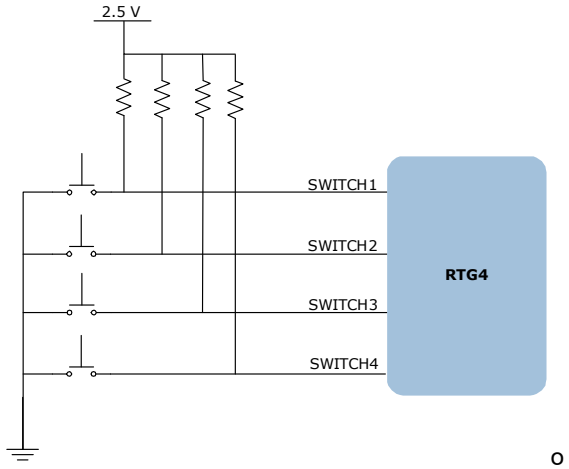
The RTG4 Development Kit comes with five push-button tactile switches connected to the RTG4 device. The following table lists the on-board push-button switches.

Table 13 • **Push-Button Switches**

RTG4 Development Kit Pin	RTG4 Package Pin Number	RTG4 Device Pin Name
SW1	AA30	MSIOD68NB1
SW2	AB31	MSIOD65PB1
SW3	AB30	MSIOD68PB1
SW4	AB32	MSIOD65NB1
SW7	J33	DEVRST_n

The following figure shows the switches interface of the RTG4 Development Board.

Figure 17 • **Switches Interface**



For more information, see the Board Level Schematics document (provided separately).

4.10.3 Slide Switches - DPDT

The **SW6** switch powers the device ON or OFF switch from the +12 V external DC jack (J9).

4.10.4 DIP Switch - SPST

The **SW5** DIP switch has eight connections to the RTG4 device.

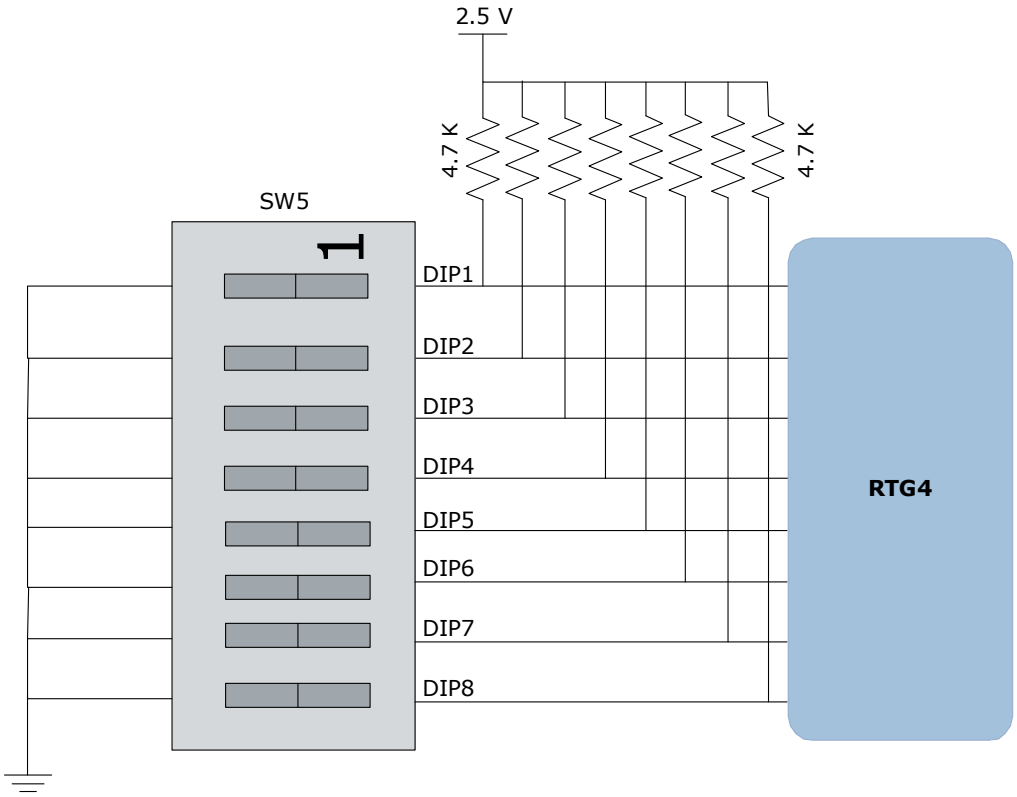
The following table lists the on-board DIP switches.

Table 14 • **DIP Switches**

RTG4 Development Kit Pin	RTG4 Package Pin Number	RTG4 Device Pin Name
SW1	AA30	MSIOD68NB1
DIP1	AA33	MSIOD57NB1
DIP2	Y31	MSIOD56PB1
DIP3	W31	MSIOD56NB1
DIP4	W30	MSIOD47NB1
DIP5	V33	MSIOD42NB1
DIP6	V34	MSIOD42PB1
DIP7	U34	MSIOD41PB1
DIP8	W36	MSIOD69PB1

The following figure shows the SPST interface of the RTG4 Development Board.

Figure 18 • **SPST Interface**



For more information, see the Board Level Schematics document (provided separately).

4.10.5 FMC Connectors

The RTG4 Development Kit has two HPC (J34 and J12) FMC connectors on the board for connecting the daughter cards to enable future expansion of interfaces. These FMC connectors are compliant with the VITA 57.1 specification.

4.10.5.1 FMC Connector J34

The RTG4 MSIO, MSIOD, Spacewire, CCC, SERDES3, and SERDES4 signals are routed to the J34 FMC connector for application development.

The following table provides the J34 FMC pinout details.

Table 15 • **J34 FMC Connector Pinout**

FMC Pin Number-J34	FMC Net Name	RTG4 Pin Number	RTG4 Pin Name
A2	HPC1_SERDES3_RXD1_P	BA25	SERDES_3_RXD1_P
A3	HPC1_SERDES3_RXD1_N	AY25	SERDES_3_RXD1_N
A6	HPC1_SERDES3_RXD2_P	AW26	SERDES_3_RXD2_P
A7	HPC1_SERDES3_RXD2_N	AV26	SERDES_3_RXD2_N
A10	HPC1_SERDES3_RXD3_P	BA27	SERDES_3_RXD3_P
A11	HPC1_SERDES3_RXD3_N	AY27	SERDES_3_RXD3_N
A14	HPC1_SERDES4_RXD0_P	BA29	SERDES_4_RXD0_P
A15	HPC1_SERDES4_RXD0_N	AY29	SERDES_4_RXD0_N
A18	HPC1_SERDES4_RXD1_P	AW30	SERDES_4_RXD1_P
A19	HPC1_SERDES4_RXD1_N	AV30	SERDES_4_RXD1_N
A22	HPC1_SERDES3_TXD1_P	AV24	SERDES_3_TXD1_P
A23	HPC1_SERDES3_TXD1_N	AW24	SERDES_3_TXD1_N
A26	HPC1_SERDES3_TXD2_P	AT25	SERDES_3_TXD2_P
A27	HPC1_SERDES3_TXD2_N	AU25	SERDES_3_TXD2_N
A30	HPC1_SERDES3_TXD3_P	AT27	SERDES_3_TXD3_P
A31	HPC1_SERDES3_TXD3_N	AU27	SERDES_3_TXD3_N
A34	HPC1_SERDES4_TXD0_P	AV28	SERDES_4_TXD0_P
A35	HPC1_SERDES4_TXD0_N	AW28	SERDES_4_TXD0_N
A38	HPC1_SERDES4_TXD1_P	AT29	SERDES_4_TXD1_P
A39	HPC1_SERDES4_TXD1_N	AU29	SERDES_4_TXD1_N
B1	HPC1_CLK_DIR_B4	D34	MSIO349PB4
B12	HPC1_SERDES4_RXD3_P	AW32	SERDES_4_RXD3_P
B13	HPC1_SERDES4_RXD3_N	AV32	SERDES_4_RXD3_N
B16	HPC1_SERDES4_RXD2_P	BA31	SERDES_4_RXD2_P
B17	HPC1_SERDES4_RXD2_N	AY31	SERDES_4_RXD2_N
B20	HPC1_SERDES4_REFCLK0_P	AP30	SERDES_4_REFCLK_P
B21	HPC1_SERDES4_REFCLK0_N	AR30	SERDES_4_REFCLK_N
B32	HPC1_SERDES4_TXD3_P	AT33	SERDES_4_TXD3_P
B33	HPC1_SERDES4_TXD3_N	AU33	SERDES_4_TXD3_N

Table 15 • **J34 FMC Connector Pinout *(continued)***

FMC Pin Number-J34	FMC Net Name	RTG4 Pin Number	RTG4 Pin Name
B36	HPC1_SERDES4_TXD2_P	AT31	SERDES_4_TXD2_P
B37	HPC1_SERDES4_TXD2_N	AU31	SERDES_4_TXD2_N
C2	HPC1_SERDES3_TXD0_P	AT23	SERDES_3_TXD0_P
C3	HPC1_SERDES3_TXD0_N	AU23	SERDES_3_TXD0_N
C6	HPC1_SERDES3_RXD0_P	BA23	SERDES_3_RXD0_P
C7	HPC1_SERDES3_RXD0_N	AY23	SERDES_3_RXD0_N
C10	HPC1_LA06_P_B6	H11	MSIO248PB6
C11	HPC1_LA06_N_B6	J11	MSIO248NB6
C14	HPC1_LA10_P_B6	H13	MSIO263PB6
C15	HPC1_LA10_N_B6	H14	MSIO263NB6
C18	HPC1_LA14_P_B6	G12	MSIO262PB6
C19	HPC1_LA14_N_B6	G13	MSIO262NB6
C22	HPC1_LA18_CC_P_B6	C10	MSIO265PB6/GB5/CCC_SW1_CLKI2/SPWR_SW1_1_RX_STROBE_P
C23	HPC1_LA18_CC_N_B6	C11	MSIO265NB6/SPWR_SW1_1_RX_STROBE_N
C26	HPC1_LA27_P_B6	A7	MSIO261PB6
C27	HPC1_LA27_N_B6	A8	MSIO261NB6
C30	HPC1_SCL	K28	MSIO344PB4
C31	HPC1_SDA	K27	MSIO344NB4
C34	HPC1_GA0	A29	MSIO319PB5
D1	HPC1_PG_C2M	A1	PG
D4	HPC1_SERDES3_REFCLK0_P	AP26	SERDES_3_REFCLK_P
D5	HPC1_SERDES3_REFCLK0_N	AR26	SERDES_3_REFCLK_N
D8	HPC1_LA01_CC_P_B6	K15	MSIO266PB6/GB7/CCC_SW1_CLKI3/SPWR_SW1_1_RX_DATA_P
D9	HPC1_LA01_CC_N_B6	K14	MSIO266NB6/SPWR_SW1_1_RX_DATA_N
D11	HPC1_LA05_P_B6	J12	MSIO251PB6
D12	HPC1_LA05_N_B6	K12	MSIO251NB6
D14	HPC1_LA09_P_B6	J16	MSIO272PB6
D15	HPC1_LA09_N_B6	K16	MSIO272NB6
D17	HPC1_LA13_P_B6	F13	MSIO267PB6
D18	HPC1_LA13_N_B6	F14	MSIO267NB6
D20	HPC1_LA17_CC_P_B6	E6	MSIO253PB6/GB1/CCC_SW0_CLKI2/SPWR_SW0_1_RX_STROBE_P

Table 15 • **J34 FMC Connector Pinout *(continued)***

FMC Pin Number-J34	FMC Net Name	RTG4 Pin Number	RTG4 Pin Name
D21	HPC1_LA17_CC_N_B6	E7	MSIO253NB6/SPWR_SW0_1_ RX_STROBE_N
D23	HPC1_LA23_P_B6	A9	MSIO274PB6
D24	HPC1_LA23_N_B6	A10	MSIO274NB6
D26	HPC1_LA26_P_B6	B7	MSIO252PB6
D27	HPC1_LA26_N_B6	B8	MSIO252NB6
D35	HPC1_GA1	A30	MSIO319NB5
E2	HPC1_HA01_CC_P_B5	E19	MSIO293PB5/GB11/GRESET
E3	HPC1_HA01_CC_N_B5	F19	MSIO293NB5
E6	HPC1_HA05_P_B5	J18	MSIO290PB5
E7	HPC1_HA05_N_B5	K19	MSIO290NB5
E9	HPC1_HA09_P_B5	F17	MSIO287PB5
E10	HPC1_HA09_N_B5	F18	MSIO287NB5
E12	HPC1_HA13_P_B5	C20	MSIO295PB5
E13	HPC1_HA13_N_B5	C21	MSIO295NB5
E15	HPC1_HA16_P_B5	D18	MSIO289PB5
E16	HPC1_HA16_N_B5	C18	MSIO289NB5
E18	HPC1_HA20_P_B5	B15	MSIO286PB5
E19	HPC1_HA20_N_B5	B16	MSIO286NB5
E21	HPC1_HB03_P_B2	M31	MSIOD9PB2
E22	HPC1_HB03_N_B2	L30	MSIOD9NB2
E24	HPC1_HB05_P_B2	H39	MSIOD19PB2
E25	HPC1_HB05_N_B2	J39	MSIOD19NB2
E27	HPC1_HB09_P_B2	E40	MSIOD7PB2
E28	HPC1_HB09_N_B2	E41	MSIOD7NB2
E30	HPC1_HB13_P_B2	D38	MSIOD10PB2
E31	HPC1_HB13_N_B2	D39	MSIOD10NB2
E33	HPC1_HB19_P_B2	G36	MSIOD8PB2
E34	HPC1_HB19_N_B2	H36	MSIOD8NB2
E36	HPC1_HB21_P_B2	J36	MSIOD17PB2
E37	HPC1_HB21_N_B2	K36	MSIOD17NB2
E39	VCCIO_HPC1_VADJ		
F1	HPC1_PG_M2C	J31	MSIO356PB4
F4	HPC1_HA00_CC_P_B5	A17	MSIO292PB5/GB9/GRESET
F5	HPC1_HA00_CC_N_B5	A18	MSIO292NB5
F7	HPC1_HA04_P_B5	J19	MSIO296PB5
F8	HPC1_HA04_N_B5	H19	MSIO296NB5
F10	HPC1_HA08_P_B5	E20	MSIO299PB5

Table 15 • **J34 FMC Connector Pinout *(continued)***

FMC Pin Number-J34	FMC Net Name	RTG4 Pin Number	RTG4 Pin Name
F11	HPC1_HA08_N_B5	F20	MSIO299NB5
F13	HPC1_HA12_P_B5	D19	MSIO294PB5
F14	HPC1_HA12_N_B5	C19	MSIO294NB5
F16	HPC1_HA15_P_B5	B17	MSIO291PB5
F17	HPC1_HA15_N_B5	B18	MSIO291NB5
F19	HPC1_HA19_P_B5	C13	MSIO277PB5
F20	HPC1_HA19_N_B5	C14	MSIO277NB5
F22	HPC1_HB02_P_B2	K35	MSIOD11PB2
F23	HPC1_HB02_N_B2	L35	MSIOD11NB2
F25	HPC1_HB04_P_B2	G39	MSIOD13PB2/GB12_23/CCC_SE1_CLKI0/SPWR_SE1_0_RX_STROBE_P
F26	HPC1_HB04_N_B2	G40	MSIOD13NB2/SPWR_SE1_0_RX_STROBE_N
F28	HPC1_HB08_P_B2	D40	MSIOD3PB2
F29	HPC1_HB08_N_B2	D41	MSIOD3NB2
F31	HPC1_HB12_P_B2	E37	MSIOD1PB2
F32	HPC1_HB12_N_B2	F37	MSIOD1NB2
F34	HPC1_HB16_P_B2	J34	MSIOD16PB2
F35	HPC1_HB16_N_B2	J35	MSIOD16NB2
F37	HPC1_HB20_P_B2	L32	MSIOD2PB2
F38	HPC1_HB20_N_B2	K32	MSIOD2NB2
F40	VCCIO_HPC1_VADJ		
G2	HPC1_CLK1_M2C_P_B4	F28	MSIO334PB4/GB17/CCC_SE0_CLKI2/SPWR_SE0_1_RX_STROBE_P
G3	HPC1_CLK1_M2C_N_B4	F29	MSIO334NB4/SPWR_SE0_1_RX_STROBE_N
G6	HPC1_LA00_CC_P_B6	H10	MSIO254PB6/GB3/CCC_SW0_CLKI3/SPWR_SW0_1_RX_DATA_P
G7	HPC1_LA00_CC_N_B6	J9	MSIO254NB6/SPWR_SW0_1_RX_DATA_N
G9	HPC1_LA03_P_B6	K10	MSIO242PB6
G10	HPC1_LA03_N_B6	K11	MSIO242NB6
G12	HPC1_LA08_P_B6	J14	MSIO260PB6
G13	HPC1_LA08_N_B6	J13	MSIO260NB6
G15	HPC1_LA12_P_B6	F15	MSIO269PB6
G16	HPC1_LA12_N_B6	G15	MSIO269NB6
G18	HPC1_LA16_P_B6	D11	MSIO268PB6

Table 15 • **J34 FMC Connector Pinout *(continued)***

FMC Pin Number-J34	FMC Net Name	RTG4 Pin Number	RTG4 Pin Name
G19	HPC1_LA16_N_B6	D12	MSIO268NB6
G21	HPC1_LA20_P_B6	B10	MSIO270PB6
G22	HPC1_LA20_N_B6	B11	MSIO270NB6
G24	HPC1_LA22_P_B6	B5	MSIO255PB6
G25	HPC1_LA22_N_B6	B6	MSIO255NB6
G27	HPC1_LA25_P_B6	D6	MSIO246PB6
G28	HPC1_LA25_N_B6	C6	MSIO246NB6
G30	HPC1_LA29_P_B6	C3	MSIO243PB6
G31	HPC1_LA29_N_B6	B3	MSIO243NB6
G33	HPC1_LA31_P_B6	E10	MSIO264PB6
G34	HPC1_LA31_N_B6	E11	MSIO264NB6
G36	HPC1_LA33_P_B6	F12	MSIO271PB6
G37	HPC1_LA33_N_B6	E12	MSIO271NB6
H2	HPC1_PRSNT_M2CL	F34	MSIO357PB4
H4	HPC1_CLK0_M2C_P_B4	F27	MSIO335PB4/GB19/CCC_SE0_CLKI3/SPWR_SE0_1_RX_DATA_P
H5	HPC1_CLK0_M2C_N_B4	G27	MSIO335NB4/SPWR_SE0_1_RX_DATA_N
H7	HPC1_LA02_P_B6	H8	MSIO245PB6
H8	HPC1_LA02_N_B6	H9	MSIO245NB6
H10	HPC1_LA04_P_B6	F9	MSIO258PB6
H11	HPC1_LA04_N_B6	F10	MSIO258NB6
H13	HPC1_LA07_P_B6	G10	MSIO257PB6
H14	HPC1_LA07_N_B6	G11	MSIO257NB6
H16	HPC1_LA11_P_B6	D13	MSIO273PB6
H17	HPC1_LA11_N_B6	D14	MSIO273NB6
H19	HPC1_LA15_P_B6	E9	MSIO259PB6
H20	HPC1_LA15_N_B6	D9	MSIO259NB6
H22	HPC1_LA19_P_B6	C8	MSIO256PB6
H23	HPC1_LA19_N_B6	C9	MSIO256NB6
H25	HPC1_LA21_P_B6	A4	MSIO247PB6
H26	HPC1_LA21_N_B6	A5	MSIO247NB6
H28	HPC1_LA24_P_B6	D7	MSIO250PB6
H29	HPC1_LA24_N_B6	D8	MSIO250NB6
H31	HPC1_LA28_P_B6	C4	MSIO241PB6
H32	HPC1_LA28_N_B6	C5	MSIO241NB6
H34	HPC1_LA30_P_B6	F7	MSIO249PB6

Table 15 • **J34 FMC Connector Pinout *(continued)***

FMC Pin Number-J34	FMC Net Name	RTG4 Pin Number	RTG4 Pin Name
H35	HPC1_LA30_N_B6	F8	MSIO249NB6
H37	HPC1_LA32_P_B6	G7	MSIO244PB6
H38	HPC1_LA32_N_B6	G8	MSIO244NB6
H40	VCCIO_HPC1_VADJ		
J2	HPC1_CLK3_BIDIR_P_B4	G29	MSIO347PB4/GB23/CCC_SE1_CLKI3/SPWR_SE1_1_RX_DATA_P
J3	HPC1_CLK3_BIDIR_N_B4	H29	MSIO347NB4/SPWR_SE1_1_RX_DATA_N
J6	HPC1_HA03_P_B5	G16	MSIO281PB5
J7	HPC1_HA03_N_B5	G17	MSIO281NB5
J9	HPC1_HA07_P_B5	J17	MSIO278PB5
J10	HPC1_HA07_N_B5	K17	MSIO278NB5
J12	HPC1_HA11_P_B5	D21	MSIO298PB5
J13	HPC1_HA11_N_B5	E21	MSIO298NB5
J15	HPC1_HA14_P_B5	D16	MSIO285PB5
J16	HPC1_HA14_N_B5	D17	MSIO285NB5
J18	HPC1_HA18_P_B5	A14	MSIO288PB5
J19	HPC1_HA18_N_B5	A15	MSIO288NB5
J21	HPC1_HA22_P_B5	B12	MSIO279PB5
J22	HPC1_HA22_N_B5	B13	MSIO279NB5
J24	HPC1_HB01_P_B2	P31	MSIOD20PB2
J25	HPC1_HB01_N_B2	N31	MSIOD20NB2
J27	HPC1_HB07_P_B2	P33	MSIOD21PB2
J28	HPC1_HB07_N_B2	N33	MSIOD21NB2
J30	HPC1_HB11_P_B2	F38	MSIOD18PB2
J31	HPC1_HB11_N_B2	E38	MSIOD18NB2
J33	HPC1_HB15_P_B2	G37	MSIOD6PB2
J34	HPC1_HB15_N_B2	H37	MSIOD6NB2
J36	HPC1_HB18_P_B2	M30	MSIOD5PB2
J37	HPC1_HB18_N_B2	N30	MSIOD5NB2
J39	VCCIO_HPC1_VIO_B_M2C_FMC	C40	VDDI2_1
K1	VCCIO_HPC1_VIO_B_M2C_FMC	C40	VDDI2_1
K4	HPC1_CLK2_BIDIR_P_B4	D33	MSIO346PB4/GB21/CCC_SE1_CLKI2/SPWR_SE1_1_RX_STROBE_P
K5	HPC1_CLK2_BIDIR_N_B4	E33	MSIO346NB4/SPWR_SE1_1_RX_STROBE_N
K7	HPC1_HA02_P_B5	E16	MSIO280PB5

Table 15 • **J34 FMC Connector Pinout *(continued)***

FMC Pin Number-J34	FMC Net Name	RTG4 Pin Number	RTG4 Pin Name
K8	HPC1_HA02_N_B5	E17	MSIO280NB5
K10	HPC1_HA06_P_B5	G18	MSIO284PB5
K11	HPC1_HA06_N_B5	H18	MSIO284NB5
K13	HPC1_HA10_P_B5	A19	MSIO297PB5
K14	HPC1_HA10_N_B5	A20	MSIO297NB5
K16	HPC1_HA17_CC_P_B5	B20	MSIO301PB5
K17	HPC1_HA17_CC_N_B5	B21	MSIO301NB5
K19	HPC1_HA21_P_B5	A12	MSIO283PB5
K20	HPC1_HA21_N_B5	A13	MSIO283NB5
K22	HPC1_HA23_P_B5	C15	MSIO282PB5
K23	HPC1_HA23_N_B5	C16	MSIO282NB5
K25	HPC1_HB00_CC_P_B2	N34	MSIOD23PB2/GB12_23/CCC_SE0_CLKI1/SPWR_SE0_0_RX_DATA_P
K26	HPC1_HB00_CC_N_B2	P34	MSIOD23NB2/SPWR_SE0_0_RX_DATA_N
K28	HPC1_HB06_CC_P_B2	N32	MSIOD14PB2/GB12_23/CCC_SE1_CLKI1/SPWR_SE1_0_RX_DATA_P
K29	HPC1_HB06_CC_N_B2	M32	MSIOD14NB2/SPWR_SE1_0_RX_DATA_N
K31	HPC1_HB10_P_B2	F39	MSIOD12PB2
K32	HPC1_HB10_N_B2	F40	MSIOD12NB2
K34	HPC1_HB14_P_B2	L33	MSIOD4PB2
K35	HPC1_HB14_N_B2	K33	MSIOD4NB2
K37	HPC1_HB17_CC_P_B2	K37	MSIOD22PB2/GB12_23/CCC_SE0_CLKI0/SPWR_SE0_0_RX_STROBE_P
K38	HPC1_HB17_CC_N_B2	K38	MSIOD22NB2/SPWR_SE0_0_RX_STROBE_N
K40	VCCIO_HPC1_VIO_B_M2C_FMC	C40	VDDI2_1

4.10.5.2 FMC Connector J12

The RTG4 MSIO, MSIOD, Spacewire, CCC, SERDES1, and SERDES2 signals are routed to the J12 FMC connector for application development.

The following table provides the J12 FMC pinout details.

Table 16 • **J12 FMC Connector Pinout**

FMC Pin Number—J12	FMC Net Name	RTG4 Pin Number	RTG4 Pin Name
A2	HPC2_SERDES1_RXD1_P	AY11	SERDES_1_RXD1_P
A3	HPC2_SERDES1_RXD1_N	BA11	SERDES_1_RXD1_N

Table 16 • **J12 FMC Connector Pinout *(continued)***

FMC Pin Number—J12	FMC Net Name	RTG4 Pin Number	RTG4 Pin Name
A6	HPC2_SERDES1_RXD2_P	AV12	SERDES_1_RXD2_P
A7	HPC2_SERDES1_RXD2_N	AW12	SERDES_1_RXD2_N
A10	HPC2_SERDES1_RXD3_P	AY13	SERDES_1_RXD3_P
A11	HPC2_SERDES1_RXD3_N	BA13	SERDES_1_RXD3_N
A14	HPC2_SERDES2_RXD0_P	AY15	SERDES_2_RXD0_P
A15	HPC2_SERDES2_RXD0_N	BA15	SERDES_2_RXD0_N
A18	HPC2_SERDES2_RXD1_P	AV16	SERDES_2_RXD1_P
A19	HPC2_SERDES2_RXD1_N	AW16	SERDES_2_RXD1_N
A22	HPC2_SERDES1_TXD1_P	AU11	SERDES_1_TXD1_P
A23	HPC2_SERDES1_TXD1_N	AT11	SERDES_1_TXD1_N
A26	HPC2_SERDES1_TXD2_P	AU13	SERDES_1_TXD2_P
A27	HPC2_SERDES1_TXD2_N	AT13	SERDES_1_TXD2_N
A30	HPC2_SERDES1_TXD3_P	AW14	SERDES_1_TXD3_P
A31	HPC2_SERDES1_TXD3_N	AV14	SERDES_1_TXD3_N
A34	HPC2_SERDES2_TXD0_P	AU15	SERDES_2_TXD0_P
A35	HPC2_SERDES2_TXD0_N	AT15	SERDES_2_TXD0_N
A38	HPC2_SERDES2_TXD1_P	AU17	SERDES_2_TXD1_P
A39	HPC2_SERDES2_TXD1_N	AT17	SERDES_2_TXD1_N
B1	HPC2_CLK_DIR_B4	D35	MSIO349NB4
B12	HPC2_SERDES2_RXD3_P	AY19	SERDES_2_RXD3_P
B13	HPC2_SERDES2_RXD3_N	BA19	SERDES_2_RXD3_N
B16	HPC2_SERDES2_RXD2_P	AY17	SERDES_2_RXD2_P
B17	HPC2_SERDES2_RXD2_N	BA17	SERDES_2_RXD2_N
B20	HPC2_SERDES2_REFCLK0_P	AR16	SERDES_2_REFCLK_P
B21	HPC2_SERDES2_REFCLK0_N	AP16	SERDES_2_REFCLK_N
B32	HPC2_SERDES2_TXD3_P	AU19	SERDES_2_TXD3_P
B33	HPC2_SERDES2_TXD3_N	AT19	SERDES_2_TXD3_N
B36	HPC2_SERDES2_TXD2_P	AW18	SERDES_2_TXD2_P
B37	HPC2_SERDES2_TXD2_N	AV18	SERDES_2_TXD2_N
C2	HPC2_SERDES1_TXD0_P	AU9	SERDES_1_TXD0_P
C3	HPC2_SERDES1_TXD0_N	AT9	SERDES_1_TXD0_N
C6	HPC2_SERDES1_RXD0_P	AV10	SERDES_1_RXD0_P
C7	HPC2_SERDES1_RXD0_N	AW10	SERDES_1_RXD0_N
C10	HPC2_LA06_P_B8	AB11	MSIOD176PB8
C11	HPC2_LA06_N_B8	AB10	MSIOD176NB8
C14	HPC2_LA10_P_B8	W7	MSIOD179PB8
C15	HPC2_LA10_N_B8	Y7	MSIOD179NB8

Table 16 • **J12 FMC Connector Pinout *(continued)***

FMC Pin Number—J12	FMC Net Name	RTG4 Pin Number	RTG4 Pin Name
C18	HPC2_LA14_P_B8	V8	MSIOD199PB8
C19	HPC2_LA14_N_B8	V9	MSIOD199NB8
C22	HPC2_LA18_CC_P_B8	M2	MSIOD198PB8/GB0_11/CCC_NW1_CLKI0/SPWR_NW1_0_RX_STROBE_P
C23	HPC2_LA18_CC_N_B8	M1	MSIOD198NB8/SPWR_NW1_0_RX_STROBE_N
C26	HPC2_LA27_P_B8	Y2	MSIOD171PB8
C27	HPC2_LA27_N_B8	Y1	MSIOD171NB8
C30	HPC2_SCL	B36	MSIO345PB4
C31	HPC2_SDA	B37	MSIO345NB4
C34	HPC2_GA0	F3	MSIOD229PB7
D4	HPC2_SERDES1_REFCLK0_P	AR12	SERDES_1_REFCLK_P
D5	HPC2_SERDES1_REFCLK0_N	AP12	SERDES_1_REFCLK_N
D8	HPC2_LA01_CC_P_B8	AA8	MSIOD182PB8/GB0_11/CCC_NW0_CLKI1/SPWR_NW0_0_RX_DATA_P
D9	HPC2_LA01_CC_N_B8	AB8	MSIOD182NB8/SPWR_NW0_0_RX_DATA_N
D11	HPC2_LA05_P_B8	Y9	MSIOD189PB8
D12	HPC2_LA05_N_B8	Y10	MSIOD189NB8
D14	HPC2_LA09_P_B8	W6	MSIOD172PB8
D15	HPC2_LA09_N_B8	Y6	MSIOD172NB8
D17	HPC2_LA13_P_B8	W8	MSIOD195PB8
D18	HPC2_LA13_N_B8	W9	MSIOD195NB8
D20	HPC2_LA17_CC_P_B8	T3	MSIOD183PB8/GB0_11/CCC_NW0_CLKI0/SPWR_NW0_0_RX_STROBE_P
D21	HPC2_LA17_CC_N_B8	U3	MSIOD183NB8/SPWR_NW0_0_RX_STROBE_N
D23	HPC2_LA23_P_B8	U5	MSIOD187PB8
D24	HPC2_LA23_N_B8	V5	MSIOD187NB8
D26	HPC2_LA26_P_B8	AA3	MSIOD168PB8/GB0_11/CCC_NW1_CLKI2/SPWR_NW1_1_RX_STROBE_P
D27	HPC2_LA26_N_B8	AB3	MSIOD168NB8/SPWR_NW1_1_RX_STROBE_N
D35	HPC2_GA1	F2	MSIOD229NB7
E21	HPC2_HB03_P_B7	P9	MSIOD220PB7
E22	HPC2_HB03_N_B7	N9	MSIOD220NB7
E24	HPC2_HB05_P_B7	L8	MSIOD208PB7

Table 16 • **J12 FMC Connector Pinout *(continued)***

FMC Pin Number—J12	FMC Net Name	RTG4 Pin Number	RTG4 Pin Name
E25	HPC2_HB05_N_B7	M8	MSIOD208NB7
E27	HPC2_HB09_P_B7	F4	MSIOD223PB7
E28	HPC2_HB09_N_B7	E4	MSIOD223NB7
E30	HPC2_HB13_P_B7	J2	MSIOD213PB7
E31	HPC2_HB13_N_B7	J1	MSIOD213NB7
E33	HPC2_HB19_P_B7	L5	MSIOD214PB7
E34	HPC2_HB19_N_B7	M5	MSIOD214NB7
E36	HPC2_HB21_P_B7	P11	MSIOD221PB7
E37	HPC2_HB21_N_B7	R11	MSIOD221NB7
E39	VCCIO_HPC2_VADJ	AA13	VDDI8_1
F1	HPC2_PG_M2C	J30	MSIO356NB4
F4	HPC2_HA00_CC_P_B8	AB5	MSIOD167PB8/GB0_11/CCC_NW1_CLKI3/SPWR_NW1_1_RX_DATA_P
F5	HPC2_HA00_CC_N_B8	AB6	MSIOD167NB8/SPWR_NW1_1_RX_DATA_N
F22	HPC2_HB02_P_B7	K5	MSIOD219PB7/GB0_11/CCC_SW1_CLKI0/SPWR_SW1_0_RX_STROBE_P
F23	HPC2_HB02_N_B7	K4	MSIOD219NB7/SPWR_SW1_0_RX_STROBE_N
F25	HPC2_HB04_P_B7	M7	MSIOD212PB7
F26	HPC2_HB04_N_B7	M6	MSIOD212NB7
F28	HPC2_HB08_P_B7	H3	MSIOD222PB7
F29	HPC2_HB08_N_B7	J3	MSIOD222NB7
F31	HPC2_HB12_P_B7	K2	MSIOD205PB7
F32	HPC2_HB12_N_B7	K1	MSIOD205NB7
F34	HPC2_HB16_P_B7	N6	MSIOD207PB7
F35	HPC2_HB16_N_B7	N5	MSIOD207NB7
F37	HPC2_HB20_P_B7	R9	MSIOD216PB7
F38	HPC2_HB20_N_B7	R10	MSIOD216NB7
F40	VCCIO_HPC2_VADJ	AA13	VDDI8_1
G2	HPC2_CLK1_M2C_P_B1	M40	MSIOD43PB1/GB12_23/CCC_NE0_CLKI0/SPWR_NE0_0_RX_STROBE_P
G3	HPC2_CLK1_M2C_N_B1	M41	MSIOD43NB1/SPWR_NE0_0_RX_STROBE_N
G6	HPC2_LA00_CC_P_B8	V11	MSIOD197PB8/GB0_11/CCC_NW1_CLKI1/SPWR_NW1_0_RX_DATA_P

Table 16 • **J12 FMC Connector Pinout *(continued)***

FMC Pin Number—J12	FMC Net Name	RTG4 Pin Number	RTG4 Pin Name
G7	HPC2_LA00_CC_N_B8	V10	MSIOD197NB8/SPWR_NW1_0_RX_DATA_N
G9	HPC2_LA03_P_B8	AB12	MSIOD173PB8
G10	HPC2_LA03_N_B8	AA12	MSIOD173NB8
G12	HPC2_LA08_P_B8	Y11	MSIOD185PB8
G13	HPC2_LA08_N_B8	W11	MSIOD185NB8
G15	HPC2_LA12_P_B8	U8	MSIOD200PB8
G16	HPC2_LA12_N_B8	U7	MSIOD200NB8
G18	HPC2_LA16_P_B8	R7	MSIOD191PB8
G19	HPC2_LA16_N_B8	T7	MSIOD191NB8
G21	HPC2_LA20_P_B8	V4	MSIOD177PB8
G22	HPC2_LA20_N_B8	W4	MSIOD177NB8
G24	HPC2_LA22_P_B8	AA2	MSIOD166PB8
G25	HPC2_LA22_N_B8	AB2	MSIOD166NB8
G27	HPC2_LA25_P_B8	N4	MSIOD192PB8
G28	HPC2_LA25_N_B8	N3	MSIOD192NB8
G30	HPC2_LA29_P_B8	N1	MSIOD190PB8
G31	HPC2_LA29_N_B8	P1	MSIOD190NB8
G33	HPC2_LA31_P_B8	R2	MSIOD186PB8
G34	HPC2_LA31_N_B8	R1	MSIOD186NB8
G36	HPC2_LA33_P_B8	U1	MSIOD180PB8
G37	HPC2_LA33_N_B8	V1	MSIOD180NB8
G39	VCCIO_HPC2_VADJ	AA13	VDDI8_1
H2	HPC2_PRSNT_M2CL	F35	MSIO357NB4
H4	HPC2_CLK0_M2C_P_B1	AA34	MSIOD59PB1/GB12_23/CCC_NE1_CLKI1/SPWR_NE1_0_RX_DATA_P
H5	HPC2_CLK0_M2C_N_B1	AB34	MSIOD59NB1/SPWR_NE1_0_RX_DATA_N
H7	HPC2_LA02_P_B8	AA7	MSIOD178PB8
H8	HPC2_LA02_N_B8	AB7	MSIOD178NB8
H10	HPC2_LA04_P_B8	AA10	MSIOD184PB8
H11	HPC2_LA04_N_B8	AA9	MSIOD184NB8
H13	HPC2_LA07_P_B8	V12	MSIOD194PB8
H14	HPC2_LA07_N_B8	W12	MSIOD194NB8
H16	HPC2_LA11_P_B8	Y4	MSIOD170PB8
H17	HPC2_LA11_N_B8	AA4	MSIOD170NB8
H19	HPC2_LA15_P_B8	Y5	MSIOD169PB8

Table 16 • **J12 FMC Connector Pinout *(continued)***

FMC Pin Number—J12	FMC Net Name	RTG4 Pin Number	RTG4 Pin Name
H20	HPC2_LA15_N_B8	AA5	MSIOD169NB8
H22	HPC2_LA19_P_B8	U6	MSIOD188PB8
H23	HPC2_LA19_N_B8	V6	MSIOD188NB8
H25	HPC2_LA21_P_B8	T5	MSIOD196PB8
H26	HPC2_LA21_N_B8	T4	MSIOD196NB8
H28	HPC2_LA24_P_B8	P3	MSIOD193PB8
H29	HPC2_LA24_N_B8	P2	MSIOD193NB8
H31	HPC2_LA28_P_B8	V3	MSIOD174PB8
H32	HPC2_LA28_N_B8	W3	MSIOD174NB8
H34	HPC2_LA30_P_B8	T2	MSIOD181PB8
H35	HPC2_LA30_N_B8	U2	MSIOD181NB8
H37	HPC2_LA32_P_B8	W2	MSIOD175PB8
H38	HPC2_LA32_N_B8	W1	MSIOD175NB8
H40	VCCIO_HPC2_VADJ	AA13	VDDI8_1
J2	HPC2_CLK3_BIDIR_P_B1	V31	MSIOD44PB1/GB12_23/CCC_NE0_CLKI1/SPWR_NE0_0_RX_DATA_P
J3	HPC2_CLK3_BIDIR_N_B1	V32	MSIOD44NB1/SPWR_NE0_0_RX_DATA_N
J24	HPC2_HB01_P_B7	R12	MSIOD215PB7
J25	HPC2_HB01_N_B7	T12	MSIOD215NB7
J27	HPC2_HB07_P_B7	J6	MSIOD224PB7
J28	HPC2_HB07_N_B7	K6	MSIOD224NB7
J30	HPC2_HB11_P_B7	G1	MSIOD217PB7
J31	HPC2_HB11_N_B7	H1	MSIOD217NB7
J33	HPC2_HB15_P_B7	P7	MSIOD206PB7
J34	HPC2_HB15_N_B7	P6	MSIOD206NB7
J36	HPC2_HB18_P_B7	U12	MSIOD209PB7
J37	HPC2_HB18_N_B7	U11	MSIOD209NB7
J39	VCCIO_HPC2_VIO_B_M2C_FMC	C2	VDDI7_1
K1	VCCIO_HPC2_VIO_B_M2C_FMC	C2	VDDI7_1
K4	HPC2_CLK2_BIDIR_P_B1	T39	MSIOD58PB1/GB12_23/CCC_NE1_CLKI0/SPWR_NE1_0_RX_STROBE_P
K5	HPC2_CLK2_BIDIR_N_B1	U39	MSIOD58NB1/SPWR_NE1_0_RX_STROBE_N
K25	HPC2_HB00_CC_P_B7	N8	MSIOD218PB7/GB0_11/CCC_SW1_CLKI1/SPWR_SW1_0_RX_DATA_P

Table 16 • **J12 FMC Connector Pinout *(continued)***

FMC Pin Number—J12	FMC Net Name	RTG4 Pin Number	RTG4 Pin Name
K26	HPC2_HB00_CC_N_B7	P8	MSIOD218NB7/SPWR_SW1_0_RX_DATA_N
K28	HPC2_HB06_CC_P_B7	G3	MSIOD228PB7/GB0_11/CCC_SW0_CLKI0/SPWR_SW0_0_RX_STROBE_P
K29	HPC2_HB06_CC_N_B7	G2	MSIOD228NB7/SPWR_SW0_0_RX_STROBE_N
K31	HPC2_HB10_P_B7	L4	MSIOD210PB7
K32	HPC2_HB10_N_B7	L3	MSIOD210NB7
K34	HPC2_HB14_P_B7	U10	MSIOD211PB7
K35	HPC2_HB14_N_B7	T10	MSIOD211NB7
K37	HPC2_HB17_CC_P_B7	N10	MSIOD227PB7/GB0_11/CCC_SW0_CLKI1/SPWR_SW0_0_RX_DATA_P
K38	HPC2_HB17_CC_N_B7	N11	MSIOD227NB7/SPWR_SW0_0_RX_DATA_N
K40	VCCIO_HPC2_VIO_B_M2C_FMC	C2	VDDI7_1

5 Pin List

For the RTG4 Development Board pin list, see the CG1657 Package Pin Assignment Table at *http://www.microsemi.com/document-portal/doc_download/134616-cg1657-package-pin-assignment-table*.

6 Board Components Placement

The following two figures show the placement of various components of the RTG4 Development Kit silkscreen from the top and bottom view.

Figure 19 • **RTG4 Development Kit Silkscreen Top View**

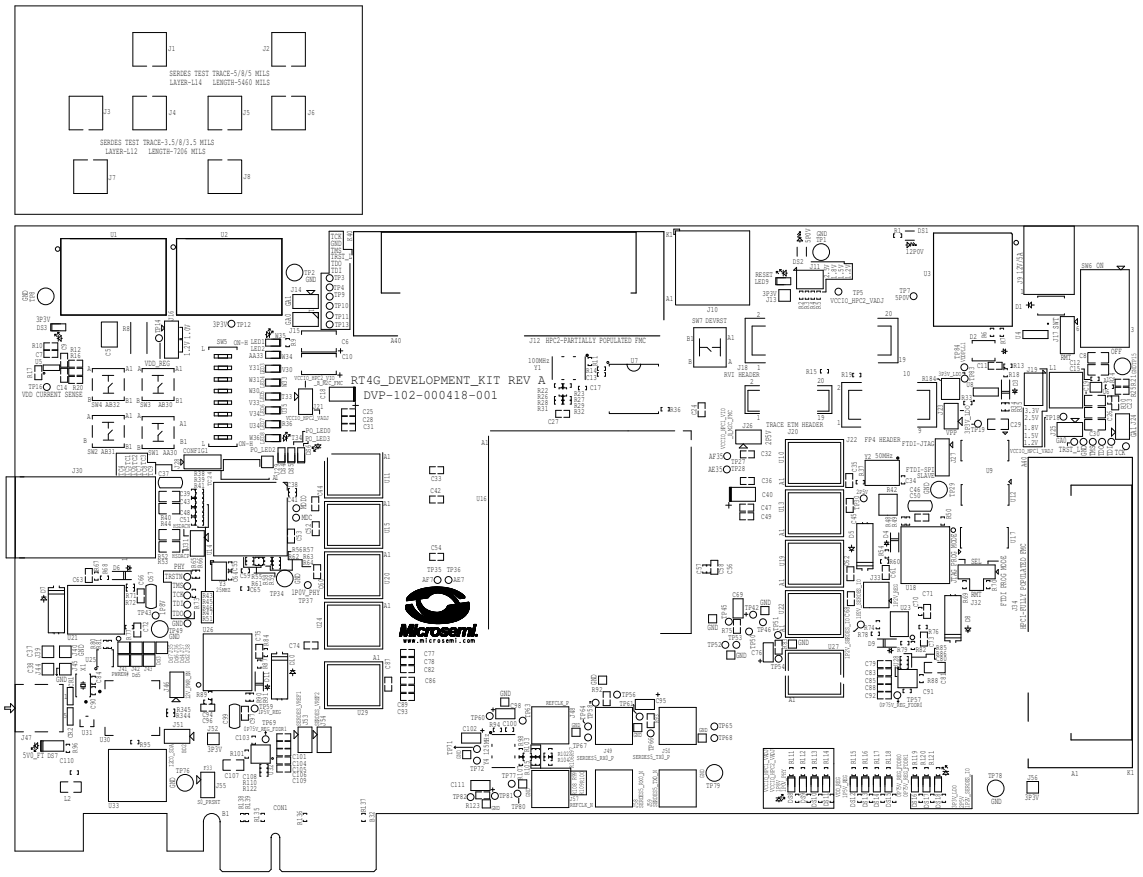
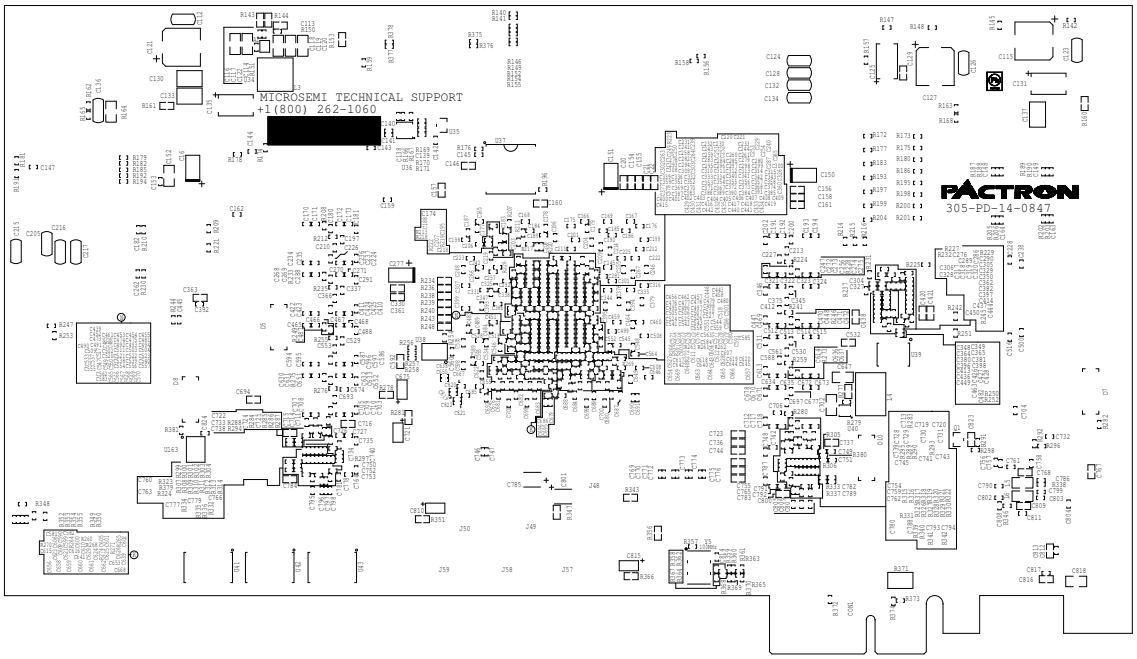


Figure 20 • **RTG4 Development Kit Silkscreen Bottom View**



7 Demo Design

The RTG4 Development Kit does not come with a preloaded demo design, but it can be programmed using the following demo designs associated with the following documents.

- *DG0624: RTG4 FPGA SERDES EPCS Protocol Design Demo Guide*
- *DG0622: RTG4 FPGA PCIe Data Plane Demo using Two Channel Fabric DMA Demo Guide*
- *LG0623: RTG4 FPGA Fabric Lab Guide*
- *DG0630: RTG4 FPGA DSP FIR Filter Demo Guide*
- *DG0625: Interfacing RTG4 FPGA with the External DDR3 Memory Through FDDR Demo Guide*

8 Software Installation

The RTG4 Development Kit has an on-board embedded FlashPro5 (FP5) programmer supported the by FlashPro version 11.5 or later. An external programmer is not required.

The following are the system requirements for FlashPro:

- Windows 7 Professional or later 64-bit operating system
- 500 MB disk space

For more information about system requirements, see *http://www.microsemi.com/products/fpga-soc/design-resources/programming/flashpro#software*.

Download and install FlashPro version 11.5, available at *http://soc.microsemi.com/download/reg/download.aspx?p=f%3dFlashProv11_5*. Then, connect one end of the USB cable (mini USB to Type A USB cable) to J47, and connect the other end to the USB port. If the cable is already connected, unplug the cable and connect it again. Once the USB cable is connected, the PC will detect the on-board embedded FP5 and install the drivers.

Note: Installing drivers is a one-time process.

9 Appendix: Programming the Device Using FlashPro4

The following table lists jumper settings for programming the board using FlashPro4.

Table 17 • **Jumper Settings for Programming Using FlashPro4**

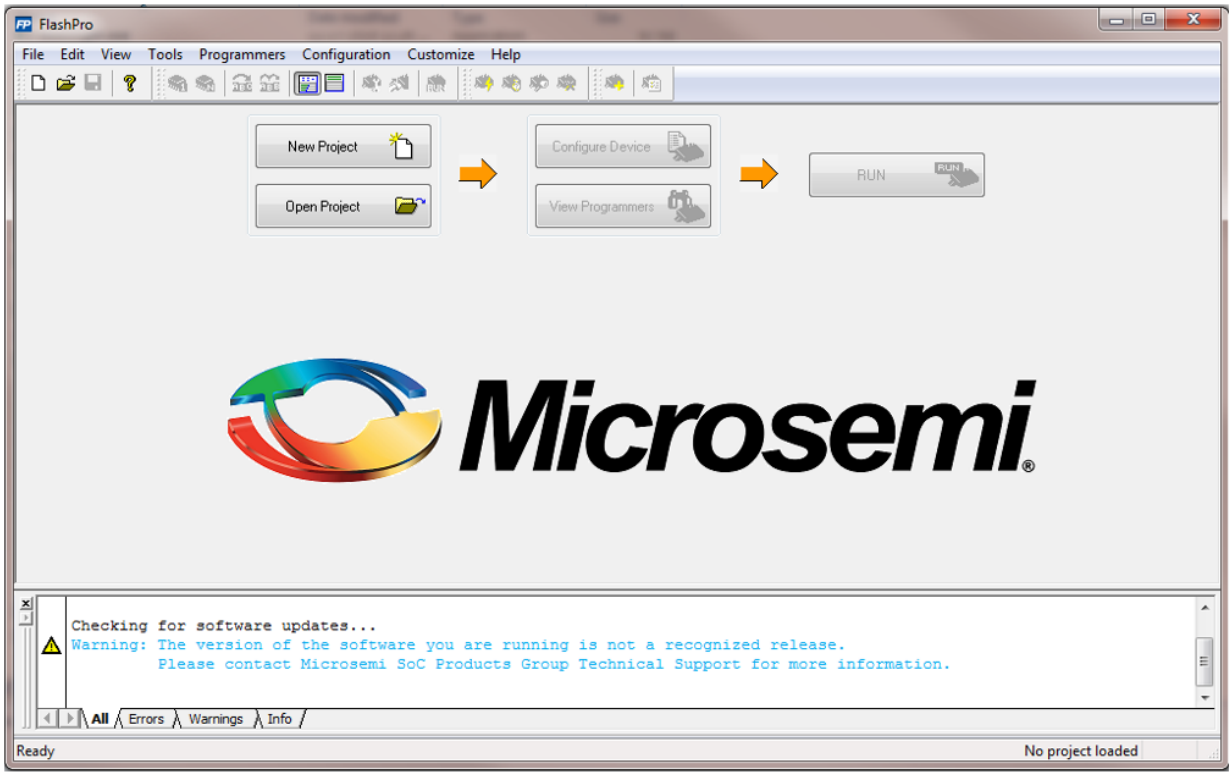
Jumper	Description	Pins	Settings
J32	PROG-SEL-JUMPER	2-3	Short
J27	JTAG/SPI SEL	1-2	Short
J23	VPP power jumper	1-2	Short

The following steps describe how to program the board using FlashPro4.

Note: Ensure FlashPro4 is installed on the host PC.

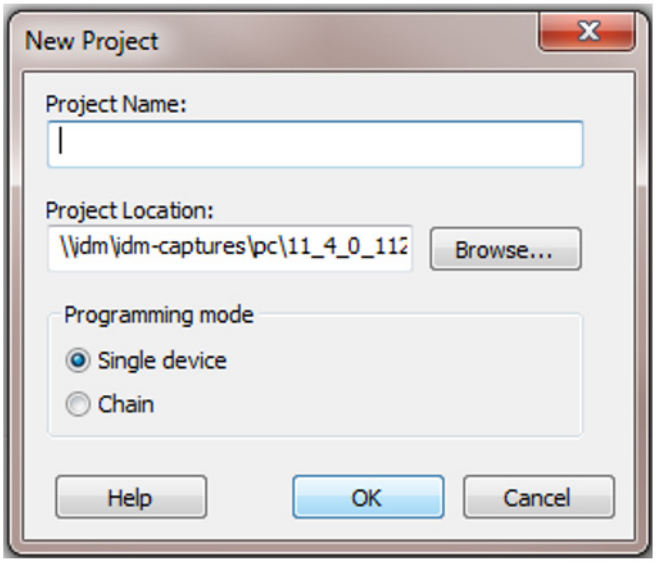
1. Connect the FlashPro4 header to **J22**.
2. Switch **ON** the **SW6** power supply switch.
3. Open the FlashPro software.

Figure 21 • **FlashPro Window**



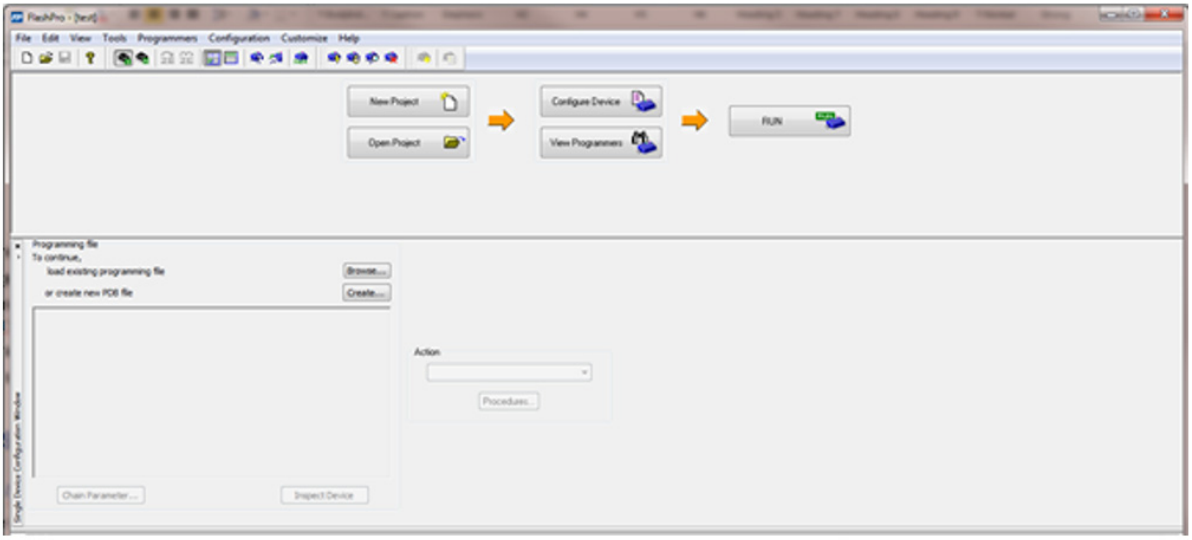
4. Click **New Project** to create a new project, as shown in Figure 22, page 44.
   - Enter the **Project Name**.
   - Select **Single device** as the Programming mode, then click **OK**.

Figure 22 • **Creating a New Project**



5. Click **Configure Device**, as shown in the following figure.
   - Click **Browse**, then select the `uprom Boot mtd 40KB uPROM Final.stp` file from the **Load Programming File** window.

Figure 23 • **Configuring the Device**



6. Click **Program** to program the device.
7. When the device is programmed successfully, the status **Run Program PASSED** is displayed.