Product Update

Errata to Z8 Encore! XP® Z8F0823 Series

UP007503-1207

Z8 Encore! XP® Z8F0823 Series Silicon with All Date Codes

Table 1 lists the errata found in Z8 Encore! XP® Z8F0823 Series devices with all date codes. When reviewing the following errata, it is recommend to download the latest version of the Product Specification from www.zilog.com. Data in this document is Preliminary only. Refer to the product specification for the supported memory configurations.

Table 1. Z8 Encore! XP® Z8F0823 Series Errata for Devices with All Date Codes

No	Summary	Detailed Description
1	Table 115 of PS0243 indicates FLAGS are modified by BIT, BSET, and BCLR instructions. This is incorrect.	Table 115: '*eZ8 CPU Instruction Summary*' indicates that FLAG status is changed when the BIT, BSET, or BCLR instructions are invoked. These commands have no effect on FLAG status.
2	Vectored interrupts do not work upon Stop Mode Recovery.	If Stop Mode Recovery is triggered by an interrupt, the pending interrupt is cleared before completing the recovery and is not serviced. **Workaround** None.
3	Stop Mode Recovery does not reset the state of the Watchdog Timer (WDT) enable.	According to the product specification, the WDT must be disabled upon completion of Stop Mode Recovery, unless the WDT_AO option bit is asserted. For this and all previous silicon revisions, the WDT continues to run after a WDT Event. **Workaround** After entering STOP mode, you must manually disable the WDT oscillator using the oscillator control register. Before re-entering STOP mode, the WDT oscillator must be re-enabled.
4	Stop Mode Recovery requires special RESET pin handling.	The default configuration for the RESET pin (PD0 on the 20- and 28-pin devices, PA2 on the 8-pin devices) is the reset function. If this pin is reprogrammed to any other function, the device does not properly recover from STOP mode. **Workaround** Before entering STOP mode, ensure that the RESET pin is programmed to the reset function.

Z8 Encore! XP® Z8F0823 Series (8-pin Devices)

Errata for Date Codes 0439 and Later

Table 2 lists the errata found in the production of Z8 Encore! XP Z8F0823 Series 8-pin products with date codes 0439 and later, where the code is YYWW (year and week of assembly). Refer to the product specification for the supported memory configurations.

Table 2. Z8 Encore! XP® Z8F0823 Series Errata (8-pin Devices) with Date Codes 0439 and Later

No	Summary	Detailed Description
1	Internal Precision Oscillator (IPO) frequency out of specification over voltage and temperature.	The IPO frequency is specified to be 5.5296 MHz +/- 4% over the supply voltage range of 2.7 V to 3.6 V and the temperature range of -40 ºC to +105 ºC. Actual silicon performance is +/-4% only over a supply voltage range of 3.15 V to 3.45 V and a temperature range of 0 ºC to +70 ºC. **Workaround** If the application requires better than +/-4% oscillator accuracy, the voltage and temperature must be controlled such that they remain within the above ranges.
2	Writes to the Timer Polarity (TPOL) bit must be done twice when the timer is not enabled.	When the timer is not enabled, the TPOL bit does not affect the timer output when changed. **Workaround** When the timer is not enabled, write the Timer Control Register 1 twice with the same value. This causes the correct timer output.
3	Programmable pull-up resistors source less than the specified current.	The pull-up devices are specified to source at least 30 µA. Actually, the pull-up devices source 7 µA. **Workaround** If a faster pull-up is required, use an external pull-up resistor.
4	PA2 does not output a strong high.	The PMOS output device of the PA2 port is disabled. The PA2 port does not output a high level unless the internal pull-up resistor is enabled. This pull-up resistor is enabled by default but it must not be turned off unless the port is pulled up externally. As there is no active drive high, the PA2 port only produces slow rising edges. **Workaround** If a fast rising edge response time is required, use another GPIO port.
5	Voltage Brownout (VBO)/Power On-Reset (POR) hysteresis is greater than specified in the product specification.	The hysteresis is measured to be around 100 mV. **Workaround** None.

Table 2. Z8 Encore! XP® Z8F0823 Series Errata (8-pin Devices) with Date Codes 0439 and Later (Continued)

No	Summary	Detailed Description
6	WDT default timeout period longer than specified.	The default timeout period of the WDT is 100 ms. However, for this version of silicon, the default timeout value is equal to the maximum timeout value. **Workaround** Manually set the WDT timeout to the appropriate value.
7	Slow V_{DD} ramp can hang the device.	When the power supply voltage takes longer than 20 ms to ramp, the device sometimes fail to exit reset. **Workaround** Speed up the V_{DD} ramp or add an external circuit to generate an active Low start-up pulse on the RESET pin. This circuit can be a simple RC delay with time-constant greater than the power supply ramp time.
8	UART driver enable pin does not work.	The DE function is not available on Port A2 as specified. **Workaround** None.
9	VBO level higher than specified.	The VBO generates a reset at higher supply voltage levels than specified. **Workaround** Ensure that the supply voltage does not drop below 2.8 V.

Z8 Encore! XP® Z8F0823 Series (20-pin and 28-pin Devices)

Errata for Date Codes 0440 and Later

Table 3 lists the errata found in the production of Z8 Encore! XP Z8F0823 Series 20-pin and 28-pin products with date codes 0440 and later, where the code is YYWW (year and week of assembly). Refer to the product specification for the supported memory configurations.

Table 3. Z8 Encore! XP® Z8F0823 Series Errata (20- and 28-pin Devices) with Date Codes 0440 and Later

No	Summary	Detailed Description
1	IPO frequency out of specification over voltage and temperature.	The IPO frequency is specified to be 5.5296 MHz +/- 4% over the supply voltage range of 2.7 V to 3.6 V and the temperature range of -40 ºC to +105 ºC. Actual silicon performance is +/-4% only over a supply voltage range of 3.15 V to 3.45 V and a temperature range of 0 ºC to +70 ºC. **Workaround** If the application requires better than +/-4% oscillator accuracy, the voltage and temperature must be controlled such that they remain within the above ranges.
2	Writes to the TPOL bit must be done twice when the timer is not enabled.	When the timer is not enabled, the TPOL bit does not affect the timer output when changed. **Workaround** When the timer is not enabled, write the Timer Control Register 1 twice with the same value. This causes the correct timer output.
3	Programmable pull-up resistors source less than the specified current.	The pull-up devices are specified to source at least 30 µA. In actuality, the pull-up devices sources 7 µA. **Workaround** If a faster pull-up is required, use an external pull-up resistor.
4	PD0 does not output a strong high.	The PMOS output device of the PD0 port is disabled. The PD0 port does not output a high level unless the internal pull-up resistor is enabled. This pull-up resistor is enabled by default but it should not be turned off unless the port is pulled up externally. As there is no active drive high, the PD0 port only produces slow rising edges. **Workaround** If a fast rising edge response time is required, use another GPIO port.
5	VBO/POR hysteresis is greater than specified in the product specification.	The hysteresis has been measured to be around 100 mV. **Workaround** None.

Table 3. Z8 Encore! XP® Z8F0823 Series Errata (20- and 28-pin Devices) with Date Codes 0440 and Later

No	Summary	Detailed Description
6	WDT default timeout period longer than specified.	The default timeout period of the WDT is 100 ms. However, for this version of silicon, the default is equal to the maximum timeout value. **Workaround** Manually set the WDT timeout to the appropriate value.
7	Open drain output control only on Port A.	Open drain output configuration set by Port A-D Output Control subregisters is possible only for Port A pins. It is not possible to configure Port B, C, D pins for open drain output. **Workaround** None. Use Port A pins for open drain output.
8	External V_{REF} is not available on 20-pin parts.	For 20-pin devices, external V_{REF} is not an option on pin PC2. **Workaround** None.
9	IPO current consumption higher than typically specified.	When the IPO is enabled, the product specification gives a typical current consumption of 300 µA. The consumption for these date codes is typically 1.5 mA. **Workaround** None.

Errata for date codes 0426 and before 0440

Table 4 lists the errata for Z8 Encore! XP Z8F0823 Series 20- and 28-pin products with date codes 0426 and before 0440, where the code is YYWW (year and week of assembly). Refer to the product specification for the supported memory configurations.

Table 4. Z8 Encore! XP® Z8F0823 Series Errata (20- and 28-Pin) Devices with Date Codes 0426 and Before 0440

No	Summary	Detailed Description
1	IPO frequency out of specification over voltage and temperature.	The IPO frequency is specified to be 5.5296 MHz +/- 4% over the supply voltage range of 2.7 V to 3.6 V and the temperature range of -40 ºC to +105 ºC. Actual silicon performance is +/-4% only over a supply voltage range of 3.15 V to 3.45 V and a temperature range of 0 ºC to +70 ºC. **Workaround** If the application requires better than +/-4% oscillator accuracy, the voltage and temperature must be controlled such that they remain within the above ranges.

Table 4. Z8 Encore! XP® Z8F0823 Series Errata (20- and 28-Pin) Devices with Date Codes 0426 and Before 0440 (Continued)

No	Summary	Detailed Description
2	Writes to the TPOL bit must be done twice when the timer is not enabled.	When the timer is not enabled, the TPOL bit does not affect the timer output when changed. **Workaround** When the timer is not enabled, write the Timer Control Register 1 twice with the same value. This results in correct timer output.
3	Programmable pull-up resistors source less than the specified current.	The pull-up devices are specified to source at least 30 µA. Actually, the pull-up devices sources 7 µA. **Workaround:** If a faster pull-up is required, use an external pull-up resistor.
4	PD0 does not output a strong high.	The PMOS output device of the PD0 port is disabled. The PD0 port does not output a high level unless the internal pull-up resistor is enabled. This pull-up resistor is enabled by default but it must not be turned off unless the port is pulled up externally. As there is no active drive High, the PD0 port only produces slow rising edges. **Workaround** If a fast rising edge response time is required, use another GPIO port.
5	VBO/POR hysteresis is greater than specified in the product specification.	The hysteresis has been measured to be around 100 mV. **Workaround** None.
6	WDT default timeout period longer than specified.	The default timeout period of the WDT is 100 ms. However, for this version of silicon, the default is equal to the maximum timeout value. **Workaround** Manually set the WDT timeout to the appropriate value.
7	Open drain output control only on Port A.	Open drain output configuration set by Port A-D Output Control sub registers is possible only for Port A pins. It is not possible to configure Port B, C, D pins for open drain output. **Workaround** None. Use Port A pins for open drain output.
8	ADC internal reference voltage Error.	Internal reference voltage (V_{REF}) set by REFSEL field in the ADC Control Register was not set optimally, reporting 1.91 V for a specified 2.0 V setting. **Workaround** None. External V_{REF} sourced ADC measurements are not affected by this errata.

Table 4. Z8 Encore! XP® Z8F0823 Series Errata (20- and 28-Pin) Devices with Date Codes 0426 and Before 0440 (Continued)

No	Summary	Detailed Description
9	STOP mode current out of specification.	Measured STOP mode current with Low Power Op Amp (LPO) ON is 50 µA typical versus the specified 10 µA. STOP mode current with all peripherals OFF is 4 µA typical versus the specified 2 µA. **Workaround** None.
10	Unstable comparator output.	Internal reference voltage level set by the REFLVL field in the Comparator Control Register causes an unstable comparator output, worsening as the internal reference voltage increases. **Workaround** None.
11	External V_{REF} is not available on 20-pin parts.	For 20-pin devices, external V_{REF} is not an option on pin PC2. **Workaround** None.
12	IPO current consumption higher than typically specified.	When the IPO is enabled, the product specification gives a typical current consumption of 300 µA. The consumption for these date codes is typically 1.5 mA. **Workaround** None.

Errata for date codes 0352 and before 0426

Table 5 lists the errata for Z8 Encore! XP Z8F0823 Series 20- and 28-pin products with date codes 0352 and before 0426, where the date code is YYWW (year and week of assembly). Refer to the product specification for the supported memory configurations.

Table 5. Z8 Encore! XP® Z8F0823 Series Errata (20- and 28-pin) Devices with Date Codes 0352 and Before 0426

No	Summary	Detailed Description
1	IPO frequency out of specification over voltage and temperature.	The IPO frequency is specified to be 5.5296 MHz +/- 4% over the supply voltage range of 2.7 V to 3.6 V and the temperature range of -40 ºC to +105 ºC. Actual silicon performance is +/-4% only over a supply voltage range of 3.15 V to 3.45 V and a temperature range of 0 ºC to +70 ºC. **Workaround** If the application requires better than +/-4% oscillator accuracy, the voltage and temperature must be controlled such that they remain within the above ranges.

Table 5. Z8 Encore! XP® Z8F0823 Series Errata (20- and 28-pin) Devices with Date Codes 0352 and Before 0426 (Continued)

No	Summary	Detailed Description
2	Writes to the TPOL bit must be done twice when the timer is not enabled.	When the timer is not enabled, the TPOL bit does not affect the timer output when changed. **Workaround** When the timer is not enabled, write the Timer Control Register 1 twice with the same value. This causes the correct timer output.
3	Programmable pull-up resistors source less than the specified current.	The pull-up devices are specified to source at least 30 µA. Actually, the pull-up devices sources 7 µA. **Workaround** If a faster pull-up is required, use an external pull-up resistor.
4	PD0 does not output a strong high.	The PMOS output device of the PD0 port is disabled. The PD0 port does not output a high level unless the internal pull-up resistor is enabled. This pull-up resistor is enabled by default but it must not be turned off unless the port is pulled up externally. As there is no active drive high, the PD0 port only produces slow rising edges. **Workaround** If a fast rising edge response time is required, use another GPIO port.
5	VBO/POR hysteresis is greater than specified in the product specification.	The hysteresis has been measured to be around 100 mV. **Workaround** None.
6	WDT default timeout period longer than specified.	The default timeout period of the WDT is 100 ms. However, for this version of silicon, the default value is equal to the maximum timeout value. **Workaround** Manually set the WDT timeout to the appropriate value.
7	Open drain output control only on Port A.	Open drain output configuration set by Port A-D Output Control sub registers is possible only for Port A pins. It is not possible to configure Port B, C, D pins for open drain output. **Workaround** None. Use Port A pins for open drain output.
8	ADC internal reference voltage error.	Internal reference voltage (V_{REF}) set by REFSEL field in the ADC Control Register was not set optimally, reporting 1.91 V for a specified 2.0 V setting. **Workaround** None. External V_{REF} sourced ADC measurements are not affected by this errata.

Table 5. Z8 Encore! XP® Z8F0823 Series Errata (20- and 28-pin) Devices with Date Codes 0352 and Before 0426 (Continued)

No	Summary	Detailed Description
9	Excessive STOP mode current.	ICCS, Supply Current in STOP mode, is out of specification. Consumption in the 1—3 mA range is typical. **Workaround** None.
10	Unstable comparator output.	Internal reference voltage level set by the REFLVL field in the Comparator Control Register causes an unstable comparator output, worsening as the internal reference voltage increases. **Workaround** None.
11	IPO 32 kHz frequency error.	Two frequencies can be chosen for the oscillator: 5.5296 MHz or 32.768 kHz. The frequency is selected by the OCSEL bit in the Oscillator Control Register. A 32 kHz operation is not trimmed to the specified accuracy because of an error in a divider circuit. **Workaround** None. In 32.768 kHz mode best case frequency is 32 kHz.
12	Internal V_{REF} has excessive variation with V_{DD}.	Internal Voltage Reference (V_{REF}) set by REFSEL field in the ADC Control register does not stay within specification over the full V_{DD} range. **Workaround** ADC measurements assume 15% V_{REF} error when using the internal voltage reference. The error is 5% more than specified and appears as an ADC gain error, not as an offset error. External V_{REF} sourced ADC measurements are not affected by this errata.
13	WDT frequency is incorrect.	WDT oscillator frequency is specified at 10 kHz but actually is 5 kHz. **Workaround** Set WDT reload and timeout delay parameters based on the 5 kHz frequency.
14	Potential electromigration issues through V_{DD} pads.	Current metal width does not support target current density specification for production products. **Workaround** Devices with these date codes (silicon revision AA) are not recommended for use in high current draw continuous operation applications.

Table 5. Z8 Encore! XP® Z8F0823 Series Errata (20- and 28-pin) Devices with Date Codes 0352 and Before 0426 (Continued)

No	Summary	Detailed Description
15	Switching from PD0 to $\overline{\text{RESET}}$ causes a reset.	$\overline{\text{RESET}}$ and Port D0 are multiplexed on one package pin. Port D0 is a general-purpose output-only pin configuration. When switching the Alternate Function Sub-register PDAF from PD0 output mode (00H) to $\overline{\text{RESET}}$ input mode (01H) generates a device external reset. **Workaround** None.
16	STOP mode does not automatically power down some blocks.	Executing the eZ8 CPU's STOP instruction does not fully place the device into STOP mode. **Workaround** Manually power down blocks using the power control register before entering STOP mode.
17	WDT unlock state machine requires flush for subsequent writes.	WDT state machine does not return the correct state following a single write operation. **Workaround** After each WDT write insert an additional dummy write to the WDT control register to flush the state machine.
18	External V_{REF} is not available on 20-pin parts.	For 20-pin devices, external V_{REF} is not an option on pin PC2. **Workaround** None.
19	IPO current consumption higher than typically specified.	When the IPO is enabled, the product specification gives a typical current consumption of 300 µA. The consumption for these date codes is typically 1.5 mA. **Workaround** None.

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