dsPIC33FJ256MCX06A/X08A/X10A Family Silicon Errata and Data Sheet Clarification

The dsPIC33FJ256MCX06A/X08A/X10A family devices that you have received conform functionally to the current Device Data Sheet (DS70594**C**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the dsPIC33FJ256MCX06A/X08A/X10A silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A4**).

Data Sheet clarifications and corrections start on page 7, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 3 or PICkit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 3 programmer/debugger or PICkit 3.
2. From the main menu in MPLAB IDE, select *Configure>Select Device*, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The Device and Revision ID values for the various dsPIC33FJ256MCX06A/X08A/X10A silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)		
		A2	A3	A4
dsPIC33FJ256MC510A	0x07B7	0x3002	0x3003	0x3004
dsPIC33FJ256MC710A	0x07BF			

Note 1: The Device and Revision IDs (DEVID and DEVREV) are located at the last two implemented addresses in program memory.

2: Refer to the *"dsPIC33F/PIC24H Flash Programming Specification"* (DS70152) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)		
				A2	A3	A4
ECAN™	WAKIF bit	1.	The WAKIF bit in the CxINTF register cannot be cleared by software instruction after the device is interrupted from Sleep due to activity on the CAN bus.	X	X	X
ECAN	DMA	2.	False DMA Error Traps may be generated in applications that perform both transmissions and receptions using ECAN with DMA.	X		
QEI	Timer Gated Accumulation	3.	When Timer Gated Accumulation is enabled, the QEI does not generate an interrupt on every falling edge.	X	X	X
QEI	Timer Gated Accumulation	4.	When Timer Gated Accumulation is enabled, and an external signal is applied, the POSCNT increments and generates an interrupt after a match with MAXCNT.	X	X	X
UART	Break Characters	5.	The UART module will not generate consecutive break characters.	X	X	X
ADC	DONE bit	6.	The ADC Conversion Status bit (DONE) does not work when External Interrupt is selected as the ADC trigger source.	X	X	X
SPI	TBF bit	7.	Writing to the SPIBUF register as soon as the TBF bit is cleared will cause the SPI module to ignore the written data.	X	X	X
DMA Controller	CPU Write Collision Detection	8.	DMA CPU write collisions will not be detected.		X	X
ADC	Current Consumption in Sleep Mode	9.	If the ADC module is in an enabled state when the device enters Sleep mode, the power-down current (IPD) of the device may exceed the device data sheet specifications.	X	X	X
All	150ºC Operation	10.	Affected revisions of silicon only support 140ºC operation instead of 150ºC for extended operating temperature.	X	X	X
CPU	Interrupt Disable	11.	When a previous `DISI` instruction is active (i.e., the DISICNT register is non-zero), and the value of the DISICNT register is updated manually, the DISICNT register freezes and disables interrupts permanently.	X	X	X
CPU	`div.sd`	12.	When using the `div.sd` instruction, the overflow bit is not getting set when an overflow occurs.	X	X	X
UART	TX Interrupt	13.	A transmit (TX) Interrupt may occur before the data transmission is complete.	X	X	X
JTAG	Flash Programming	14.	JTAG Flash programming is not supported.	X	X	X
ADC	Analog Pins	15.	When sampling either AN0 or AN3 at 1.1 Msps on both CH0 and CH1, the CH1 sample is not identical to the CH0 sample. If CH0 and CH1 sample different ANx inputs, the samples are identical as they would be expected.	X	X	X
ECAN	DMA	16.	A DMA trap is not generated when the CPU and DMA write to the ECAN module at the same time.	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A4**).

1. Module: ECAN™

The WAKIF bit in the CxINTF register cannot be cleared by software instruction after the device is interrupted from Sleep due to activity on the CAN bus.

When the device wakes up from Sleep due to CAN bus activity, the ECAN module is placed in operational mode. The ECAN Event interrupt occurs due to the WAKIF flag. Trying to clear the flag in the Interrupt Service Routine (ISR) may not clear the flag. The WAKIF bit being set will not cause repetitive Interrupt Service Routine execution.

Work around

Although the WAKIF bit does not clear, the device Sleep and ECAN Wake functions continue to work as expected. If the ECAN event is enabled, the CPU will enter the Interrupt Service Routine due to the WAKIF flag getting set. The application can maintain a secondary flag, which tracks the device Sleep and Wake events.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

2. Module: ECAN

In user applications that perform both transmissions and receptions using ECAN with DMA, intermittent DMA Write Collisions might get generated, resulting in the generation of DMA Error Traps. The ECAN messages would be transmitted and received correctly even when these DMA Error Traps occur.

Work around

Within the DMA Error Trap service routine in the application software, read the DMACS0 register and inspect the two XWCOLn (n = 0, 1, …,7) bits corresponding to the DMA channels being used for ECAN transmission and reception.

For example, if DMA Channel 1 is used for ECAN Reception and DMA Channel 2 is used for ECAN Transmission, inspect the XWCOL1 and XWCOL2 bits. If either of these bits is found to be set, clear the DMACERR bit in the INTCON1 register and return from the DMA Error Trap service routine.

Affected Silicon Revisions

A2	A3	A4					
X							

3. Module: QEI

When the TQCS and TQGATE bits in the QEIxCON register are set, a QEI interrupt should be generated after an input pulse on the QEA input. This interrupt is not generated in the affected silicon.

Work around

None.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

4. Module: QEI

When the TQCS and TQGATE bits in the QEIxCON register are set, the POSCNT counter should not increment but erroneously does, and if allowed to increment to match MAXCNT, a QEI interrupt will be generated.

Work around

To prevent the erroneous increment of POSCNT while running the QEI in Timer Gated Accumulation mode, initialize MAXCNT = 0.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

5. Module: UART

The UART module will not generate consecutive break characters. Trying to perform a back-to-back Break character transmission will cause the UART module to transmit the dummy character used to generate the first Break character instead of transmitting the second Break character. Break characters are generated correctly if they are followed by non-Break character transmission.

Work around

None.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

6. Module: ADC

The ADC Conversion Status (DONE) bit (ADxCON1<0>) does not indicate completion of conversion when External Interrupt is selected as the ADC trigger source (ADxCON1<SSRC> = 1).

Work around

Use an ADC interrupt or poll ADxIF bit in the IFSx registers to determine the completion of conversion.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

7. Module: SPI

Writing to the SPIxBUF register as soon as the TBF bit is cleared will cause the SPI module to ignore the written data. *Applications that use SPI with DMA are not affected by this erratum.*

Work around

After the TBF bit is cleared, wait for a minimum duration of one SPI clock before writing to the SPIxBUF register.

Alternatively, do one of the following:

- Poll the RBF bit and wait for it to get set before writing to the SPIxBUF register
- Poll the SPI Interrupt flag and wait for it to get set before writing to the SPIxBUF register
- Use an SPI Interrupt Service Routine
- Use DMA

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

8. Module: DMA Controller

DMA CPU write collisions will not be detected, and the corresponding XWCOLn bit (n = 0, 1, …, 7) will not be set. As a result, a CPU write collision event will not generate a DMA Error Trap.

Work around

None. Before writing to any memory location in DMA RAM, ensure that none of the enabled DMA channels is using the same memory location for data transfers from a peripheral.

Affected Silicon Revisions

A2	A3	A4					
	X	X					

9. Module: ADC

If the ADC module is in an enabled state when the device enters Sleep mode as a result of executing a `PWRSAV #0` instruction, the device power-down current (IPD) may exceed the specifications listed in the device data sheet. This may happen even if the ADC module is disabled by clearing the ADON bit prior to entering Sleep mode.

Work around

In order to remain within the IPD specifications listed in the device data sheet, the user software must completely disable the ADC module by setting the ADC Module Disable bit in the corresponding Peripheral Module Disable register (PMDx), prior to executing a `PWRSAV #0` instruction.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

10. Module: All

The affected silicon revisions listed below are not warranted for operation at 150ºC.

Work around

Only use the affected revisions of silicon for Hi-Temp operating range from -40ºC to +140ºC.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

11. Module: CPU

When a previous `DISI` instruction is active (i.e., the DISICNT register is non-zero), and the value of the DISICNT register is updated manually, the DISICNT register freezes and disables interrupts permanently.

Work around

Avoid updating the DISICNT register manually. Instead, use the `DISI #n` instruction with the required value for '`n`'.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

12. Module: CPU

When using the Signed 32-by-16-bit Division instruction, `div.sd`, the overflow bit does not always get set when an overflow occurs.

Work around

Test for and handle overflow conditions outside of the `div.sd` instruction.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

13. Module: UART

When using UTXISEL = `01` (Interrupt when last character is shifted out of the Transmit Shift Register) and the final character is being shifted out through the Transmit Shift Register, the Transmit (TX) Interrupt may occur before the final bit is shifted out.

Work around

If it is critical that the interrupt processing occur only when all transmit operations are complete. Hold off the interrupt routine processing by adding a loop at the beginning of the routine that polls the Transmit Shift Register Empty bit (TRMT) before processing the rest of the interrupt.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

14. Module: JTAG

JTAG Flash programming is not supported.

Work around

None.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

15. Module: ADC

When sampling either AN0 or AN3 at 1.1 Msps on both CH0 and CH1, the CH1 sample is not identical to the CH0 sample. If CH0 and CH1 sample different ANx inputs the samples are identical as they would be expected.

Work around

Bring the analog signal into the device on two separate ANx pins. This will isolate the signals to the two channels when one sample starts at the same time another sample ends.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

16. Module: ECAN

A DMA trap is not generated when the CPU and DMA write to the ECAN module transmit SFR at the same time.

Work around

The CPU should not write to the ECAN transmit SFR while the DMA is in operation.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS70594**C**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: DC Characteristics: Idle Current (I_{IDLE})

The typical and maximum Idle Current specifications were incorrectly reported in Table 26-6 in the current version of the device data sheet. The correct specifications are provided in the following table.

TABLE 26-6: DC CHARACTERISTICS: IDLE CURRENT (I_{IDLE})

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Parameter No.	Typical	Max	Units	Conditions		
Idle Current (I_{IDLE}): Core OFF Clock ON Base Current						
DC40d	**11**	**16**	mA	-40°C	3.3V	10 MIPS
DC40a	**11**	**16**	mA	+25°C		
DC40b	**15**	**20**	mA	+85°C		
DC40c	**19**	**24**	mA	+125°C		
DC41d	**15**	**20**	mA	-40°C	3.3V	16 MIPS
DC41a	**15**	**20**	mA	+25°C		
DC41b	**19**	**24**	mA	+85°C		
DC41c	**24**	**29**	mA	+125°C		
DC42d	**19**	**24**	mA	-40°C	3.3V	20 MIPS
DC42a	**19**	**24**	mA	+25°C		
DC42b	**23**	**28**	mA	+85°C		
DC42c	**28**	**33**	mA	+125°C		
DC43a	**27**	**32**	mA	+25°C	3.3V	30 MIPS
DC43d	**27**	**32**	mA	-40°C		
DC43b	**30**	**35**	mA	+85°C		
DC43c	**36**	**41**	mA	+125°C		
DC44d	**35**	**41**	mA	-40°C	3.3V	40 MIPS
DC44a	**35**	**41**	mA	+25°C		
DC44b	**40**	**46**	mA	+85°C		
DC44c	**44**	**50**	mA	+125°C		

2. Module: I/O Pin Output Specifications

The I/O Pin Output specifications (V_{OL}, V_{OH} and $V_{OH}1$) were incorrectly reported in the Table 26-10 in the current version of the device data sheet. The correct specifications are provided in the following table.

TABLE 26-10: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
DO10	V_{OL}	**Output Low Voltage I/O Pins: 2x Sink Driver Pins - All pins not defined by 4x or 8x driver pins**	—	—	**0.4**	V	**I_{OL} ≤3 mA, V_{DD} = 3.3V See Note 1**
		Output Low Voltage I/O Pins: 4x Sink Driver Pins - RA2, RA3, RA9, RA10, RA14, RA15, RB0, RB1, RB11, RF4, RF5, RG2, RG3	—	—	**0.4**	V	**I_{OL} ≤6 mA, V_{DD} = 3.3V See Note 1**
		Output Low Voltage I/O Pins: 8x Sink Driver Pins - OSC2, CLKO, RC15	—	—	**0.4**	V	**I_{OL} ≤10 mA, V_{DD} = 3.3V See Note 1**
DO20	V_{OH}	**Output High Voltage I/O Pins: 2x Source Driver Pins - All pins not defined by 4x or 8x driver pins**	**2.4**	—	—	V	**I_{OL} ≥ -3 mA, V_{DD} = 3.3V See Note 1**
		Output High Voltage I/O Pins: 4x Source Driver Pins - RA2, RA3, RA9, RA10, RA14, RA15, RB0, RB1, RB11, RF4, RF5, RG2, RG3	**2.4**	—	—	V	**I_{OL} ≥ -6 mA, V_{DD} = 3.3V See Note 1**
		Output High Voltage I/O Pins: 8x Source Driver Pins - OSC2, CLKO, RC15	**2.4**	—	—	V	**I_{OL} ≥ -10 mA, V_{DD} = 3.3V See Note 1**

Note 1: Parameters are characterized, but not tested.

TABLE 26-10: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
DO20A	VOH1	**Output High Voltage I/O Pins: 2x Source Driver Pins - All pins not defined by 4x or 8x driver pins**	**1.5**	—	—	V	**IOH ≥ -6 mA, VDD = 3.3V See Note 1**
			2.0	—	—		**IOH ≥ -5 mA, VDD = 3.3V See Note 1**
			3.0	—	—		**IOH ≥ -2 mA, VDD = 3.3V See Note 1**
		Output High Voltage 4x Source Driver Pins - RA2, RA3, RA9, RA10, RA14, RA15, RB0, RB1, RB11, RF4, RF5, RG2, RG3	**1.5**	—	—	V	**IOH ≥ -12 mA, VDD = 3.3V See Note 1**
			2.0	—	—		**IOH ≥ -11 mA, VDD = 3.3V See Note 1**
			3.0	—	—		**IOH ≥ -3 mA, VDD = 3.3V See Note 1**
		Output High Voltage 8x Source Driver Pins - OSC2, CLKO, RC15	**1.5**	—	—	V	**IOH ≥ -16 mA, VDD = 3.3V See Note 1**
			2.0	—	—		**IOH ≥ -12 mA, VDD = 3.3V See Note 1**
			3.0	—	—		**IOH ≥ -4 mA, VDD = 3.3V See Note 1**

Note 1: Parameters are characterized, but not tested.

APPENDIX A: REVISION HISTORY

Rev A Document (9/2009)

Initial release of this document; issued for revision A2 silicon.

Includes silicon issues 1-2 (ECAN™), 3-4 (QEI), 5 (UART), 6 (ADC) and 7 (SPI).

Rev B Document (12/2009)

Added Rev. A3 silicon information.

Added silicon issue 8 (DMA Controller).

Rev C Document (6/2010)

Added silicon issue 9 (ADC) and data sheet clarification 1 (DC Characteristics: I/O Pin Input Specifications).

Rev D Document (9/2010)

Added silicon issue 10 (All).

Rev E Document (3/2011)

Removed data sheet clarification 1.

Rev F Document (11/2011)

Added silicon issues 11 (CPU), 12 (CPU), 13 (UART), and 14 (JTAG).

Rev G Document (4/2012)

Added Rev. A4 silicon information.

Added silicon issues 15 (ADC) and 16 (ECAN) and data sheet clarifications 1 (DC Characteristics: Idle Current (I_{IDLE})) and 2 (I/O Pin Output Specifications).

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