

MC74VHCT259A

8-Bit Addressable Latch/1-of-8 Decoder CMOS Logic Level Shifter with LSTTL-Compatible Inputs

The MC74VHCT259 is an 8-bit Addressable Latch fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output.

The VHC259 is designed for general purpose storage applications in digital systems. The device has four modes of operation as shown in the mode selection table. In the addressable latch mode, the signal on Data In is written into the addressed latch. The addressed latch follows the data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous state and are unaffected by the Data or Address inputs. In the one-of-eight decoding or demultiplexing mode, the addressed output follows the state of Data In with all other outputs in the LOW state. In the Reset mode, all outputs are LOW and unaffected by the address and data inputs. When operating the VHCT259 as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode.

The VHCT inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3 V to 5.0 V because it has full 5 V CMOS level output swings.

The VHCT259A input structures provide protection when voltages between 0 V and 5.5 V are applied, regardless of the supply voltage. The output structures also provide protection when $V_{CC} = 0$ V. These input and output structures help prevent device destruction caused by supply voltage—input/output voltage mismatch, battery backup, hot insertion, etc.

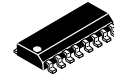
- High Speed: $t_{PD} = 7.6$ ns (Typ) at $V_{CC} = 5$ V
- Low Power Dissipation: $I_{CC} = 2$ μ A (Max) at $T_A = 25^\circ$ C
- TTL-Compatible Inputs: $V_{IL} = 0.8$ V; $V_{IH} = 2.0$ V
- Power Down Protection Provided on Inputs and Outputs
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance: HBM > 2000 V



ON Semiconductor™

<http://onsemi.com>

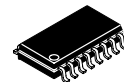
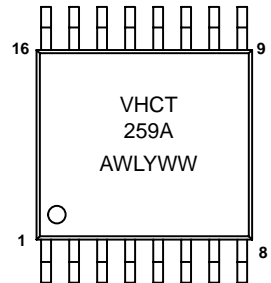
MARKING DIAGRAMS



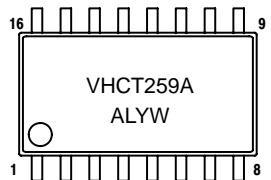
SOIC-16
D SUFFIX
CASE 751B



TSSOP-16
DT SUFFIX
CASE 948F



SOIC EIAJ-16
M SUFFIX
CASE 966



A = Assembly Location
L, WL = Wafer Lot
Y, YY = Year
W, WW = Work Week

ORDERING INFORMATION

| Device | Package | Shipping |
|------------------|--------------|-----------------|
| MC74VHCT259AD | SOIC-16 | 48 Units/Rail |
| MC74VHCT259ADR2 | SOIC-16 | 2500 Units/Reel |
| MC74VHCT259ADT | TSSOP-16 | 96 Units/Rail |
| MC74VHCT259ADTEL | TSSOP-16 | 2000 Units/Reel |
| MC74VHCT259ADTR2 | TSSOP-16 | 2500 Units/Reel |
| MC74VHCT259AM | SOIC EIAJ-16 | 50 Units/Rail |
| MC74VHCT259AMEL | SOIC EIAJ-16 | 2000 Units/Reel |

MC74VHCT259A

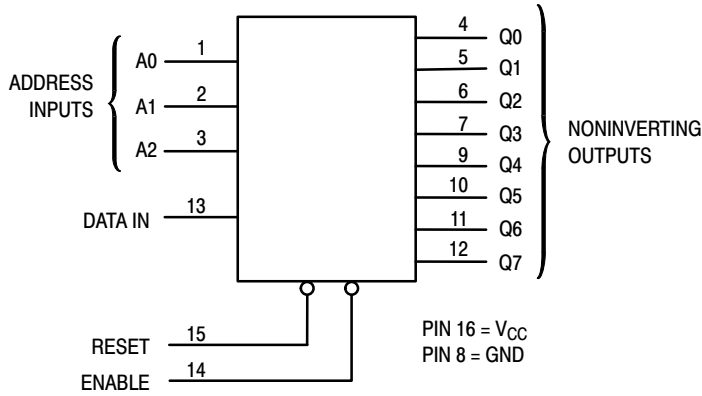


Figure 1. Logic Diagram

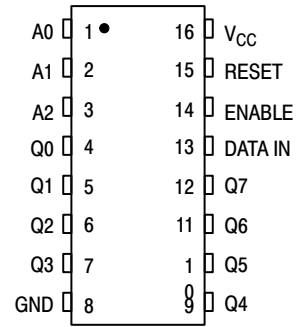


Figure 2. Pin Assignment

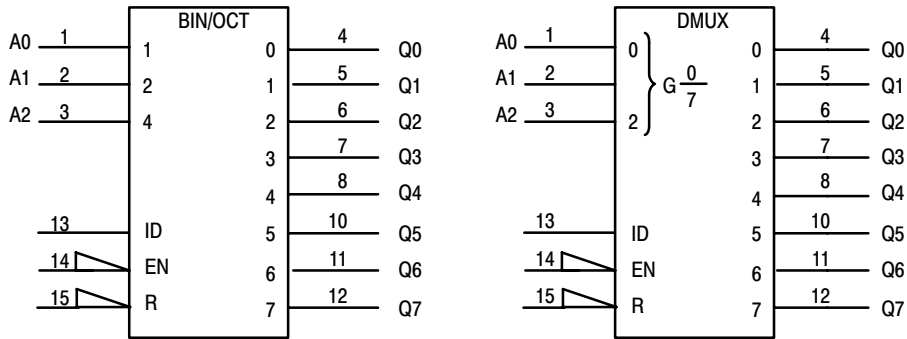


Figure 3. IEC Logic Symbol

MODE SELECTION TABLE

| Enable | Reset | Mode |
|--------|-------|----------------------|
| L | H | Addressable Latch |
| H | H | Memory |
| L | L | 8-Line Demultiplexer |
| H | L | Reset |

LATCH SELECTION TABLE

| Address Inputs | | | Latch Addressed |
|----------------|---|---|-----------------|
| C | B | A | |
| L | L | L | Q0 |
| L | L | H | Q1 |
| L | H | L | Q2 |
| L | H | H | Q3 |
| H | L | L | Q4 |
| H | L | H | Q5 |
| H | H | L | Q6 |
| H | H | H | Q7 |

MC74VHCT259A

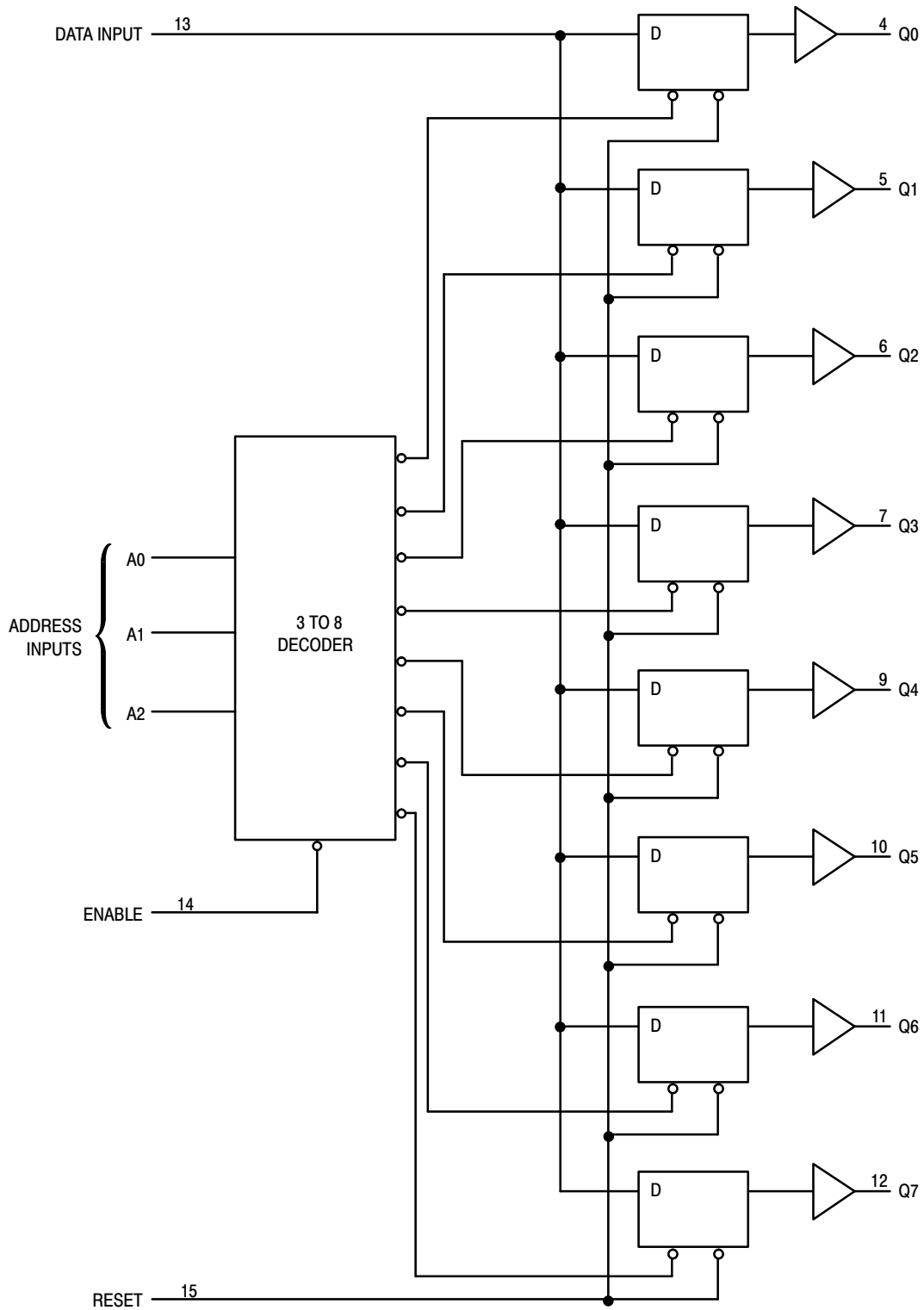


Figure 4. Expanded Logic Diagram

MC74VHCT259A

MAXIMUM RATINGS (Note 1.)

| Symbol | Parameter | Value | Unit |
|-----------------------|---|---|-------------|
| V _{CC} | Positive DC Supply Voltage | -0.5 to +7.0 | V |
| V _{IN} | Digital Input Voltage | -0.5 to +7.0 | V |
| V _{OUT} | DC Output Voltage | Output in 3-State High or Low State -0.5 to +7.0 -0.5 to V _{CC} +0.5 | V |
| I _{IK} | Input Diode Current | -20 | mA |
| I _{OK} | Output Diode Current | ± 20 | mA |
| I _{OUT} | DC Output Current, per Pin | ± 25 | mA |
| I _{CC} | DC Supply Current, V _{CC} and GND Pins | ± 75 | mA |
| P _D | Power Dissipation in Still Air | SOIC Package TSSOP 200 180 | mW |
| T _{STG} | Storage Temperature Range | -65 to +150 | °C |
| V _{ESD} | ESD Withstand Voltage | Human Body Model (Note 2.) Machine Model (Note 3.) Charged Device Model (Note 4.) >2000 >200 >2000 | V |
| I _{LATCH-UP} | Latch-Up Performance | Above V _{CC} and Below GND at 125°C (Note 5.) | ± 300 mA |
| θ _{JA} | Thermal Resistance, Junction to Ambient | SOIC Package TSSOP 143 164 | °C/W |

1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.
2. Tested to EIA/JESD22-A114-A
3. Tested to EIA/JESD22-A115-A
4. Tested to JESD22-C101-A
5. Tested to EIA/JESD78

RECOMMENDED OPERATING CONDITIONS

| Symbol | Characteristics | Min | Max | Unit |
|---------------------------------|--|--|------------------------|------------|
| V _{CC} | DC Supply Voltage | 4.5 | 5.5 | V |
| V _{IN} | DC Input Voltage | 0 | 5.5 | V |
| V _{OUT} | DC Output Voltage | Output in 3-State High or Low State 0 0 | 5.5 V _{CC} | V |
| T _A | Operating Temperature Range, all Package Types | -55 | 125 | °C |
| t _r , t _f | Input Rise or Fall Time | V _{CC} = 5.0 V ± 0.5 V | 0 | 20 ns/V |

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

| Junction Temperature °C | Time, Hours | Time, Years |
|-------------------------|-------------|-------------|
| 80 | 1,032,200 | 117.8 |
| 90 | 419,300 | 47.9 |
| 100 | 178,700 | 20.4 |
| 110 | 79,600 | 9.4 |
| 120 | 37,000 | 4.2 |
| 130 | 17,800 | 2.0 |
| 140 | 8,900 | 1.0 |

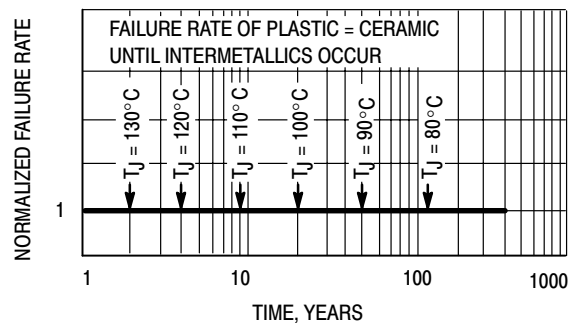


Figure 5. Failure Rate vs. Time Junction Temperature

MC74VHCT259A

DC CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Condition | V _{CC} (V) | T _A = 25°C | | | T _A ≤ 85°C | | -55°C ≤ T _A ≤ 125°C | | Unit |
|--------------------|---|--|------------------------|-----------------------|-----|------|-----------------------|------|--------------------------------|------|------|
| | | | | Min | Typ | Max | Min | Max | Min | Max | |
| V _{IH} | Minimum High-Level Input Voltage | | 4.5 to 5.5 | 2 | | | 2 | | 2 | | V |
| V _{IL} | Maximum Low-Level Input Voltage | | 4.5 to 5.5 | | | 0.8 | | 0.8 | | 0.8 | V |
| V _{OH} | Maximum High-Level Output Voltage | V _{IN} = V _{IH} or V _{IL} I _{OH} = -50 μA | 4.5 | 4.4 | 4.5 | | 4.4 | | 4.4 | | V |
| | | V _{IN} = V _{IH} or V _{IL} I _{OH} = -8 mA | 4.5 | 3.94 | | | 3.8 | | 3.66 | | V |
| V _{OL} | Maximum Low-Level Output Voltage | V _{IN} = V _{IH} or V _{IL} I _{OL} = 50 μA | 4.5 | | 0 | 0.1 | | 0.1 | | 0.1 | V |
| | | V _{IN} = V _{IH} or V _{IL} I _{OH} = 8 mA | 4.5 | | | 0.36 | | 0.44 | | 0.52 | V |
| I _{IN} | Input Leakage Current | V _{IN} = 5.5 V or GND | 0 to 5.5 | | | ±0.1 | | ±1.0 | | ±1.0 | μA |
| I _{CC} | Maximum Quiescent Supply Current | V _{IN} = V _{CC} or GND | 5.5 | | | 4.0 | | 40.0 | | 40.0 | μA |
| I _{CC(T)} | Additional Quiescent Supply Current (per Pin) | Any one input: V _{IN} = 3.4 V All other inputs: V _{IN} = V _{CC} or GND | 5.5 | | | 1.35 | | 1.5 | | 1.5 | μA |
| I _{OPD} | Output Leakage Current | V _{OUT} = 5.5 V | 0 | | | 0.5 | | 5 | | 5 | μA |

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 3.0ns)

| Symbol | Parameter | Test Conditions | T _A = 25°C | | | T _A ≤ 85°C | | -55°C ≤ T _A ≤ 125°C | | Unit |
|--|--|--|-----------------------|-----|------|-----------------------|------|--------------------------------|------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, Data to Output (Figures 6 and 11) | V _{CC} = 3.3 ± 0.3V C _L = 15pF | | 8.5 | 11.0 | 1.0 | 13.0 | 1.0 | 13.0 | ns |
| | | V _{CC} = 3.3 ± 0.3V C _L = 50pF | | 8.5 | 16.0 | 1.0 | 18.0 | 1.0 | 18.0 | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, Address Select to Output (Figures 7 and 11) | V _{CC} = 5.0 ± 0.5V C _L = 15pF | | 6.0 | 8.0 | 1.0 | 9.5 | 1.0 | 9.5 | ns |
| | | V _{CC} = 5.0 ± 0.5V C _L = 50pF | | 6.0 | 10.0 | 1.0 | 11.5 | 1.0 | 11.5 | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, Enable to Output (Figures 8 and 11) | V _{CC} = 3.3 ± 0.3V C _L = 15pF | | 8.5 | 11.0 | 1.0 | 13.0 | 1.0 | 13.0 | ns |
| | | V _{CC} = 3.3 ± 0.3V C _L = 50pF | | 8.5 | 16.0 | 1.0 | 18.0 | 1.0 | 18.0 | |
| t _{PHL} | Maximum Propagation Delay, Reset to Output (Figures 9 and 11) | V _{CC} = 5.0 ± 0.5V C _L = 15pF | | 6.0 | 8.0 | 1.0 | 9.5 | 1.0 | 9.5 | ns |
| | | V _{CC} = 5.0 ± 0.5V C _L = 50pF | | 6.0 | 10.0 | 1.0 | 11.5 | 1.0 | 11.5 | |
| C _{IN} | Maximum Input Capacitance | | | 6 | 10 | | 10 | | 10 | pF |

| C _{PD} | Power Dissipation Capacitance (Note 6.) | Typical @ 25°C, V _{CC} = 5.0V | | pF |
|-----------------|---|--|--|----|
| | | 30 | | |
| | | | | |

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

MC74VHCT259A

TIMING REQUIREMENTS (Input $t_r = t_f = 3.0\text{ns}$)

| Symbol | Parameter | Test Conditions | $T_A = 25^\circ\text{C}$ | | | $T_A \leq 85^\circ\text{C}$ | | $T_A \leq 125^\circ\text{C}$ | | Unit |
|------------|--|--------------------------------|--------------------------|-----|-----|-----------------------------|-----|------------------------------|-----|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| t_w | Minimum Pulse Width, Reset or Enable (Figure 10) | $V_{CC} = 3.3 \pm 0.3\text{V}$ | 5.0 | | | 5.5 | | 5.5 | | ns |
| | | $V_{CC} = 5.0 \pm 0.5\text{V}$ | 5.0 | | | 5.5 | | 5.5 | | |
| t_{su} | Minimum Setup Time, Address or Data to Enable (Figure 10) | $V_{CC} = 3.3 \pm 0.3\text{V}$ | 4.5 | | | 4.5 | | 4.5 | | ns |
| | | $V_{CC} = 5.0 \pm 0.5\text{V}$ | 3.0 | | | 3.0 | | 3.0 | | |
| t_h | Minimum Hold Time, Enable to Address or Data (Figure 8 or 9) | $V_{CC} = 3.3 \pm 0.3\text{V}$ | 2.0 | | | 2.0 | | 2.0 | | ns |
| | | $V_{CC} = 5.0 \pm 0.5\text{V}$ | 2.0 | | | 2.0 | | 2.0 | | |
| t_r, t_f | Maximum Input, Rise and Fall Times (Figure 6) | $V_{CC} = 3.3 \pm 0.3\text{V}$ | | | 400 | | 300 | | 300 | ns |
| | | $V_{CC} = 5.0 \pm 0.5\text{V}$ | | | 200 | | 100 | | 100 | |

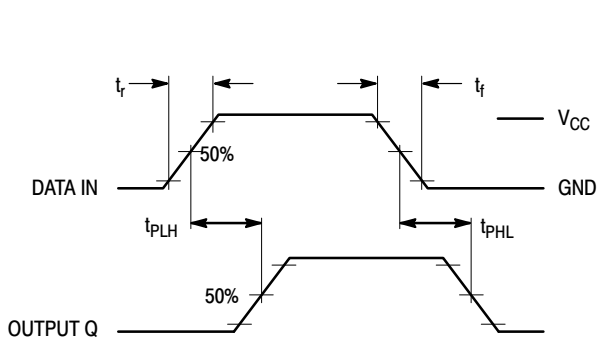


Figure 6. Switching Waveform

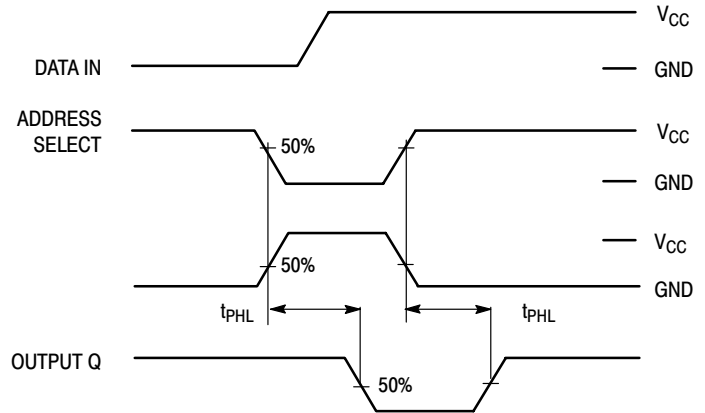


Figure 7. Switching Waveform

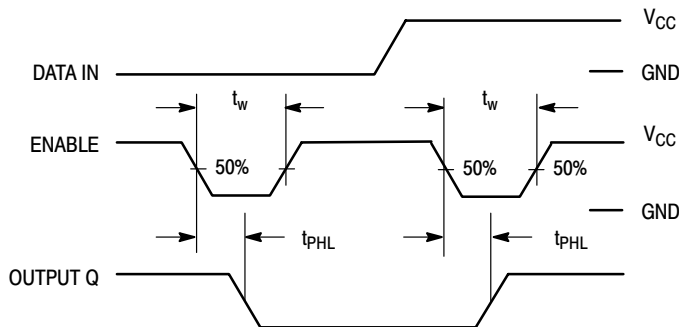


Figure 8. Switching Waveform

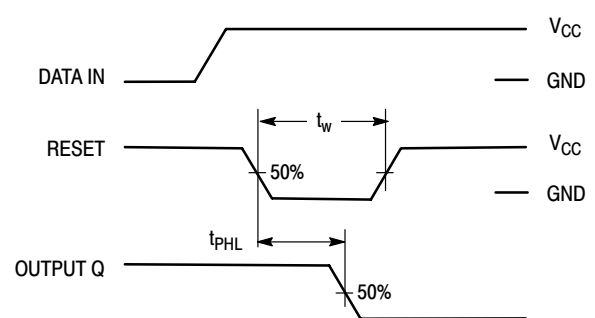


Figure 9. Switching Waveform

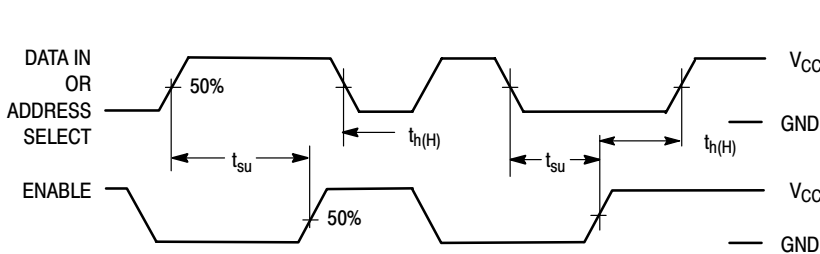
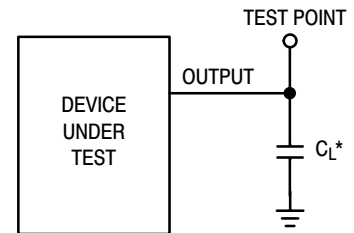


Figure 10. Switching Waveform



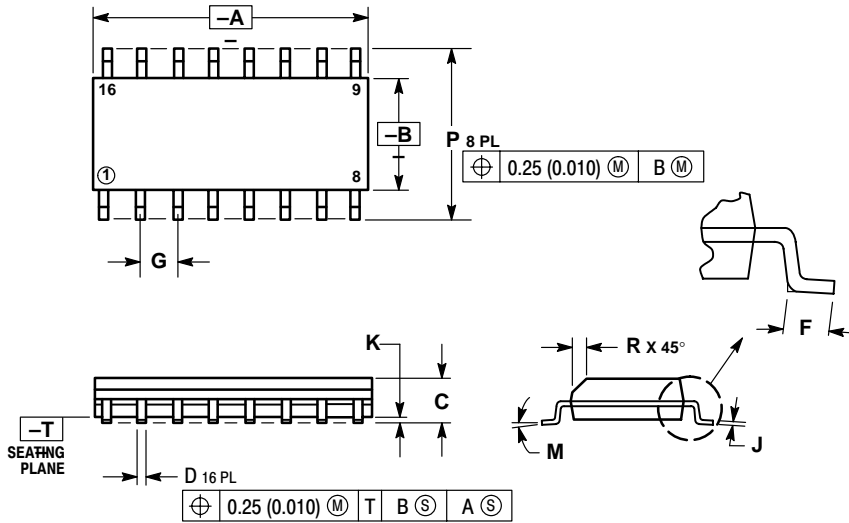
*Includes all probe and jig capacitance

Figure 11. Test Circuit

MC74VHCT259A

PACKAGE DIMENSIONS

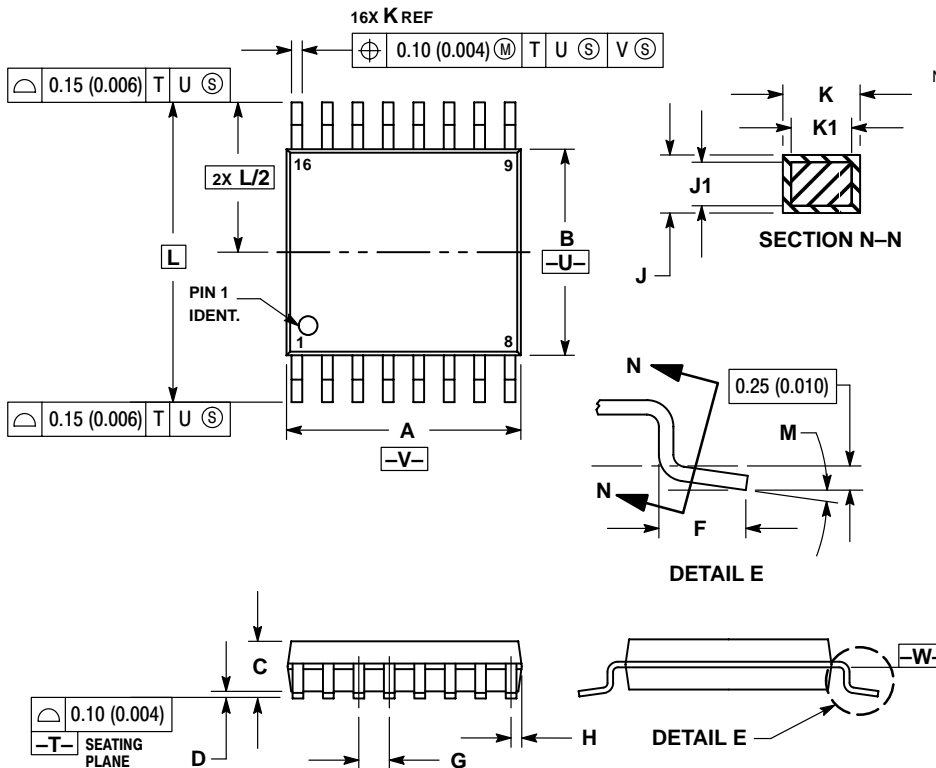
SOIC-16
D SUFFIX
CASE 751B-05
ISSUE J



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

TSSOP-16
DT SUFFIX
CASE 948F-01
ISSUE O



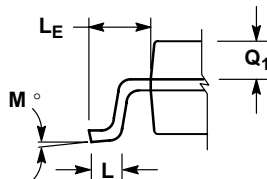
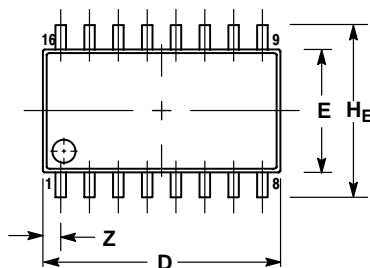
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.18 | 0.28 | 0.007 | 0.011 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

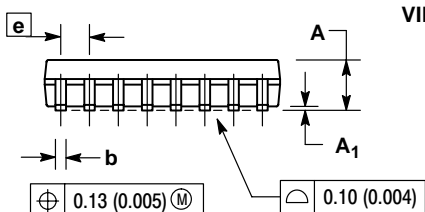
MC74VHCT259A

PACKAGE DIMENSIONS

SOIC EIAJ-16
M SUFFIX
CASE 966-01
ISSUE O



DETAIL P




VIEW P

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

| DIM | MILLIMETERS | | INCHES | |
|----------------|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | --- | 2.05 | --- | 0.081 |
| A ₁ | 0.05 | 0.20 | 0.002 | 0.008 |
| b | 0.35 | 0.50 | 0.014 | 0.020 |
| c | 0.18 | 0.27 | 0.007 | 0.011 |
| D | 9.90 | 10.50 | 0.390 | 0.413 |
| E | 5.10 | 5.45 | 0.201 | 0.215 |
| e | 1.27 BSC | | 0.050 BSC | |
| H _E | 7.40 | 8.20 | 0.291 | 0.323 |
| L | 0.50 | 0.85 | 0.020 | 0.033 |
| L _E | 1.10 | 1.50 | 0.043 | 0.059 |
| M | 0° | 10° | 0° | 10° |
| Q ₁ | 0.70 | 0.90 | 0.028 | 0.035 |
| Z | --- | 0.78 | --- | 0.031 |

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

PUBLICATION ORDERING INFORMATION

NORTH AMERICA Literature Fulfillment:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com
Fax Response Line: 303-675-2167 or 800-344-3810 Toll Free USA/Canada

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

EUROPE: LDC for ON Semiconductor – European Support

German Phone: (+1) 303-308-7140 (Mon-Fri 2:30pm to 7:00pm CET)
Email: ONlit-german@hibbertco.com
French Phone: (+1) 303-308-7141 (Mon-Fri 2:00pm to 7:00pm CET)
Email: ONlit-french@hibbertco.com
English Phone: (+1) 303-308-7142 (Mon-Fri 12:00pm to 5:00pm GMT)
Email: ONlit@hibbertco.com

EUROPEAN TOLL-FREE ACCESS*: 00-800-4422-3781

*Available from Germany, France, Italy, UK, Ireland

CENTRAL/SOUTH AMERICA:

Spanish Phone: 303-308-7143 (Mon-Fri 8:00am to 5:00pm MST)
Email: ONlit-spanish@hibbertco.com
Toll-Free from Mexico: Dial 01-800-288-2872 for Access –
then Dial 866-297-9322

ASIA/PACIFIC: LDC for ON Semiconductor – Asia Support

Phone: 1-303-675-2121 (Tue-Fri 9:00am to 1:00pm, Hong Kong Time)
Toll Free from Hong Kong & Singapore:
001-800-4422-3781
Email: ONlit-asia@hibbertco.com

JAPAN: ON Semiconductor, Japan Customer Focus Center

4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-0031
Phone: 81-3-5740-2700
Email: r14525@onsemi.com

ON Semiconductor Website: <http://onsemi.com>

For additional information, please contact your local Sales Representative.