

**OptiMOS™3 Power-Transistor**
**Features**

- Fast switching MOSFET for SMPS
- Optimized technology for DC/DC converters
- Qualified according to JEDEC<sup>1)</sup> for target applications
- N-channel; Logic level
- Excellent gate charge x  $R_{DS(on)}$  product (FOM)
- Very low on-resistance  $R_{DS(on)}$
- Superior thermal resistance
- 100% Avalanche tested
- Pb-free plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

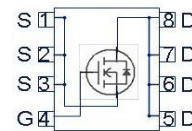
**Product Summary**

$V_{DS}$	40	V
$R_{DS(on),max}$	4.0	mΩ
$I_D$	40	A

PG-TSDSON-8



Type	Package	Marking
BSZ040N04LS G	PG-TSDSON-8	040N04L


**Maximum ratings, at  $T_j=25\text{ °C}$ , unless otherwise specified**

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	$I_D$	$V_{GS}=10\text{ V}, T_C=25\text{ °C}$	40	A
		$V_{GS}=10\text{ V}, T_C=100\text{ °C}$	40	
		$V_{GS}=4.5\text{ V}, T_C=25\text{ °C}$	40	
		$V_{GS}=4.5\text{ V}, T_C=100\text{ °C}$	40	
		$V_{GS}=10\text{ V}, T_A=25\text{ °C}, R_{thJA}=60\text{ K/W}^{2)}$	18	
Pulsed drain current <sup>3)</sup>	$I_{D,pulse}$	$T_C=25\text{ °C}$	160	
Avalanche current, single pulse <sup>4)</sup>	$I_{AS}$	$T_C=25\text{ °C}$	20	
Avalanche energy, single pulse	$E_{AS}$	$I_D=20\text{ A}, R_{GS}=25\text{ Ω}$	130	mJ
Gate source voltage	$V_{GS}$		±20	V

<sup>1)</sup> J-STD20 and JESD22

Maximum ratings, at  $T_j=25\text{ °C}$ , unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Power dissipation	$P_{\text{tot}}$	$T_C=25\text{ °C}$	69	W
		$T_A=25\text{ °C}$ , $R_{\text{thJA}}=60\text{ K/W}^2)$	2.1	
Operating and storage temperature	$T_j, T_{\text{stg}}$		-55 ... 150	°C
IEC climatic category; DIN IEC 68-1			55/150/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

#### Thermal characteristics

Thermal resistance, junction - case	$R_{\text{thJC}}$		-	-	1.8	K/W
Device on PCB	$R_{\text{thJA}}$	6 cm <sup>2</sup> cooling area <sup>2)</sup>	-	-	60	

Electrical characteristics, at  $T_j=25\text{ °C}$ , unless otherwise specified

#### Static characteristics

Drain-source breakdown voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}}=0\text{ V}, I_{\text{D}}=1\text{ mA}$	40	-	-	V
Gate threshold voltage	$V_{\text{GS(th)}}$	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=36\text{ }\mu\text{A}$	1.2	-	2	
Zero gate voltage drain current	$I_{\text{DSS}}$	$V_{\text{DS}}=40\text{ V}, V_{\text{GS}}=0\text{ V}, T_j=25\text{ °C}$	-	0.1	1	$\mu\text{A}$
		$V_{\text{DS}}=40\text{ V}, V_{\text{GS}}=0\text{ V}, T_j=125\text{ °C}$	-	10	100	
Gate-source leakage current	$I_{\text{GSS}}$	$V_{\text{GS}}=20\text{ V}, V_{\text{DS}}=0\text{ V}$	-	10	100	nA
Drain-source on-state resistance	$R_{\text{DS(on)}}$	$V_{\text{GS}}=4.5\text{ V}, I_{\text{D}}=20\text{ A}$	-	4.5	5.6	m $\Omega$
		$V_{\text{GS}}=10\text{ V}, I_{\text{D}}=20\text{ A}$	-	3.3	4	
Gate resistance	$R_{\text{G}}$		-	1.8	-	$\Omega$
Transconductance	$g_{\text{fs}}$	$ V_{\text{DS}} >2 I_{\text{D}} R_{\text{DS(on)max}}, I_{\text{D}}=20\text{ A}$	40	79	-	S

<sup>2)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70  $\mu\text{m}$  thick) copper area for drain connection. PCB is vertical in still air.

<sup>3)</sup> See figure 3 for more detailed information

<sup>4)</sup> See figure 13 for more detailed information

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Dynamic characteristics**

Input capacitance	$C_{iss}$	$V_{GS}=0\text{ V}, V_{DS}=20\text{ V},$ $f=1\text{ MHz}$	-	3800	5100	pF
Output capacitance	$C_{oss}$		-	830	1100	
Reverse transfer capacitance	$C_{rss}$		-	45	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=20\text{ V}, V_{GS}=10\text{ V},$ $I_D=20\text{ A}, R_G=1.6\ \Omega$	-	8.5	-	ns
Rise time	$t_r$		-	4.8	-	
Turn-off delay time	$t_{d(off)}$		-	33	-	
Fall time	$t_f$		-	5.4	-	

**Gate Charge Characteristics<sup>5)</sup>**

Gate to source charge	$Q_{gs}$	$V_{DD}=20\text{ V}, I_D=20\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	11	-	nC
Gate charge at threshold	$Q_{g(th)}$		-	6.1	-	
Gate to drain charge	$Q_{gd}$		-	4.9	-	
Switching charge	$Q_{sw}$		-	10	-	
Gate charge total	$Q_g$		-	48	64	
Gate plateau voltage	$V_{plateau}$		-	3.0	-	
Gate charge total	$Q_g$	$V_{DD}=20\text{ V}, I_D=20\text{ A},$ $V_{GS}=0\text{ to }4.5\text{ V}$	-	23	31	nC
Gate charge total, sync. FET	$Q_{g(sync)}$	$V_{DS}=0.1\text{ V},$ $V_{GS}=0\text{ to }10\text{ V}$	-	45	-	
Output charge	$Q_{oss}$	$V_{DD}=20\text{ V}, V_{GS}=0\text{ V}$	-	31	-	

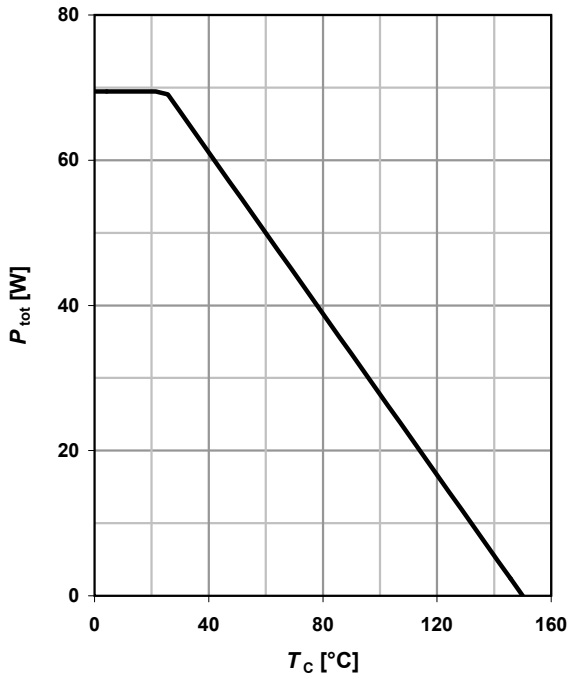
**Reverse Diode**

Diode continuous forward current	$I_S$	$T_C=25\text{ }^\circ\text{C}$	-	-	40	A
Diode pulse current	$I_{S,pulse}$		-	-	160	
Diode forward voltage	$V_{SD}$	$V_{GS}=0\text{ V}, I_F=20\text{ A},$ $T_j=25\text{ }^\circ\text{C}$	-	0.8	1.2	V
Reverse recovery charge	$Q_{rr}$	$V_R=20\text{ V}, I_F=I_S,$ $di_F/dt=400\text{ A}/\mu\text{s}$	-	26	-	nC

<sup>5)</sup> See figure 16 for gate charge parameter definition

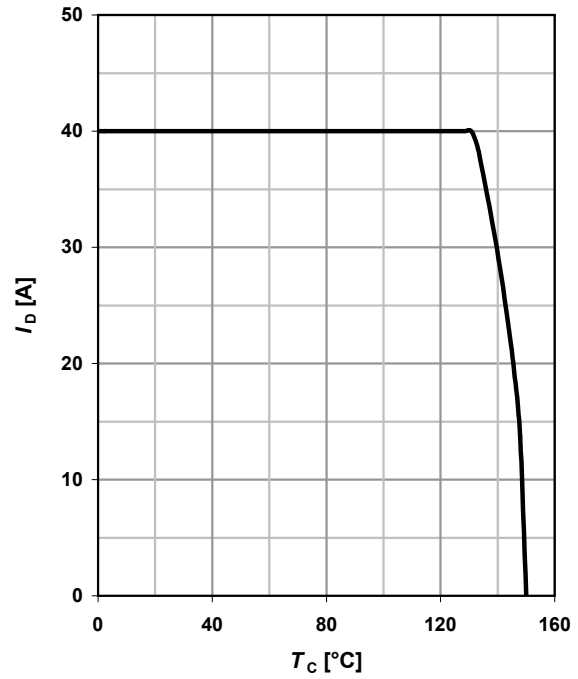
**1 Power dissipation**

$$P_{\text{tot}} = f(T_C)$$



**2 Drain current**

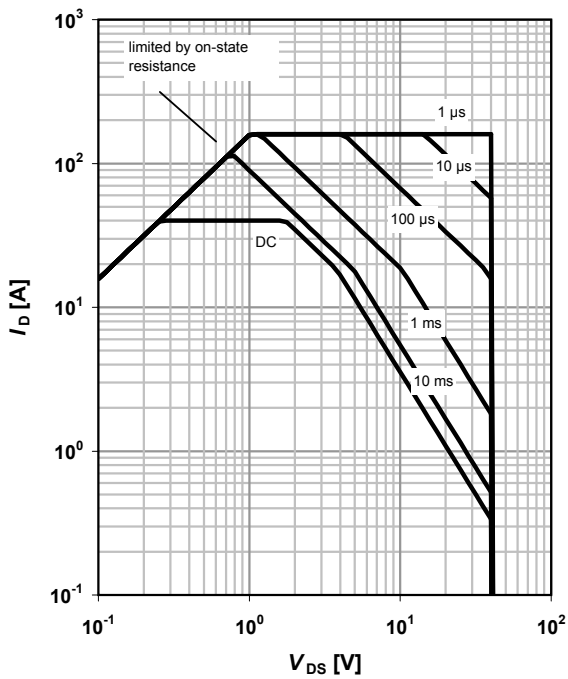
$$I_D = f(T_C); V_{\text{GS}} \geq 10 \text{ V}$$



**3 Safe operating area**

$$I_D = f(V_{\text{DS}}); T_C = 25 \text{ °C}; D = 0$$

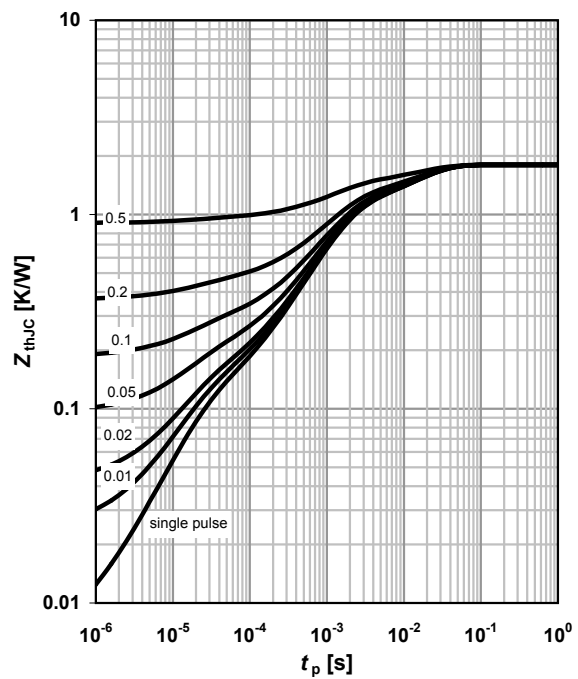
parameter:  $t_p$



**4 Max. transient thermal impedance**

$$Z_{\text{thJC}} = f(t_p)$$

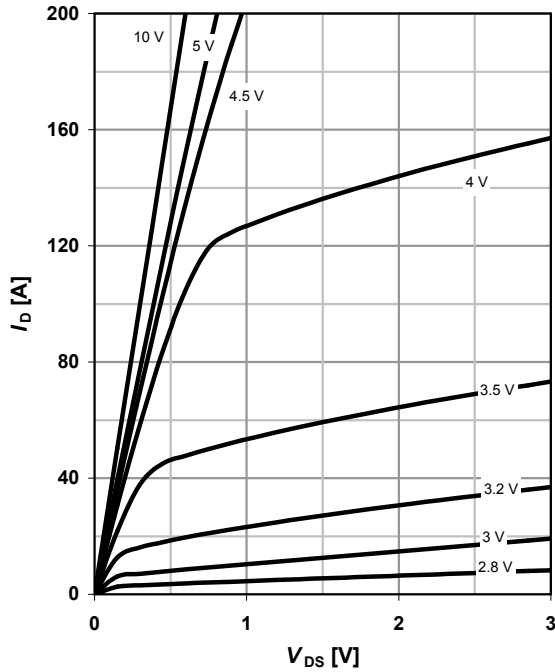
parameter:  $D = t_p / T$



**5 Typ. output characteristics**

$I_D = f(V_{DS}); T_j = 25\text{ }^\circ\text{C}$

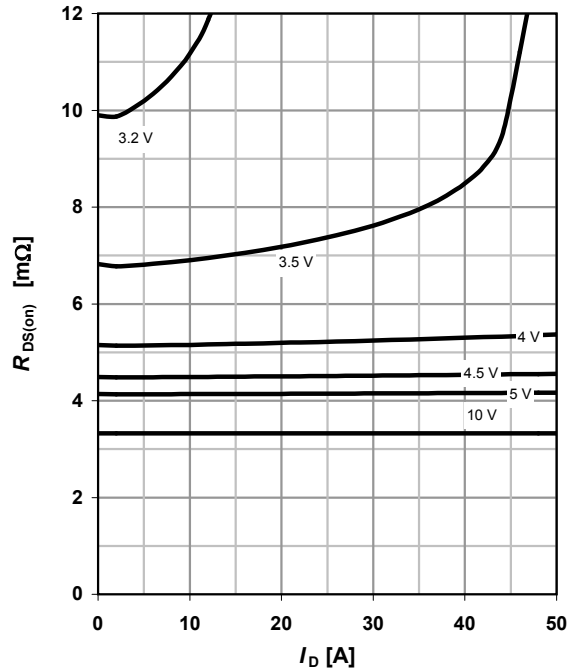
parameter:  $V_{GS}$



**6 Typ. drain-source on resistance**

$R_{DS(on)} = f(I_D); T_j = 25\text{ }^\circ\text{C}$

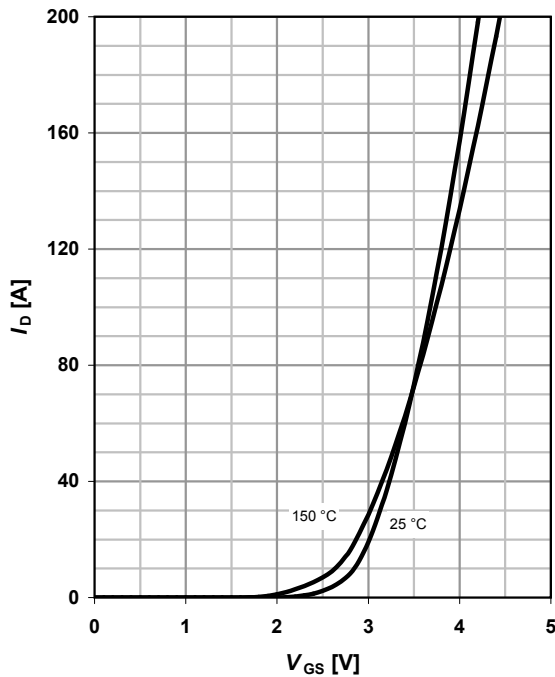
parameter:  $V_{GS}$



**7 Typ. transfer characteristics**

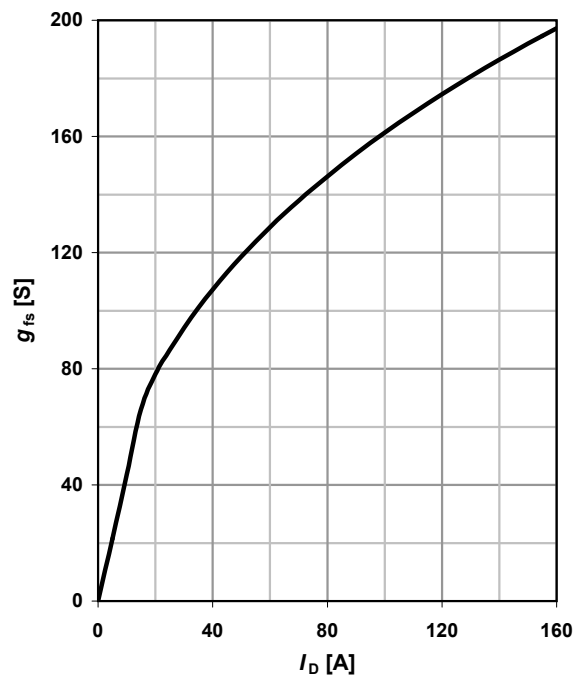
$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$

parameter:  $T_j$



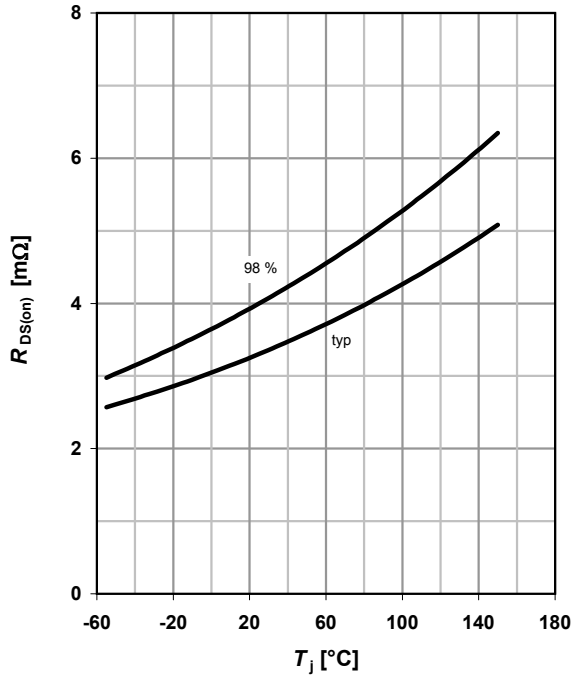
**8 Typ. forward transconductance**

$g_{fs} = f(I_D); T_j = 25\text{ }^\circ\text{C}$

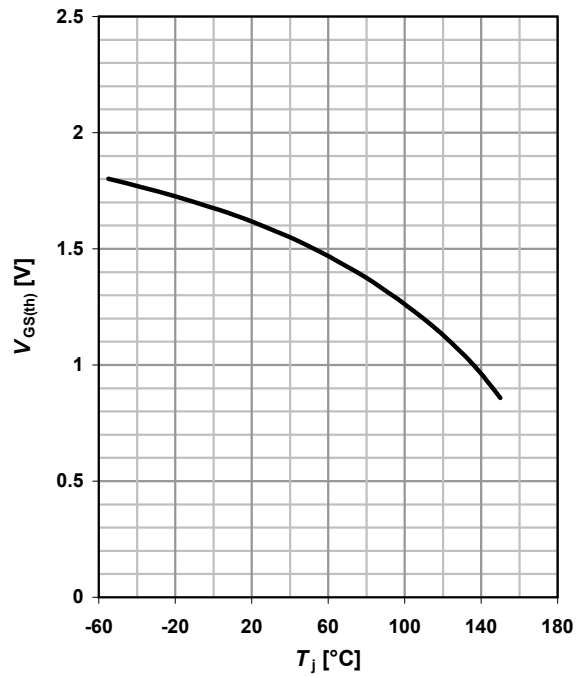


**9 Drain-source on-state resistance**

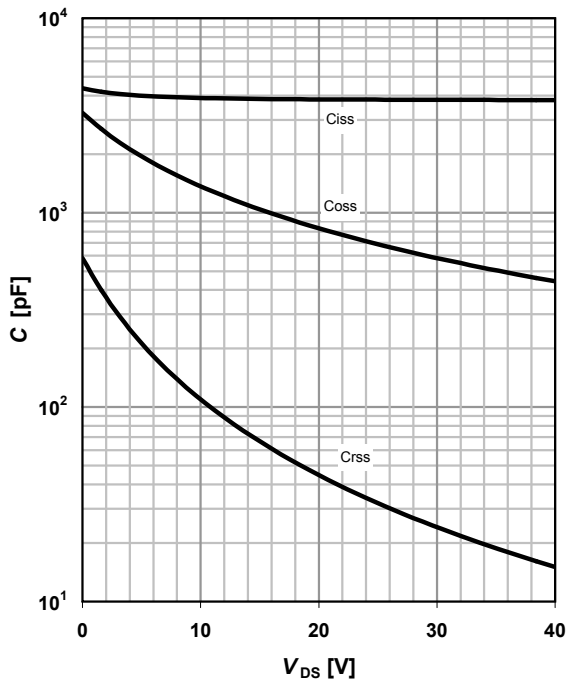
$$R_{DS(on)} = f(T_j); I_D = 20 \text{ A}; V_{GS} = 10 \text{ V}$$


**10 Typ. gate threshold voltage**

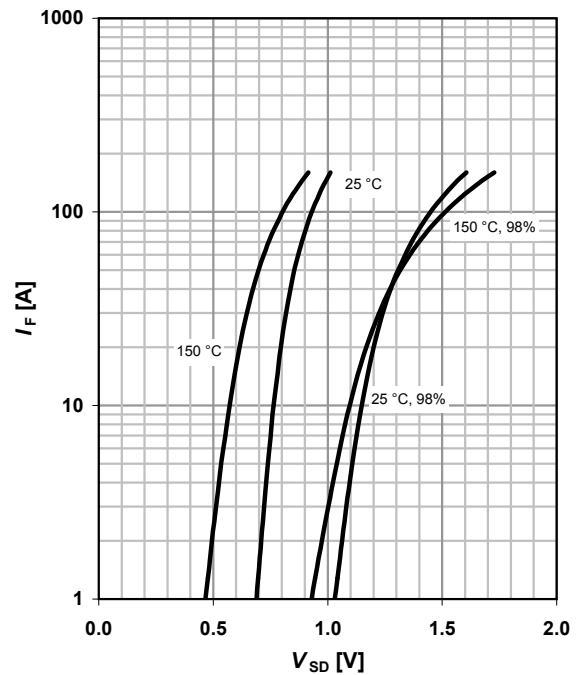
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}; I_D = 36 \mu\text{A}$$


**11 Typ. capacitances**

$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$


**12 Forward characteristics of reverse diode**

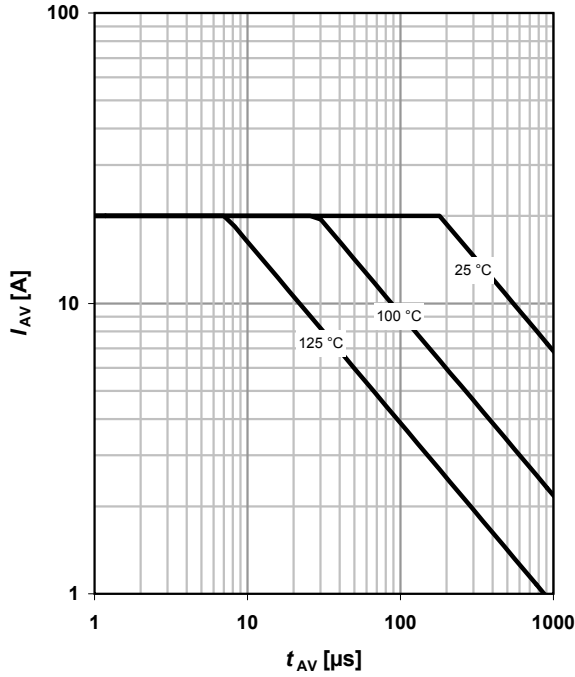
$$I_F = f(V_{SD})$$

 parameter:  $T_j$ 


**13 Avalanche characteristics**

$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$

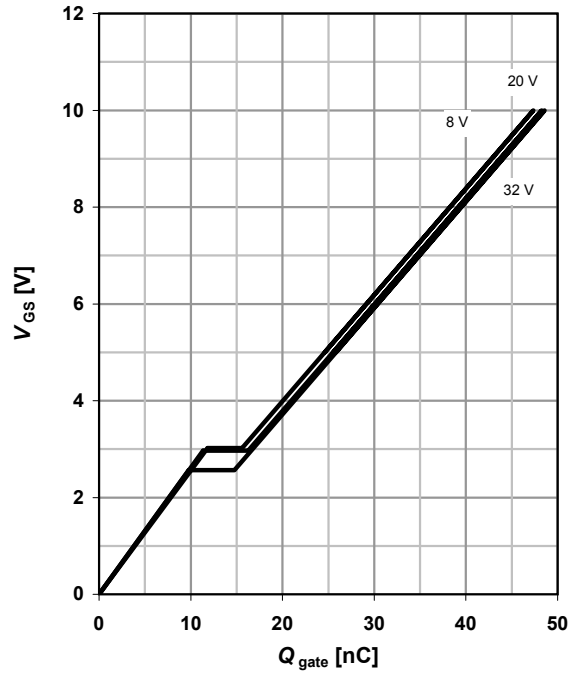
parameter:  $T_{j(start)}$



**14 Typ. gate charge**

$V_{GS}=f(Q_{gate}); I_D=20 \text{ A pulsed}$

parameter:  $V_{DD}$



**15 Drain-source breakdown voltage**

$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

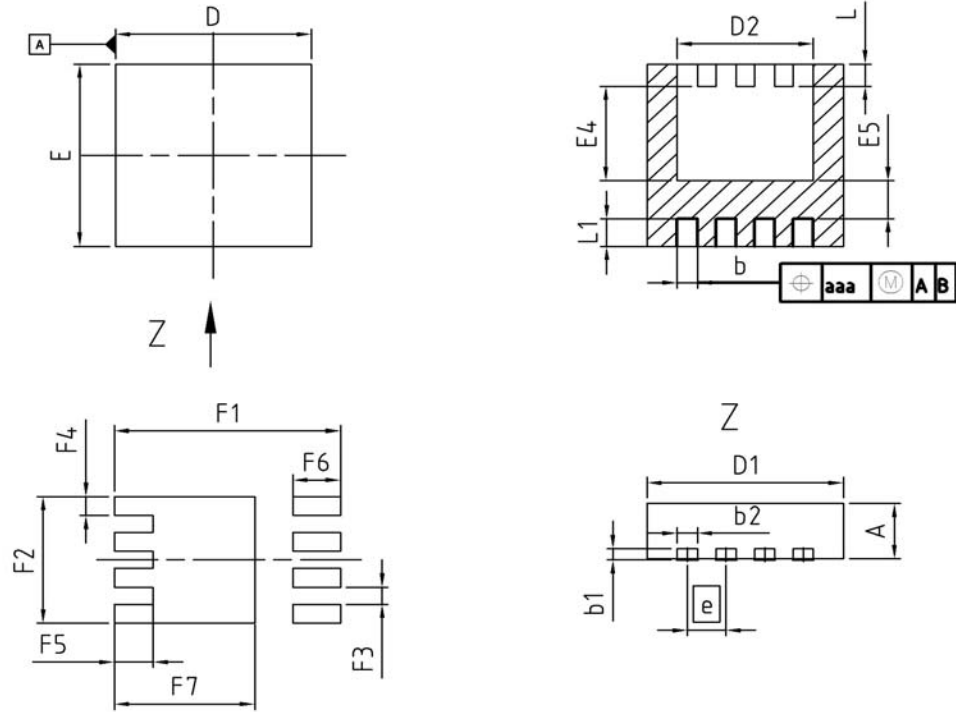


**16 Gate charge waveforms**



Package Outline

PG-TSDSON-8



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.90	1.10	0.035	0.043
b	0.24	0.44	0.009	0.017
b1	0.10	0.30	0.004	0.012
b2	0.20	0.44	0.008	0.017
D=D1	3.20	3.40	0.126	0.134
D2	2.15	2.45	0.085	0.096
E	3.20	3.40	0.126	0.134
E4	1.60	1.81	0.063	0.071
E5	0.59	0.86	0.023	0.034
e	0.65		0.026	
N	8		8	
L	0.30	0.56	0.012	0.022
L1	0.33	0.60	0.013	0.024
aaa	0.25		0.010	
F1	3.80		0.150	
F2	2.29		0.090	
F3	0.31		0.012	
F4	0.34		0.013	
F5	0.65		0.026	
F6	0.80		0.031	
F7	2.36		0.093	

DOCUMENT NO.  
Z8B00131645

SCALE

EUROPEAN PROJECTION

ISSUE DATE  
17-09-2008

REVISION  
02



**Published by**  
**Infineon Technologies AG**  
**81726 Munich, Germany**  
**© 2009 Infineon Technologies AG**  
**All Rights Reserved.**

**Legal Disclaimer**

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

**Information**

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office [www.infineon.com](http://www.infineon.com).

**Warnings**

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.