Z86K15

KEYBOARD CONTROLLER

PRODUCT SPECIFICATION

PS004301-PER0100

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1 ARCHITECTURAL OVERVIEW

The Z86K15 Keyboard Controller is a full-featured member of the Z8® MCU family, offering a unique register-to-register architecture that avoids accumulator bottlenecks. The Z86K15 is more code-efficient than RISC processors.

For keyboard applications demanding powerful I/O capabilities, the Z86K15 provides 32 pins dedicated to input and output for row, column, clock, data, and LEDs.

An on-chip counter/timer is available to relieve the system of administering real-time tasks.

5 different internal or external interrupt sources are maskable and prioritized to provide a vectored address for efficient interrupt subroutine handling and multi-tasking functions.

The Z86K15 achieves low EMI by means of several modifications in the clock circuitry and output drivers.

1.1 Z86K15 KEYBOARD CONTROLLER FEATURES

Table 1 lists the features of the Z86K15 Keyboard Controller.

TABLE 1. Z86K15 KEYBOARD CONTROLLER FEATURES

Device	ROM (KB)	I/O Lines	Speed (MHz)	Pin Count/Package
Z86K15	4	32	3–5	40-Pin DIP, 44-Pin PLCC, Chip On Board

- 4.5 V to 5.5 V Operating Range
- 0ºC to +70ºC Operating Temperature Range
- 188 Bytes of RAM
- Low Power Consumption: 40 mW @ 5 MHz
- 5 Vectored, Priority Interrupts from 5 Different Sources
- Programmable 8-Bit Counter/Timer, with 6-Bit Programmable Prescaler
- Power-On Reset (POR) Timer, Hardware Watch-Dog Timer (WDT)
- Digital-Input CMOS Levels with Internal Pull-Up Resistors
- 4 Direct-Connect LED Drive Ports
- On-Chip RC Oscillator
- Low System EMI Emission
- Z86E15 Emulation OTP

Power connections follow the conventional descriptions outlined in Table 2.

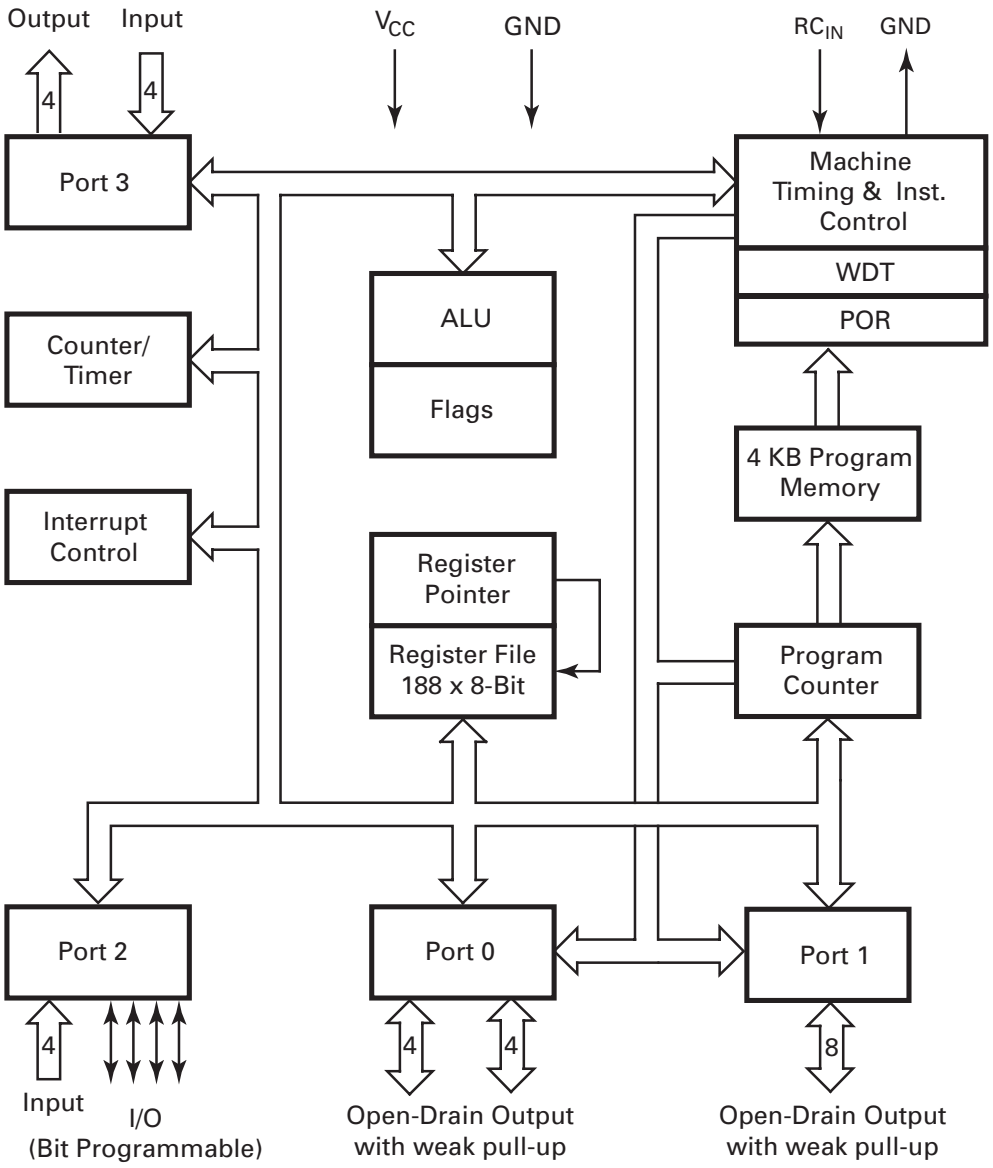
TABLE 2. POWER CONNECTIONS

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

1.2 FUNCTIONAL BLOCK DIAGRAM

Figure 1 illustrates the functional block layout of the Z86K15 Keyboard Controller.

FIGURE 1. Z86K15 FUNCTIONAL BLOCK DIAGRAM



2 PIN DESCRIPTION

Figure 2 illustrates the 40-pin DIP configuration for the Z86K15 Keyboard Controller and Table 3 describes the pin functions.

FIGURE 2. 40-PIN DIP CONFIGURATION

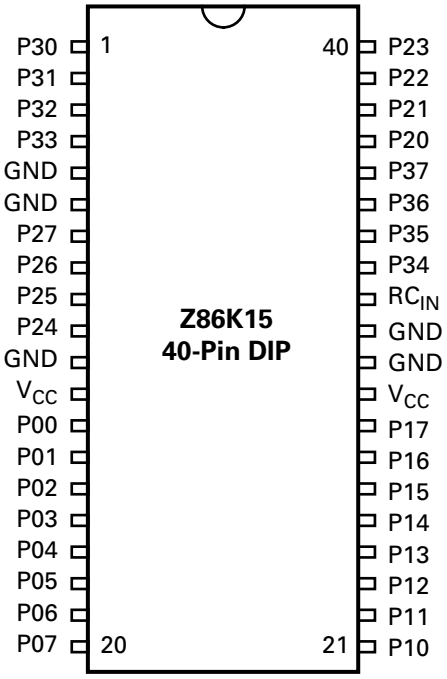


TABLE 3. 40-PIN DIP PIN IDENTIFICATION

Pin #	Symbol	Function	Direction
1–4	P30–P33	Port 3, Pins 0,1,2,3	Input
5–6	GND	Ground	
7–10	P27–P24	Port 2, Pins 7,6,5,4	In/Output
11	GND	Ground	
12	V_{CC}	Power Supply	Power
13–20	P00–P07	Port 0, Pins 0,1,2,3,4,5,6,7	Output
21–28	P10–P17	Port 1, Pins 0,1,2,3,4,5,6,7	Output
29	V_{CC}	Power Supply	Power
30	GND	Ground	
31	GND	Ground	
32	RC_{IN}	RC_{IN}	Input
33–36	P34–P37	Port 3, Pins 4,5,6,7	Output
37–40	P20–P23	Port 2, Pins 0,1,2,3	Input

Figure 3 illustrates the 44-pin PLCC configuration and Table 4 describes the pin functions.

FIGURE 3. 44-PIN PLCC CONFIGURATION

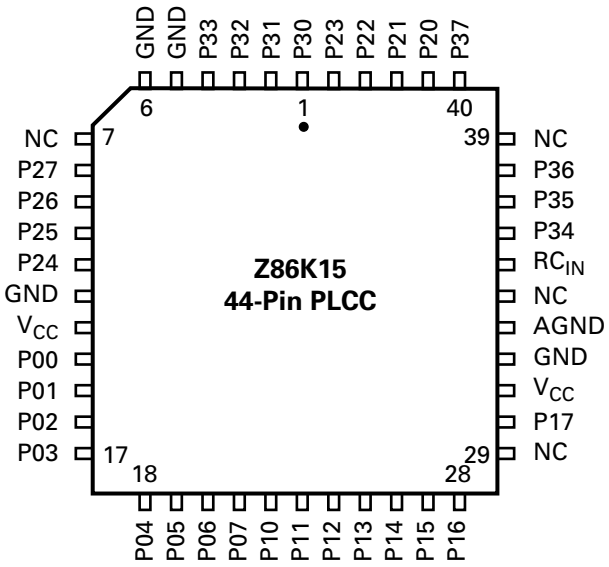


TABLE 4. 44-PIN PLCC PIN IDENTIFICATION

Pin #	Symbol	Function	Direction
1–4	P30–P33	Port 3, Pins 0,1,2,3	Input
5–7	GND	Test Pins—Ground	
8–11	P27–P24	Port 2, Pins 4,5,6,7	In/Output
12	GND	Ground	
13	V_{CC}	Power Supply	Power
14–21	P00–P07	Port 0, Pins 0,1,2,3,4,5,6,7	Output
22–28	P10–P16	Port 1, Pins 0,1,2,3,4,5,6	Output
29	NC	Not Connected	
30	P17	Port 1, Pin 7	Output
31	V_{CC}	Power Supply	Power
32	GND	Ground	
33	AGND	Ground	
34	NC	Not Connected	
35	RC_{IN}	RC_{IN}	Input
36–38	P34–P36	Port 3, Pins 4,5,6	Output
39	NC	Not Connected	
40	P37	Port 3, Pin 7	Output
41–44	P20–P23	Port 2, Pins 0,1,2,3	In/Output

3 ELECTRICAL CHARACTERISTICS

3.1 ABSOLUTE MAXIMUM RATINGS

Table 5 provides Absolute Maximum Ratings for the Z86K15 Keyboard Controller.

TABLE 5. ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage*	–0.3	+7.0	V
T_{STG}	Storage Temp	–65	+150	°C
I_A	Operating Ambient Temperature	0	+105	°C

NOTE: *Voltage on all pins with respect to GND.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

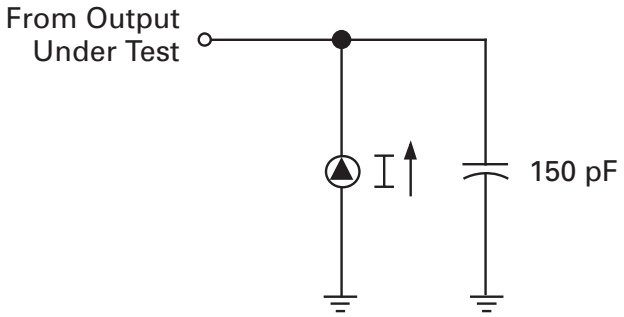
Total power dissipation should not exceed 1.21 W for the package. Power dissipation is calculated as follows:

$$\text{Total Power Dissipation} = V_{DD} \times [I_{DD} - (\text{sum of } I_{OH}), + \text{sum of } [(V_{DD} - V_{OH}) \times I_{OH}] + \text{sum of } (V_{OL} \times I_{OL})$$

3.2 STANDARD TEST CONDITIONS

The characteristics listed here apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 4).

FIGURE 4. TEST LOAD DIAGRAM



3.3 CAPACITANCE

T_A = 25ºC; V_{CC} = GND = 0 V; f = 1.0 MHz; unmeasured pins returned to GND (see Table 6).

TABLE 6. CAPACITANCE

Parameter	Max
Input Capacitance	12 pF
Output Capacitance	12 pF
I/O Capacitance	12 pF

3.4 DC CHARACTERISTICS

Table 7 provides Direct Current characteristics for the Z86K15 Keyboard Controller.

TABLE 7. DC CHARACTERISTICS

Sym	Parameter	Min	Max	Unit	Condition
V_{CH}	Clock Input High Voltage	0.7 V_{CC}	V_{CC} + 0.3 V	V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	GND –0.3	0.2 V_{CC}	V	Driven by External Clock Generator
V_{IH}	Input High Voltage	0.7 V_{CC}	V_{CC} + 0.3	V	
V_{IL}	Input Low Voltage	GND – 0.3	0.2 V_{CC}	V	
V_{OH}	Output High Voltage	V_{CC} – 0.4		V	I_{OH} = –2.0 mA
V_{OH}	Output High Voltage	V_{CC} – 0.6		V	I_{OH} = –2.0 mA[1]
V_{OL}	Output Low Voltage		.4	V	I_{OL} = 4 mA
V_{OL}	Output Low Voltage		.8	V	I_{OL} = 4 mA[1]
I_{OL}	Output Low Current	10	20	mA	V_{OL} = V_{CC} –2.2 V[1,2]
I_{OL}	Output Leakage Current	–1	1	µA	V_{IN} = 0 V, 5.25 V
I_{CC}	V_{CC} Supply Current		8	mA	@ 5.0 MHz
I_{CC1}	Halt Mode Current		3	mA	@ 5.0 MHz
I_{CC2}	Stop Mode Current		60	µA	
R_P	Pull-Up Resistor	6.76	14.04	KΩ	
R_P	Pull-Up Resistor (P26–P27)	1.8	3	KΩ	

NOTES:
1. V_{CC} = 5.0 V ± 10% @ 0°C to + 70°C.
2. Ports P37–P34. These may be used for LEDs or as general-purpose outputs requiring high sink current.\

3.5 AC ELECTRICAL CHARACTERISTICS

The ambient temperature (T_A) range for the Z86K15 Keyboard Controller's alternating current (AC) characteristics is 0ºC to 70ºC, at 5 MHz (Table 8).

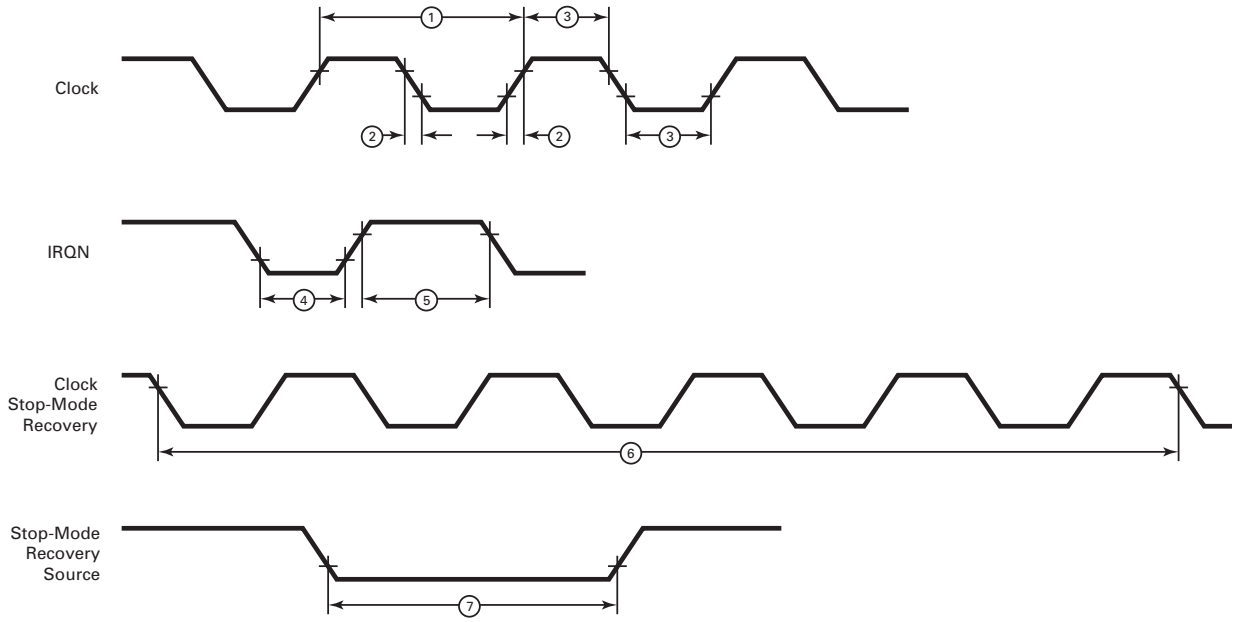
TABLE 8. AC ELECTRICAL CHARACTERISTICS

No	Symbol	Parameter	V_{CC}	Min	Max	Units	Notes
1	TpC	Input Clock Period	5.0 V	200	333	ns	1
2	TrC, TfC	Clock Input Rise & Fall Times	5.0 V		25	ns	1
3	TwC	Input Clock Width	5.0 V	37		ns	1
4	TwIL	Interrupt Request Low Time	5.0 V	3TpC			1,2
5	TwIH	Interrupt Request Input High Time	5.0 V	3TpC			1,3
6	Tost	Oscillator Start-Up Time	5.0 V		5TpC		4
7	Twsm	Stop-Mode Recovery Width Spec	5.0 V	5TpC		ns	
8	Twdt	Watch-Dog Timer Delay Time	5.0 V	53		ms	
9	Tpor	Power-On Reset	5.0 V	50	200	ms	

NOTES:
1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P30).
3. Interrupt request through Port 3 (P31–P33).
4. After Stop-Mode Recovery.

Additional timing characteristics of the Z86K15 are illustrated in Figure 5.

FIGURE 5. ADDITIONAL TIMING

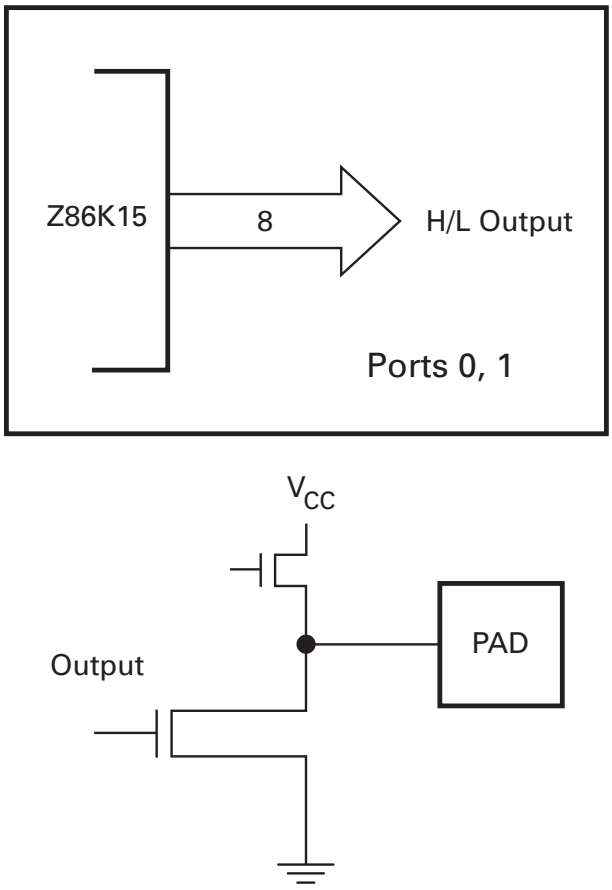


4 PIN FUNCTIONS

Port 0 (P07–P00). Port 0 is an 8-bit, CMOS-compatible, high-impedance pull-up/ low-impedance pull-down output (Figure 6).

Port 1 (P17–P10). Port 1 is an 8-bit, CMOS-compatible, high-impedance pull-up/ low-impedance pull-down output port (Figure 6).

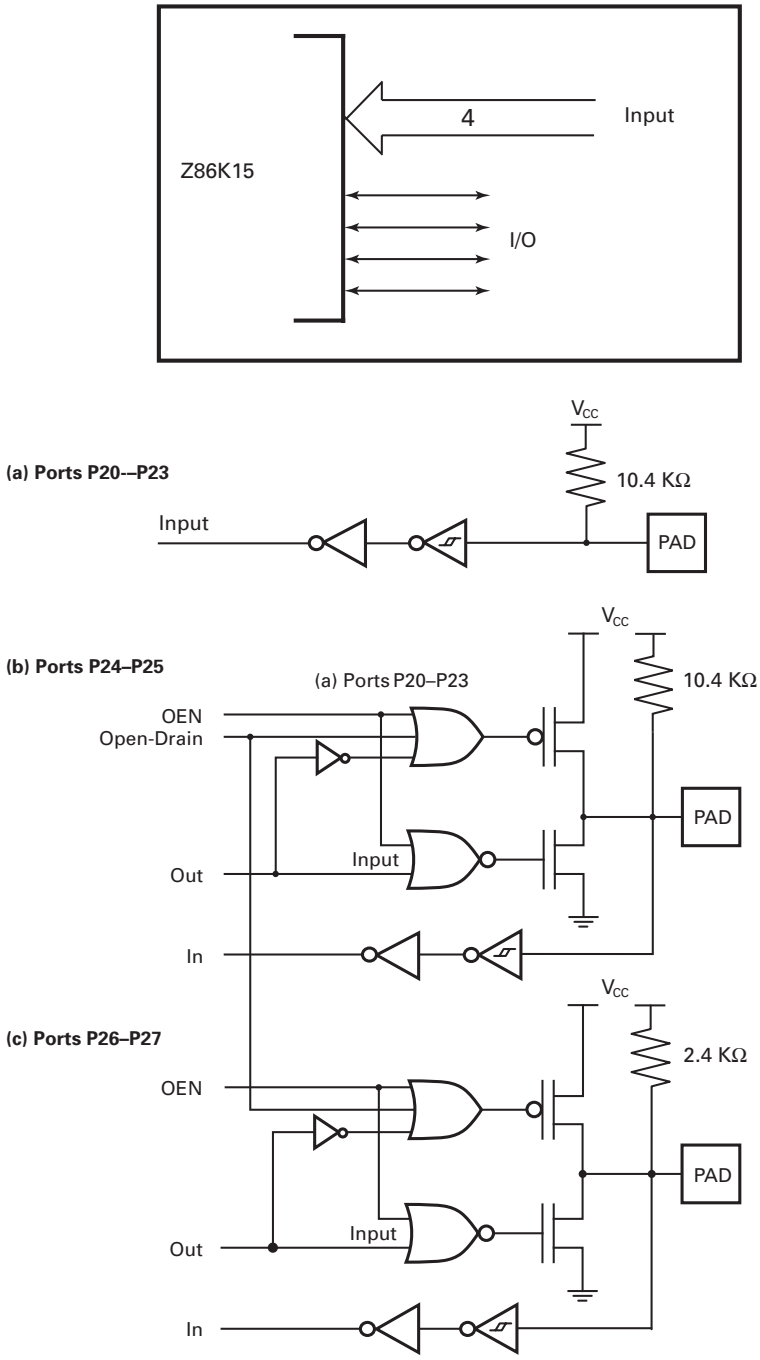
FIGURE 6. PORTS 0 AND 1 CONFIGURATION



Port 2 (P27–P20). Port 2 is an 8-bit CMOS-compatible Port with 4-bit input and 4-bit programmable I/O (Figure 7). P20–P25 feature 10.4-KΩ (±35%) pull-up resistors. P26–P27 feature 2.4-KΩ (±25%) pull-up resistors.

NOTE: Only 1 bit is used to program all 4 bits of $P2_{OUT}$ (P24–P27; Open-Drain/Push-Pull). To meet keyboard application requirements, all 4 bits are open-drain.

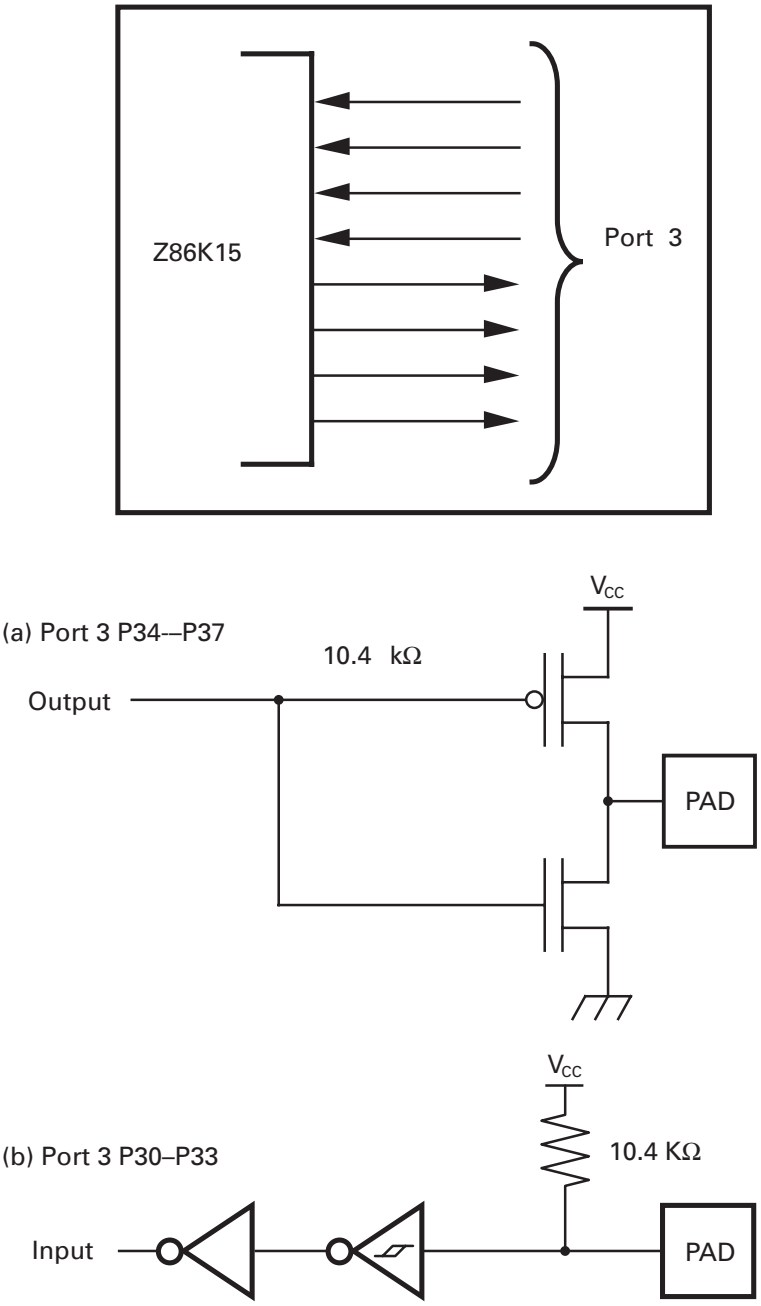
FIGURE 7. PORT 2 CONFIGURATION



Port 3 (P37–P30). Port 3 is an 8-bit, CMOS-compatible 4-fixed input (P33–P30) and 4-fixed output (P37–P34) I/O port. Port 3 inputs feature 10.4-KΩ pull-up resistors. Outputs are capable of directly driving LEDs. See Figure 8.

Port 3 is configured under software control to provide 4 external interrupt request signals (IRQ0–IRQ3).

FIGURE 8. PORT 3 CONFIGURATION



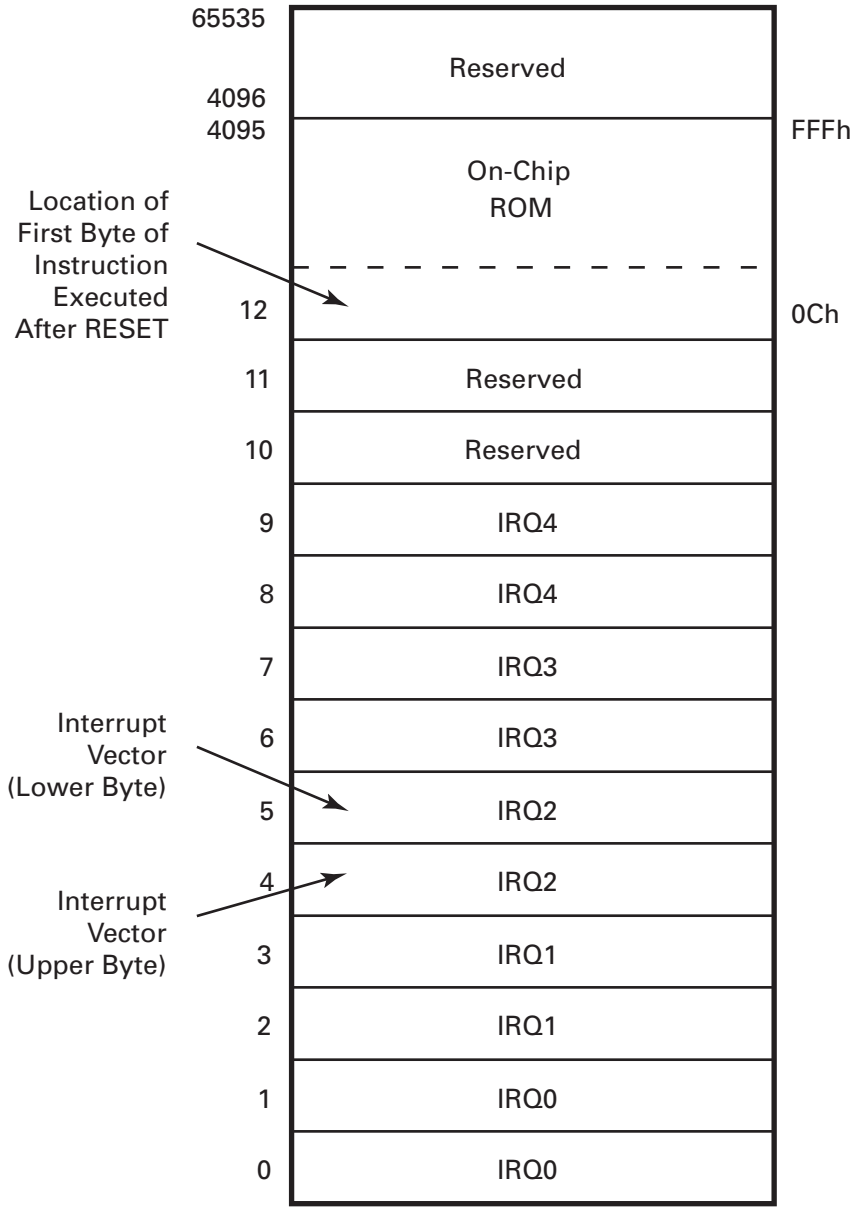
5 FUNCTIONAL DESCRIPTION

Program Memory. The 12-bit program counter addresses 4 KB of internal program memory space (Figure 9).

The first 12 bytes of program memory are reserved for the interrupt vectors. These locations provide six 16-bit vectors that correspond to the 5 available interrupts.

Byte 12 to byte 4095 consist of on-chip, mask-programmed ROM. Addresses 4096 and greater are reserved.

FIGURE 9. PROGRAM MEMORY MAP



Register File. The register file (Figure 10) consists of 4 I/O port registers, 188 general-purpose registers, and 11 control and status registers (R3–R0, R191–R4, and R255–R240, respectively). The instructions can access registers directly or indirectly through an 8-bit address field. This access allows short, 4-bit register addressing using the Register Pointer (Table 9). In the 4-bit mode, the register file is divided into 13 working-register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group.

For the complete Register File Assignment, refer to Figure 10.

FIGURE 10. REGISTER FILE CONFIGURATION

LOCATION		IDENTIFIERS
R255	Stack Pointer (Bits 7-0)	SPL
R254	Reserved	
R253	Register Pointer	RP
R252	Program Control Flags	FLAGS
R251	Interrupt Mask Register	IMR
R250	Interrupt Request Register	IRQ
R249	Interrupt Priority Register	IPR
R248	Reserved	
R247	Port 2OP*	P2P
R246	Port 2 DIR*	P2D
R245	T0 Prescaler	PREQ
R244	Timer/Counter0	T0
R243	Reserved	
R242	Reserved	
R241	Timer Mode	TMR
R240	Reserved	
	Not Implemented	
R191	General-Purpose Registers	
R4		
R3	Port 3	P3
R2	Port 2	P2
R1	Port 1	P1
R0	Port 0	P0

Note: *Does not reset with a Stop-Mode Recovery.

TABLE 9. REGISTER POINTER—R253 (FDH: READ/WRITE)

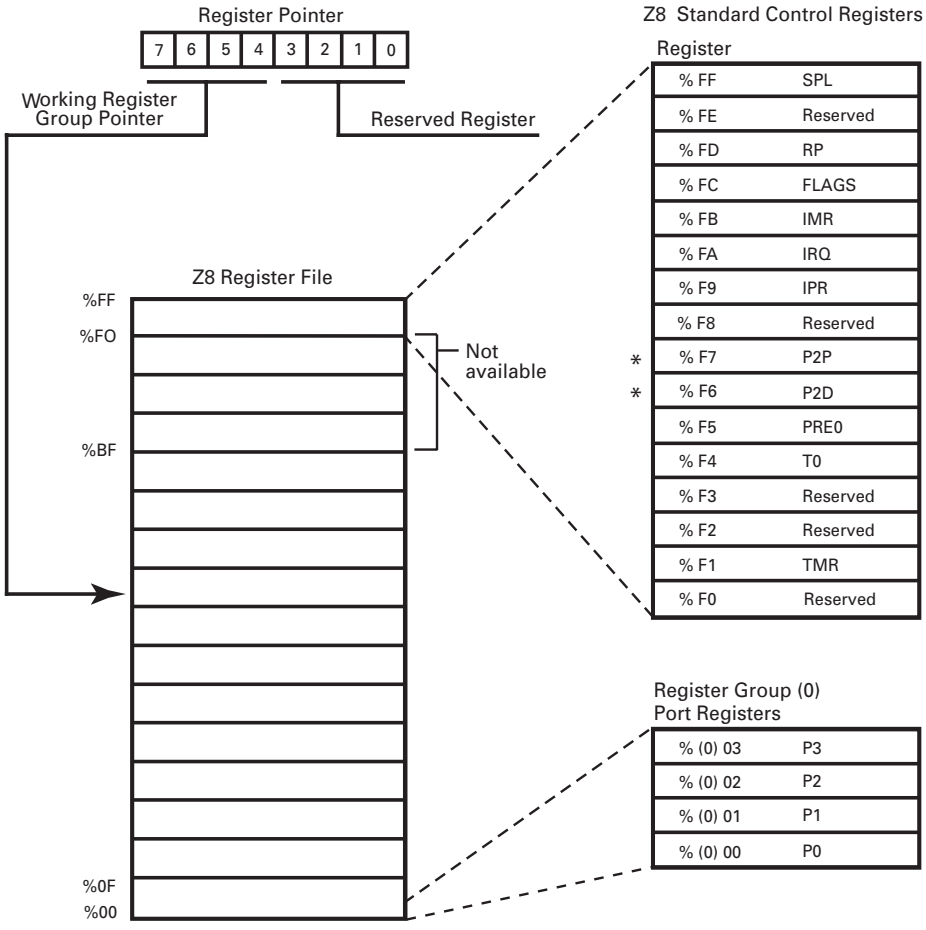
Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W				
Reset	0	0	0	0	X	X	X	X

NOTE: R = Read, W = Write, X = Indeterminate.

Bit Position	Bit Field	R/W	Reset Value	Description
D7	r7	R/W	0	Register Pointer
D6	r6	R/W	0	Register Pointer
D5	r5	R/W	0	Register Pointer
D4	r4	R/W	0	Register Pointer
D3–D0	Reserved		X	Reserved; must be 0

The complete Register File Architecture is illustrated in Figure 11.

FIGURE 11. REGISTER FILE ARCHITECTURE



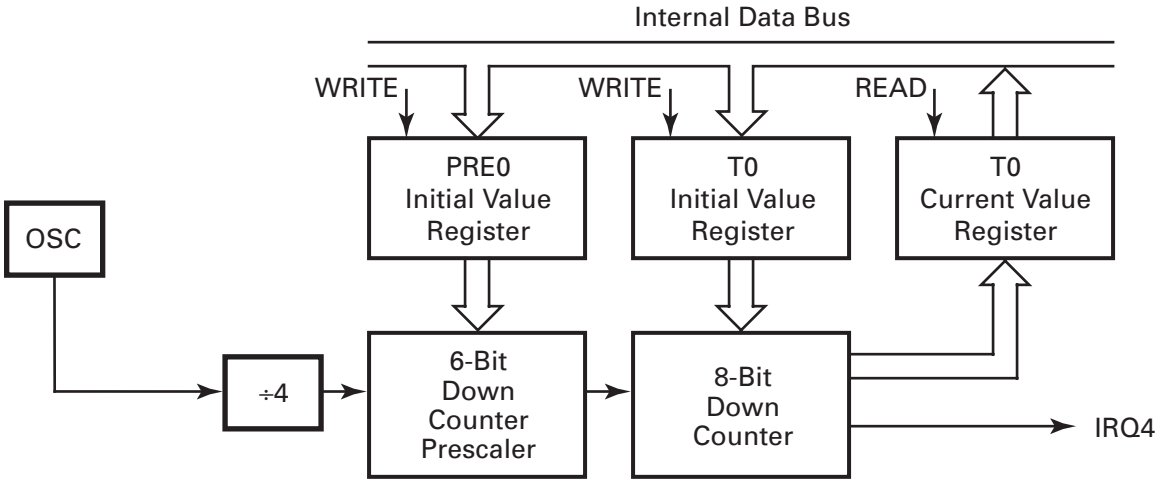
Note: *Does not reset with a Stop-Mode Recovery.

Counter/Timers. There is an 8-bit programmable counter/timer (T0) driven by its own 6-bit programmable prescaler (Figure 12).

The 6-bit prescaler can divide the input frequency of the clock by any integer number from 1 to 64. The prescaler drives its counter, which decrements the value (1 to 256) on the prescaler overflow. When both the counter and prescaler reach the end of count, a timer interrupt request, IRQ4, is generated.

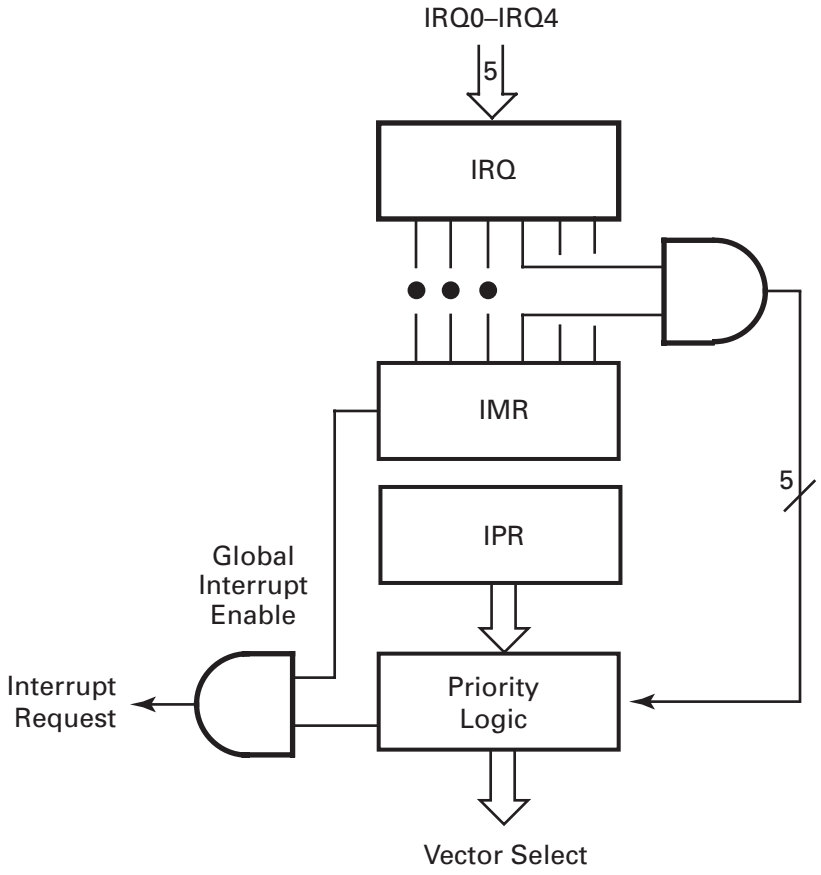
The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counter can also be programmed to stop upon reaching zero (SINGLE PASS mode) or to automatically reload the initial value and continue counting (MODULO-N CONTINUOUS mode) The counter, but not the prescaler, can be read at any time without disturbing its value or COUNT mode.

FIGURE 12. COUNTER/TIMERS BLOCK DIAGRAM



Interrupts. The Z86K15 features 5 different interrupts from 5 different sources. These interrupts are maskable and prioritized (Figure 13). The 5 sources are divided as follows: 4 sources are claimed by Port 3 lines P33–P30, and the other is claimed by the counter/timer. The Interrupt Mask Register globally or individually enables or disables the 5 interrupt requests.

FIGURE 13. INTERRUPT BLOCK DIAGRAM



When more than 1 interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All interrupts are vectored through locations in the program memory. When an interrupt machine cycle is activated, an interrupt request is granted, thus disabling all of the subsequent interrupts. The program counter and status flags are saved. The interrupt machine cycle then branches to the program memory vector location reserved for the interrupt. This memory location and the next byte contain the 16-bit address of the interrupt service routine for this particular interrupt request.

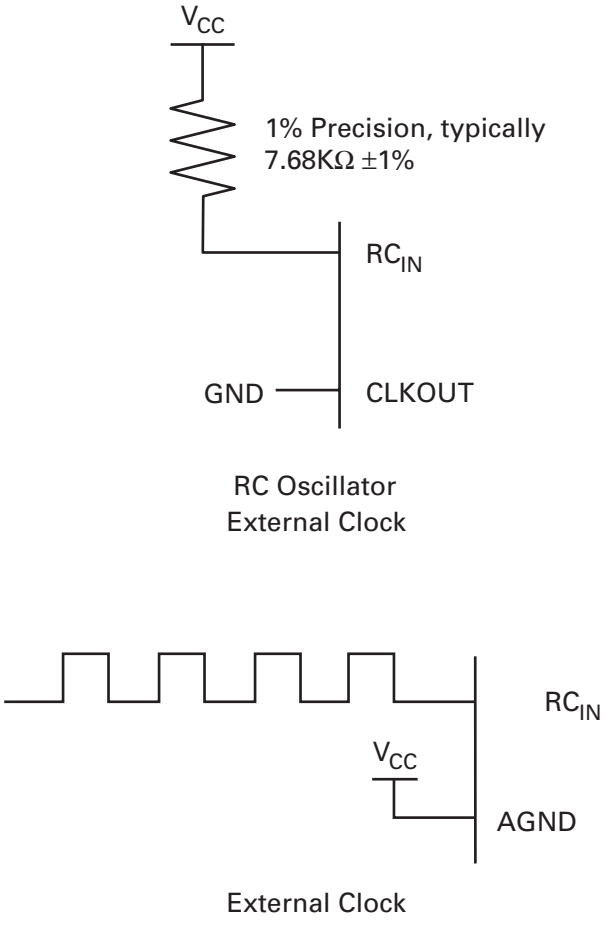
To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt request requires service.

RC Oscillator. The Z86K15 provides an internal capacitor to accommodate an RC oscillator configuration. A 1% precision resistor is necessary to achieve ±10% accurate frequency oscillation. For a nominal 4-MHz signal, use a 7.68 KΩ resistor.

RC_{IN}. A precision resistor is connected between this pin and the power supply to form the RC oscillator.

The Z86K15 also accepts an external clock from (RC_{IN}) with AGND connected to V_{CC} (Figure 14).

FIGURE 14. RC OSCILLATOR CONFIGURATIONS



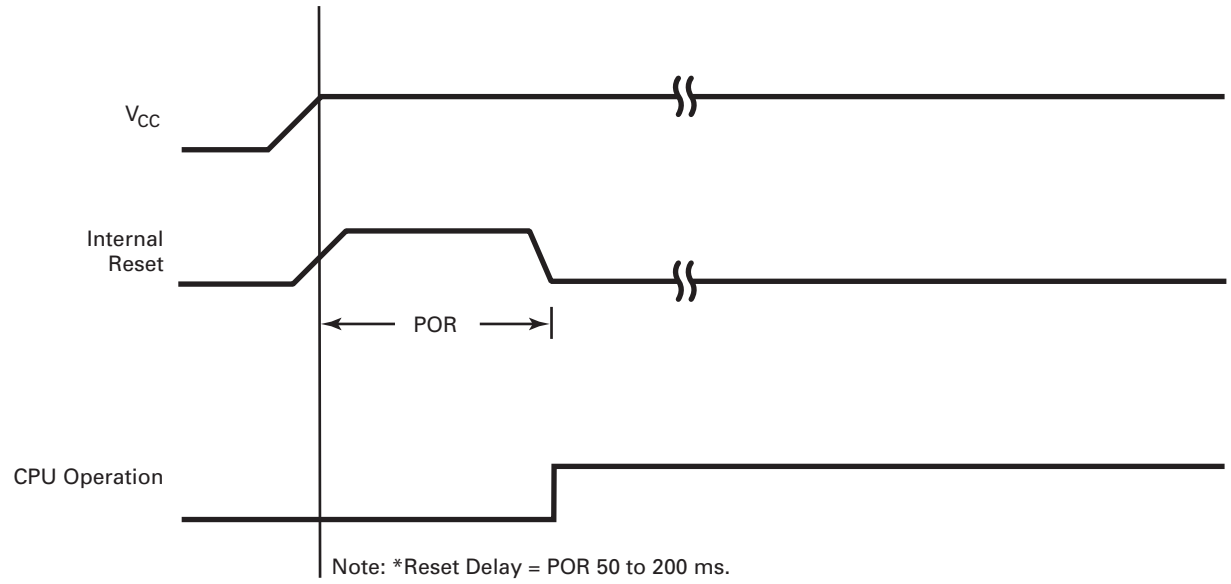
Watch-Dog Timer. The Watch-Dog Timer (WDT) is automatically activated by power-on when it is enabled in the Mask Option. The WDT is a retriggerable single-shot timer that resets the Z8 if the Z8 reaches its terminal count. The WDT is driven by the system clock. The WDT must be refreshed at least 1 time during each WDT period by executing the WDT instruction. WDT can be enabled by Mask Option (Figure 15).

WDT Hot Bit. Bit 7 of the Interrupt Request register (IRQ register FAh) determines whether a hot start or cold start occurred. A cold start is defined as reset occurring from power-up of the Z86K15 (the default upon power-up is 0). A hot start occurs after a WDT time-out (bit 7 is set to 1). Bit 7 of the IRQ register is read-only and is automatically reset to 0 when read.

Watch-Dog Timer Time-Out. The WDT time-out is 294,912 ÷ f.

WDT During HALT (D5–R250). This bit determines whether or not the WDT is active during HALT mode. The default is 1, and a 1 indicates active during HALT.

FIGURE 15. WDT TURN-ON TIMING AFTER RESET



Power-On Reset (POR). A timer circuit is triggered by the system oscillator and is used for the Power-On Reset (POR) timer function. The POR time allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins. The POR period is defined as:

$$POR = \frac{589{,}824}{f}$$

The POR timer circuit is a single-shot timer triggered by Power Fail to Power OK status. The POR time is a nominal 50 to 200 ms. The POR timer is bypassed during Stop-Mode Recovery (SMR).

HALT. HALT turns off the internal CPU clock, but not the RC oscillator. The counter/timer and external interrupts IRQ0, IRQ1, IRQ2, and IRQ3 remain active. The Z86K15 is recovered by interrupts, either externally or internally (Table 10).

STOP. This instruction turns off the internal clock and oscillator, reducing the standby current to less than 60 µA. The STOP mode is terminated by an enabled external interrupt. This termination causes the processor to restart the application program at address `000Ch` or the active external interrupt vector. In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction.

To flush the pipeline, the user must execute a NOP (`Op Code = FFh`) immediately before the appropriate sleep instruction, such as:

```
FF      NOP         ; clear the pipeline
6F      STOP        ; enter STOP mode
                    or
FF      NOP         ; clear the pipeline
7F      HALT        ; enter HALT mode
```

Bit 6 of the IRQ Registers are flags for Stop-Mode Recovery (Table 10).

TABLE 10. INTERRUPT REQUEST REGISTER—R250 IRQ (FAH: READ/WRITE)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

NOTE: R = Read, W = Write, X = Indeterminate.

Bit Position	Bit Field	R/W	Reset Value	Description
D7	WDT	R	0	Watch-Dog Timer Hot Bit 0: POR* 1: WDT Time-out
D6	STOP	R/W	0	Stop-Mode Recovery Flag 0: POR/WDT 1: Stop Recovery
D5	WDT	R/W	0	Watch-Dog Timer During HALT Mode 0: OFF* 1: ON
D4–D0	IRQ4–IRQ0	R/W	0	IRQ0 = P32 Input IRQ1 = P33 Input IRQ2 = P31 Input IRQ3 = P30 Input IRQ4 = T0

NOTE: *Upon Reset.

Cold or Warm Start (D6). This bit is set upon entering STOP mode. A 0 (cold) indicates that the device is awakened by a POR/WDT RESET. A 1 (warm) indicates that the device is awakened by a SMR source. This bit is reset when read.

A negative transition on the host data line or any of the designated row input pins recover the Z86K15 from STOP mode. See Figure 16.

FIGURE 16. STOP-MODE RECOVERY SOURCE

6 CONTROL REGISTERS

Control Register bit definitions are provided in Tables 11 through 21.

TABLE 11. TIMER MODE REGISTER—R241 TMR (F1H: READ/WRITE)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	X	X	X	X	X	X	0	0

NOTE: R = Read, W = Write, X = Indeterminate.

Bit Position	Bit Field	R/W	Reset Value	Description
D7–D2	Reserved	R/W	X	Reserved; must be 0
D1	T0 Count	R/W	0	Timer 0 Count 0: Disable T0 Count 1: Enable T0 Count
D0	T0	R/W	0	Timer0 0: No Function 1: Load T0

TABLE 12. COUNTER/TIMER 0 REGISTER—R244 T0 (F4H: READ/WRITE)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	X	X	X	X	X	X	X	X

NOTE: R = Read, W = Write, X = Indeterminate.

Bit Position	Bit Field	R/W	Reset Value	Description
D7–D0	T0 Initial Value	R/W	X	Timer0 Initial Value when WRITE; range = 1–256 decimal, 01–100 hex
	T0 Current Value	R/W	X	Timer0 Current Value when READ

TABLE 13. PRESCALER 0 REGISTER—R245 PRE0 (F5H: WRITE ONLY)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	W	W	W	W	W	W	W	W
Reset	X	X	X	X	X	X	X	X

NOTE: W = Write, X = Indeterminate.

Bit Position	Bit Field	R/W	Reset Value	Description
D7–D2	Prescaler	W	X	Prescaler Modulo; range = 1–64 decimal, 01–40 hex
D1	Reserved	W	X	Reserved; must be 0
D0	Count	W	X	COUNT Mode 0: T0 Single Pass 1: T0 Modulo N

TABLE 14. PORT 2 MODE REGISTER—R246 P2D (F6H: WRITE ONLY)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	W	W	W	W	W	W	W	W
Reset	1	1	1	1	0	0	0	0

NOTE: W = Write.

Bit Position	Bit Field	R/W	Reset Value	Description
D7–D4	P24–P27	W	1	P24–P27 I/O Definition 0: Defines bit as Output 1: Defines bit as Input
D3–D0	Reserved	W	0	Reserved; must be 0

TABLE 15. PORT 2 OPEN DRAIN MODE REGISTER—R247 P2P (F7H: WRITE ONLY)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	X

NOTE: W = Write, X = Indeterminate.

Bit Position	Bit Field	R/W	Reset Value	Description
D7–D1	Reserved	W	0	Reserved; must be 0
D0	P24–P27	W		0: P24–P27 Open-Drain* 1: P24–P27 Push-Pull

NOTE: Must be open-drain to satisfy PS/2 operation.

TABLE 16. INTERRUPT PRIORITY REGISTER—R249 IPR (F9H: WRITE ONLY)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	W	W	W	W	W	W	W	W
Reset	X	X	X	X	X	X	X	X

NOTE: W = Write, X = Indeterminate.

Bit Position	Bit Field	R/W	Reset Value	Description
D7–D6	Reserved	W	X	Reserved; must be 0
D5	Reserved	W	X	Reserved
D4–D3, D0	Interrupt	W	X	Interrupt Group Priority Reserved = 000 C > A > B = 001 A > B > C = 010 A > C > B = 011 B > C > A = 100 C > B > A = 101 B > A > C = 110 Reserved = 111
D2	IRQ0, IRQ4	W	X	IRQ0, IRQ4 Priority (Group C) 0: IRQ1 > IRQ4 1: IRQ4 > IRQ1
D1	IRQ0, IRQ2	W	X	IRQ0, IRQ2 Priority (Group B) 0: IRQ2 > IRQ0 1: IRQ0 > IRQ2

TABLE 17. INTERRUPT REQUEST REGISTER—R250 IRQ (FAH: READ/WRITE)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

NOTE: R = Read, W = Write.

Bit Position	Bit Field	R/W	Reset Value	Description
D7	WDT	R	0	Watch-Dog Timer Hot Bit 0: POR* 1: WDT Time-out
D6	STOP	R/W	0	Stop Flag 0: POR/WDT 1: Stop-Mode Recovery
D5	STOP	R/W	0	Stop Delay 0: OFF* 1: ON
D4–D0	IRQ4–IRQ0	R/W	0	IRQ0 = P32 Input IRQ1 = P33 Input IRQ2 = P31 Input IRQ3 = P30 Input IRQ4 = T0

NOTE: Upon Reset.

TABLE 18. INTERRUPT MASK REGISTER—R251 IMR (FBH: READ/WRITE)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	X	X	0	0	0	0	0

NOTE: R = Read, W = Write, X = Indeterminate.

Bit Position	Bit Field	R/W	Reset Value	Description
D7	Interrupt	R/W	0	1: Enables Interrupts
D6–D5	Reserved	R/W	X	Reserved; must be 0
D4–D0	IRQ4–IRQ0	R/W	0	1: Enables IRQ0–IRQ4; D0 = IRQ0

TABLE 19. FLAG REGISTER—R252 (FCH: READ/WRITE)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

NOTE: R = Read, W = Write.

Bit Position	Bit Field	R/W	Reset Value	Description
D7		R/W	0	Carry Flag
D6		R/W	0	Zero Flag
D5		R/W	0	Sign Flag
D4		R/W	0	Overflow Flag
D3		R/W	0	Decimal Adjust Flag
D2		R/W	0	Half Carry Flag
D1		R/W	0	User Flag F2
D0		R/W	0	User Flag F1

TABLE 20. REGISTER POINTER—R253 (FDH: READ/WRITE)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	X	X	X	X

NOTE: R = Read, W = Write, X = Indeterminate.

Bit Position	Bit Field	R/W	Reset Value	Description
D7	r7	R/W	0	Register Pointer
D6	r6	R/W	0	Register Pointer
D5	r5	R/W	0	Register Pointer
D4	r4	R/W	0	Register Pointer
D3–D0	Reserved	R/W	X	Reserved; must be 0

TABLE 21. STACK POINTER—R255 (FFH: READ/WRITE)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	X	X	X	X	X	X	X	X

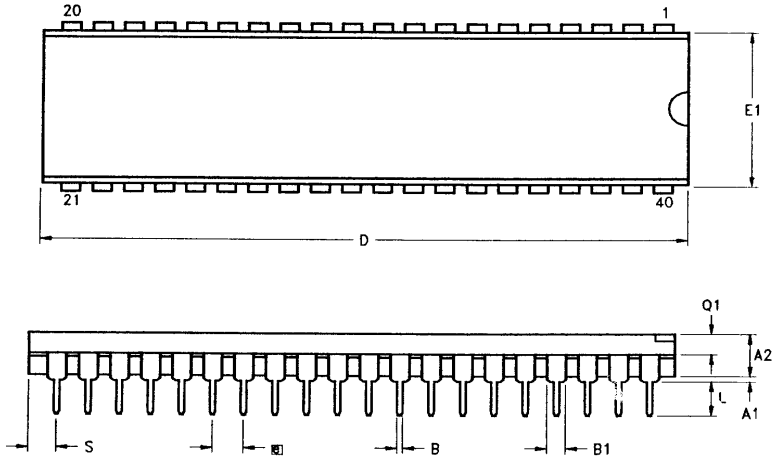
NOTE: R = Read, W = Write, X = Indeterminate.

Bit Position	Bit Field	R/W	Reset Value	Description
D7–D0	SP0–SP7	R/W	X	Stack Pointer

7 PACKAGE INFORMATION

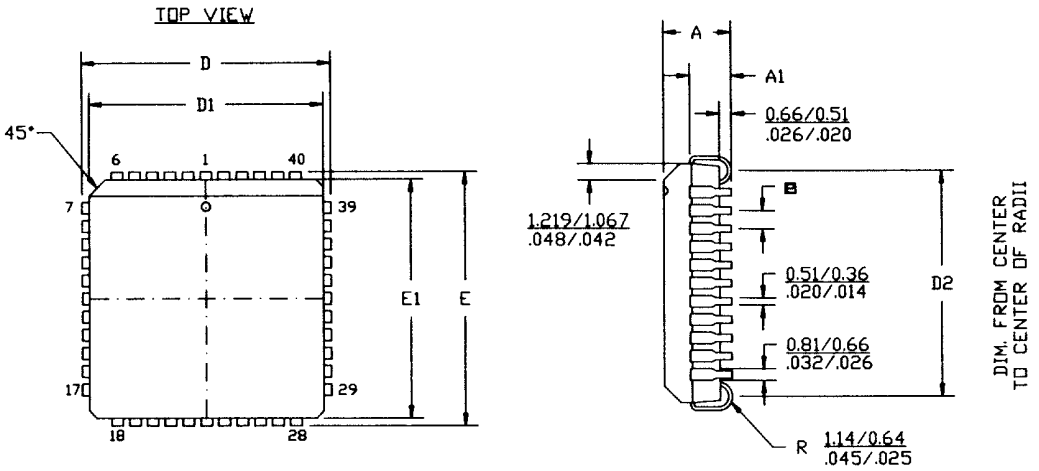
Figures 17 and 18 illustrate the 40-pin DIP and the 44-pin PLCC packages, respectively.

FIGURE 17. 40-PIN DIP PACKAGE DIAGRAM



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	1.02	.020	.040
A2	3.18	3.94	.125	.155
B	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
C	0.23	0.38	.009	.015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	.535	.560
e	2.54 TYP		.100 TYP	
eA	15.49	16.76	.610	.660
L	3.05	3.81	.120	.150
Q1	1.52	1.91	.060	.075
S	1.52	2.29	.060	.090

FIGURE 18. 44-PIN PLCC PACKAGE DIAGRAM



NOTES:

1. CONTROLLING DIMENSIONS : INCH
2. LEADS ARE COPLANAR WITHIN .004 IN.
3. DIMENSION : MM / INCH

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.27	4.57	.168	.180
A1	2.41	2.92	.095	.115
D/E	17.40	17.65	.685	.695
D1/E1	16.51	16.66	.650	.656
D2	15.24	16.00	.600	.630
e	1.27 TYP		.050 TYP	

8 ORDERING INFORMATION

Ordering Information for the Z86K15 Keyboard Controller is provided in Table 22.

TABLE 22. ORDERING INFORMATION

Part	PSI	Description
Z86K15	Z86K1505PSC	40-Pin DIP, 5 MHz, Standard Temperature
	Z86K1505VSC	44-Pin PLCC, 5 MHz, Standard Temperature

8.1 PART NUMBER DESCRIPTION

ZiLOG part numbers consist of a number of components, as indicated in Tables 23 and 24:

TABLE 23. PART NUMBER DESCRIPTION

Z	ZiLOG prefix
86K15	Product Number
05	Speed
P	Package
S	Temperature
C	Environmental Flow

TABLE 24. PACKAGE DESCRIPTION

Preferred Package	P = Plastic DIP
	V = Plastic Chip Carrier
Preferred Temperature	S = 0°C to +70°C
Speed	5 = 5 MHz
Environmental	C = Plastic Standard

EXAMPLE: Part number Z86K1505PSC is a Z86K15 MCU, a 5-MHz dual-inline package with 0ºC to +70ºC temperature range and Plastic Standard environmental flow.

For fast results, contact your local ZiLOG sales office for assistance in ordering the part required.

9 DOCUMENT INFORMATION

9.1 DOCUMENT NUMBER DESCRIPTION

The Document Control Number that appears in the footer of each page of this document contains unique identifying attributes, as indicated in the following table:

PS	Product Specification
0043	Unique Document Number
01	Revision Number
PER	Business Channel
0100	Month and Year Published

9.2 CHANGE LOG

Rev	Date	Purpose	By
01	01/00	Original issue	J. Irwin

CUSTOMER FEEDBACK FORM

Z86K15 KEYBOARD CONTROLLER PRODUCT SPECIFICATION

If you experience any problems while operating this product, or if you note any inaccuracies while reading this Product Specification, please copy and complete this form, then mail or fax it to ZiLOG (see *Return Information*, below). We also welcome your suggestions!

CUSTOMER INFORMATION

Name	Country
Company	Phone
Address	Fax
City/State/Zip	E-Mail

PRODUCT INFORMATION

Serial # or Board Fab #/Rev. #
Software Version
Document Number
Host Computer Description/Type

RETURN INFORMATION

ZiLOG
System Test/Customer Support
910 E. Hamilton Avenue, Suite 110, MS 4–3
Campbell, CA 95008
Fax: (408) 558-8536
Email: tools@zilog.com

PROBLEM DESCRIPTION OR SUGGESTION

Provide a complete description of the problem or your suggestion. If you are reporting a specific problem, include all steps leading up to the occurrence of the problem. Attach additional pages as necessary.

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