

LTC6954

Low Phase Noise, Triple Output Clock Distribution Divider/Driver

DESCRIPTION

Demonstration Circuit 1954A features the [LTC®6954](#), a Low Phase Noise, Triple Output Clock Distribution Divider/Driver.

There are four options of the DC1954A, one for each version of the LTC6954. Table 1 summarizes the available DC1954A options.

The DC1954A LVPECL outputs are AC-coupled 50Ω transmission lines making them suitable for driving 50Ω impedance instruments. The LVDS/CMOS outputs of the DC1954A are terminated with a 100Ω differential resistor and are DC-coupled. All differential input and outputs have

0.5" spaced SMA connectors. The LTC6954's EZSync™ function is made available via a turret and an SMA connector.

A DC590 USB serial controller board is used for SPI communication with the LTC6954, controlled by the supplied LTC6954_GUI software.

Design files for this circuit board are available at <http://www.linear.com/demo/DC1954A>

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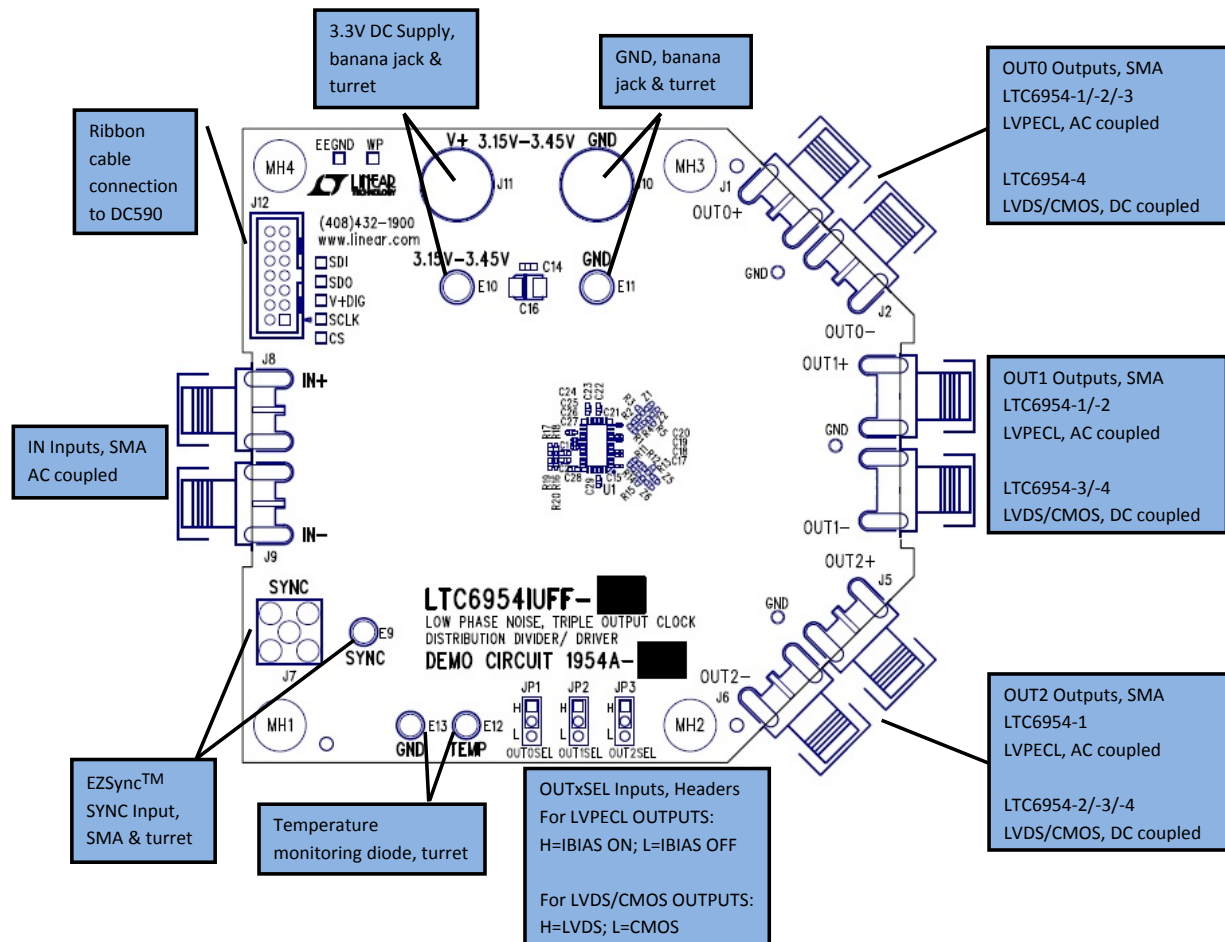


Figure 1. DC1954A Connections

DEMO MANUAL DC1954A

QUICK START PROCEDURE

The DC1954A is easy to set up to evaluate the performance of the LTC6954. Follow the procedure below.

The DC590 and LTC6954_GUI application are required to control the DC1954A through a personal computer (PC).

DC590 Configuration

Place the DC590 jumpers in the following positions (refer to Figure 2):

- JP4:** EE Must be in the EN position.
- JP5:** ISO ON must be selected.
- JP5:** SW ON must be selected.
- JP6:** VCCIO 3.3V or 5V must be selected. This sets the SPI port to 3.3V or 5V operation, 3.3V operation is recommended.

Connect the DC590 to one of your computer's USB ports with the included USB cable.

LTC6954_GUI Installation

The LTC6954_GUI software is used to communicate with the LTC6954. It uses the DC590 to translate between USB and SPI-compatible serial communications formats. The following are the LTC6954_GUI system requirements:

- Windows Operating System: Windows XP, Windows 2003 Server, Windows Vista, Windows 7
- Microsoft .NET 3.5 SP1 or later
- Windows Installer 3.1 or later
- Linear Technology's DC590 hardware

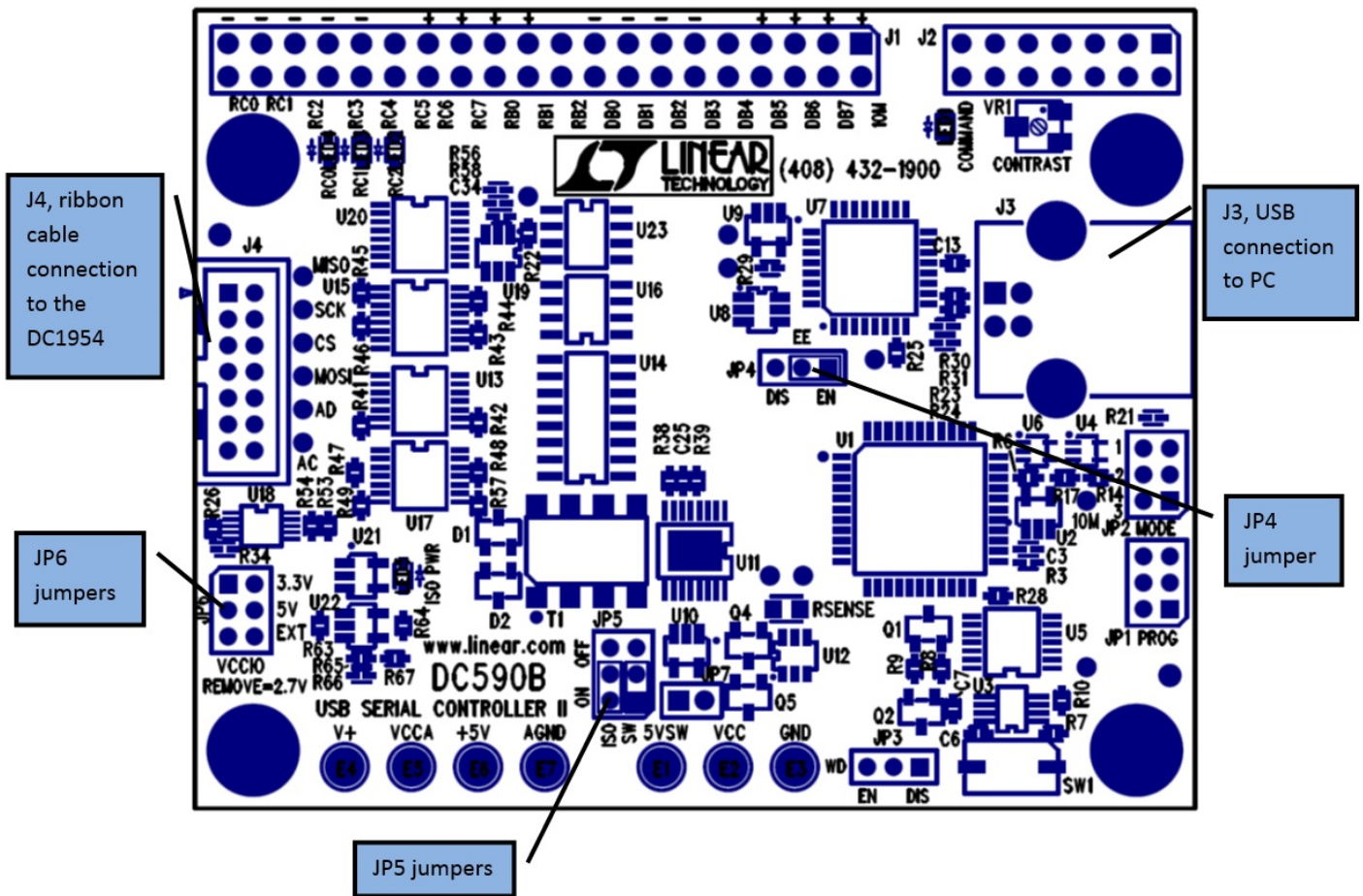


Figure 2. DC590 Jumper and Connector Locations

QUICK START PROCEDURE

Download the LTC6954_GUI setup file at:

www.linear.com/LTC6954_GUI.

Run the LTC6954_GUI setup file and follow the instructions given on the screen. The setup file will verify and/or install Microsoft .NET and install the LTC6954_GUI.

DC1954A Configuration

1. Connect the GND and V+ 3.15V-3.45V, turrets to a power supply and apply power (see Figure 1 and the Typical DC1954A Requirements and Characteristics table).
2. Connect the DC590 to the DC1954A with the provided ribbon cable.
3. Run the LTC6954_GUI application.
4. From the LTC6954_GUI, click *File -> Load Settings* and point to the LTC6954.6954set file.
5. From the LTC6954_GUI, select the Read All button. This will update the GUI to display the correct part number and associated output types.
6. Connect a low phase-noise (or jitter) single-ended or differential signal to IN+ (J8) and/or IN- (J9). Refer to the LTC6954 data sheet for acceptable input frequencies and amplitudes.
7. From the LTC6954_GUI, update Fin to the frequency of the input signal in step 6. This will update the LTC6954_GUI with the correct output frequencies.
8. Refer to the Typical DC1954A Requirements and Characteristics table for desired OUTxSEL level. Set JP1, JP2 and JP3 accordingly.
9. Connect desired output (OUT0, OUT1, OUT2) to a test instrument or other demo board to evaluate performance. *[The LVDS/CMOS outputs are DC-coupled, please make sure the levels do not exceed the test equipment input levels].*
10. To synchronize outputs provide a 1ms or greater high pulse to the SYNC SMA to take advantage of the EZSync function.

Be sure to power down or terminate any unused RF output with 50Ω, or poor spurious performance may result.

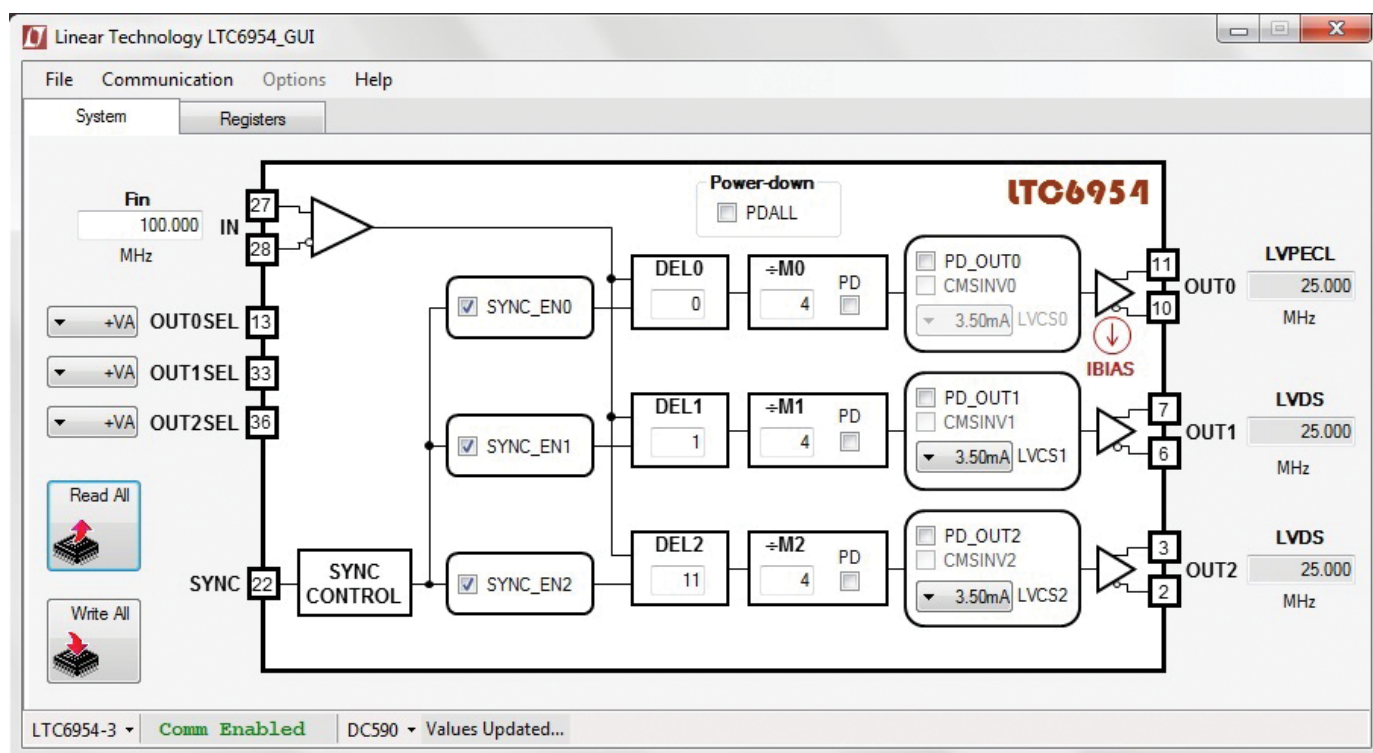


Figure 3. LTC6954_GUI Screenshot

QUICK START PROCEDURE

Troubleshooting

If the board is not functioning as expected, follow the instructions below:

1. Verify that you are able to communicate with the DC1954A. The bottom status line in LTC6954_GUI should read LTC6954 and Comm Enabled.
2. Verify that V+ 3.15V-3.45V turret has the correct voltage. (see the Typical DC1954A Requirements and Characteristics table).
3. Ensure JP1, JP2, and JP3 are set to desired position.
4. If the output type is LVPECL and the output is AC-coupled, OUTxSEL must be high for proper signal swing.
5. If the output type is LVDS, the outputs must be AC-coupled into single-ended, 50Ω input test equipment. Additionally, the unconnected output must be AC-coupled into a 50Ω load to ground to provide a balanced output load. If the LVCSx bit is low, the signal amplitude at the instrument will be approximately half of the data sheet value due to the existing 100Ω termination on the demo board.
6. If the output is CMOS, a 200Ω series resistor must be included to limit the output current when connecting to the 50Ω input on test equipment. The signal swing at the instrument is then approximately 20 percent of the data sheet value.

Contact the factory for further troubleshooting.

DC1954A RECONFIGURATION

The DC1954A allows for a variety of input and output configurations. The following covers the hardware reconfiguration of the DC1954A.

LVPECL Output Options

The DC1954A LVPECL outputs are AC-coupled and require internal biasing (OUTxSEL=H) with the default termination network. The DC1954A provides pull-down, series and a differential termination resistor options to accommodate the other LVPECL termination networks described in the data sheet.

LVDS/CMOS Output Options

The LVDS/CMOS outputs are DC-coupled and have an on board differential 100Ω resistor termination by default. The DC1954A provides pull-down, series and a differential termination resistor options to accommodate the other LVDS/CMOS termination networks described in the data sheet.

Input Options

The inputs have a 50Ω termination resistor to GND and are AC-coupled by default. The DC1954A provides pull-down, pull-up and a differential termination resistor options to accommodate the other input termination networks described in the data sheet.

Clock Follower Input Network

When using the DC1954A as a clock follower, EZSync requires the LTC6954 inputs to be taken to a low state while the SYNC pin is high. To meet this requirement, the DC1954A must be modified to support DC-coupling. Refer to the EZSync Function section and to the data sheet for more details on using the LTC6954 as a clock follower.

EZSync Function

Apply a 1ms or greater high pulse to the SYNC SMA connector to take advantage of the EZSync function. Refer to the LTC6954 data sheet for SYNC timing and level requirements.

ASSEMBLY OPTIONS

Table 1. DC1954A Assembly Options

| ASSEMBLY VERSION | U1 PART NUMBER | OUT0+/- | OUT1+/- | OUT2+/- |
|------------------|----------------|-----------|-----------|-----------|
| DC1954A-A | LTC6954IUFF-1 | LVPECL | LVPECL | LVPECL |
| DC1954A-B | LTC6954IUFF-2 | LVPECL | LVPECL | LVDS/CMOS |
| DC1954A-C | LTC6954IUFF-3 | LVPECL | LVDS/CMOS | LVDS/CMOS |
| DC1954A-D | LTC6954IUFF-4 | LVDS/CMOS | LVDS/CMOS | LVDS/CMOS |

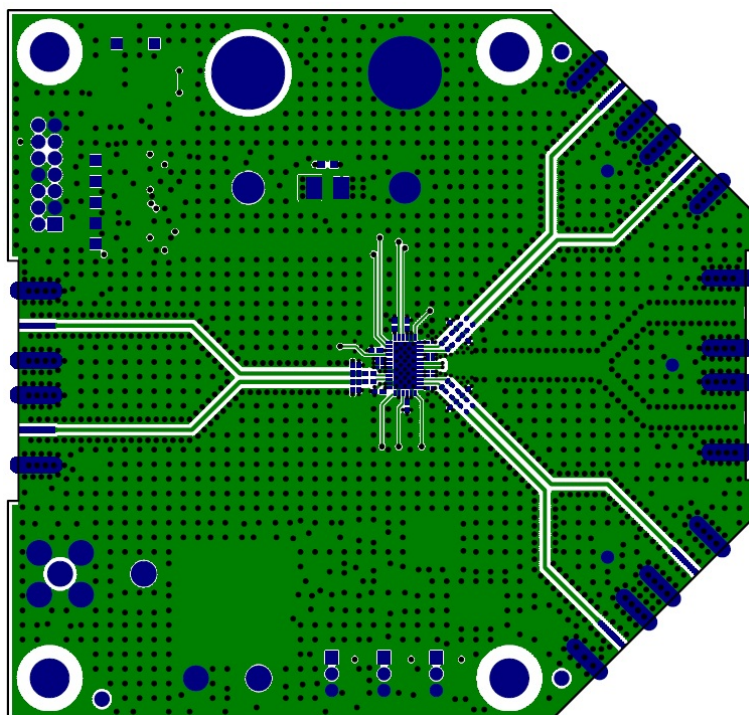
dc1954af

TYPICAL DC1954A REQUIREMENTS AND CHARACTERISTICS

| PARAMETER | INPUT OR OUTPUT | PHYSICAL LOCATION | DETAILS |
|-------------------|-----------------|--|--|
| 3.3V Power Supply | Input | J11 and J10 Banana Jacks, or 3.15V-3.45V and GND Turrets | Low-Noise and Spur-Free 3.3V, $\geq 400\text{mA}$ Capable Power Supply; Typically DC1954 Consumes $\sim 300\text{mA}$; Powers LTC6954, U2, U3, and U4 |
| OUT0+, OUT0- | Two Outputs | J1 and J2 SMA Connectors* | Refer to Figure 1 or Table 1 for Output Type If LVPECL: AC-Coupled If LVDS/CMOS: DC-Coupled Refer to LTC6954 Data Sheet for Output Levels for LVPECL, or LVDS/CMOS Option |
| OUT1+, OUT1- | Two Outputs | J3 and J4 SMA Connectors* | |
| OUT2+, OUT2- | Two Outputs | J5 and J6 SMA Connectors* | |
| OUT0SEL | Input | JP1 3-Pin Headers | If LVPECL: OUTxSEL=H: IBIAS=ON, for Default LVPECL BOM OUTxSEL=L: IBIAS=OFF, Must Install External Pull-Down Resistor, Refer to schematic If LVDS/CMOS: OUTxSEL=H: LVDS, Default LVDS/CMOS BOM OUTxSEL=L: CMOS, Remove 100Ω Differential Termination, Refer to Schematic |
| OUT1SEL | Input | JP2 3-Pin Headers | |
| OUT2SEL | Input | JP3 3-Pin Headers | |
| TEMP | Input/Output | Turret | Temperature Monitoring Diode; Force Current Measure Voltage, Refer to Data Sheet |
| TEMP GND | Input | Turret | |
| SYNC | Input | J7 SMA Connector and Turret | EZSync, 0V to 3.3V Control Signal, Refer to the Data Sheet |
| IN+, IN- | Input | J8 and J9 SMA Connectors | Input Signal Pins |

*Any unused RF output *must* be powered down or terminated with 50Ω , or poor spurious performance may result.

PCB LAYOUT



Top Layer

DEMO MANUAL DC1954A

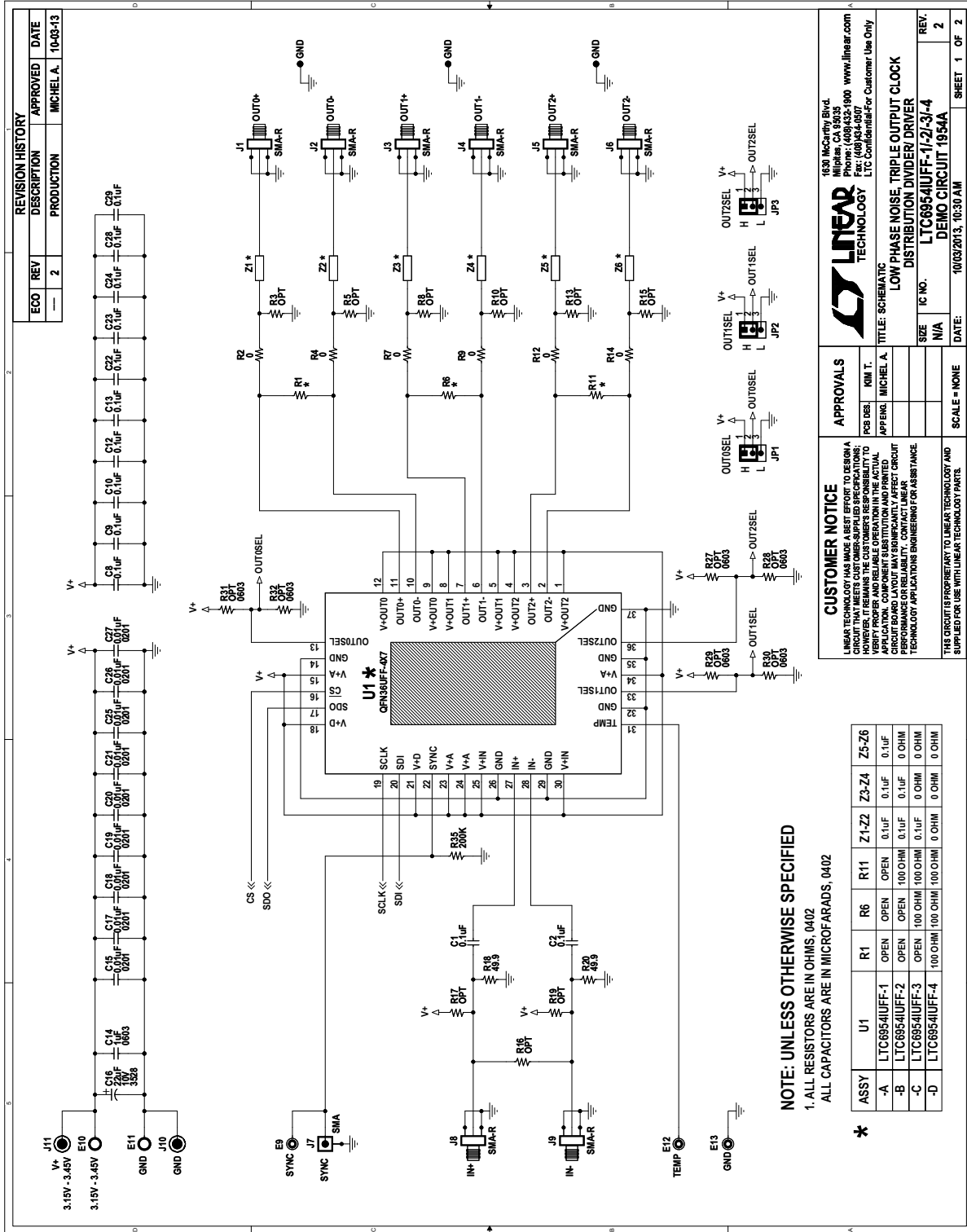
PARTS LIST

| ITEM | QTY | REFERENCE | PART DESCRIPTION | MANUFACTURER/PART NUMBER |
|--|-----|-------------------------------------|------------------------------------|-----------------------------------|
| Required Circuit Components | | | | |
| 2 | 17 | C1-C10, C12, C13, C22-C24, C28, C29 | CAP., X7R, 0.1µF, 10V, 10%, 0402 | AVX, 0402ZC104KAT2A |
| 3 | 1 | C14 | CAP., X7R, 1.0µF, 16V, 10%, 0603 | AVX, 0603YC105KAT2A |
| 4 | 9 | C15, C17-C21, C25-C27 | CAP., X7R, 0.01µF, 6.3V, 10%, 0201 | MURATA, GRM033R70J103KA01D |
| 5 | 1 | C16 | CAP., TANT, 22µF 10V, 3528 | AVX, TPSB226K010R0400 |
| 6 | 3 | E9, E12, E13 | TURRET, 0.064" | MILL-MAX, 2308-2-00-80-00-00-07-0 |
| 7 | 2 | E10, E11 | TURRET, 0.094" | MILL-MAX, 2501-2-00-80-00-00-07-0 |
| 8 | 3 | JP1, JP2, JP3 | JMP, 3 PINS 2mm CTRS. | SAMTEC, TMM-103-02-L-S |
| 9 | 8 | J1-J6, J8, J9 | CONN., SMA 50Ω EDGE-LAUNCH | EMERSON, 142-0701-851 |
| 10 | 1 | J7 | CONN, SMA STRAIGHT | CONNEX, 132134 |
| 11 | 2 | J10, J11 | JACK, BANANA | KEYSTONE, 575-4 |
| 12 | 1 | J12 | CONN., HEADER 14POS 2mm VERT GOLD | MOLEX, 87831-1420 |
| 13 | 6 | R2, R4, R7, R9, R12, R14 | RES., CHIP, 0Ω, 5% 0402 | NIC, NRC04Z0TRF |
| 14 | 0 | R3, R5, R8, R10, R13, R15-R17, R19 | RES., CHIP, 0402 | OPT |
| 15 | 2 | R18, R20 | RES., CHIP, 49.9Ω, 1/16W, 1%, 0402 | NIC, NRC04F49R9TRF |
| 16 | 5 | R22, R35, R37-R39 | RES., CHIP, 200k, 1/16W, 1%, 0402 | NIC, NRC04F2003TRF |
| 17 | 3 | R23, R24, R25 | RES., CHIP, 4.99k, 1/16W, 1%, 0402 | NIC, NRC04F4991TRF |
| 18 | 1 | R26 | RES., CHIP, 0Ω, 0603 | NIC, NRC06Z0TRF |
| 19 | 0 | R27-R29, R30-R32 | RES., CHIP, 0603 | OPT |
| 20 | 4 | R33, R34, R36, R40 | RES., CHIP, 100Ω, 1/16W, 5%, 0402 | NIC, NRC04J101TRF |
| 21 | 2 | U2, U3 | I.C., DUAL BUFFER, SC70-6 | FAIRCHILD SEMI., NC7WZ17P6X |
| 22 | 1 | U4 | I.C., DUAL TRANSCEIVER, SOT363 | NXP, 74LVC1T45GW |
| 23 | 1 | U5 | I.C., EEPROM 2KBIT 400KHZ 8TSSOP | MICROCHIP, 24LC025-I /ST |
| 24 | 3 | SHUNTS SHOWN ON ASSY DWG | SHUNT, 2mm CTRS. | SAMTEC, 2SN-BK-G |
| DC1954A-A Required Circuit Components | | | | |
| 1 | 1 | | GENERAL BOM | |
| 2 | 0 | R1, R6, R11 | RES., CHIP, 0402 | OPT |
| 3 | 6 | Z1, Z2, Z3, Z4, Z5, Z6 | CAP., X7R, 0.1µF 16V, 10%, 0402 | AVX, 0402YC104KAT2A |
| 4 | 1 | U1 | I.C., QFN36UFF-4X7 | LINEAR TECH., LTC6954IUFF-1#PBF |

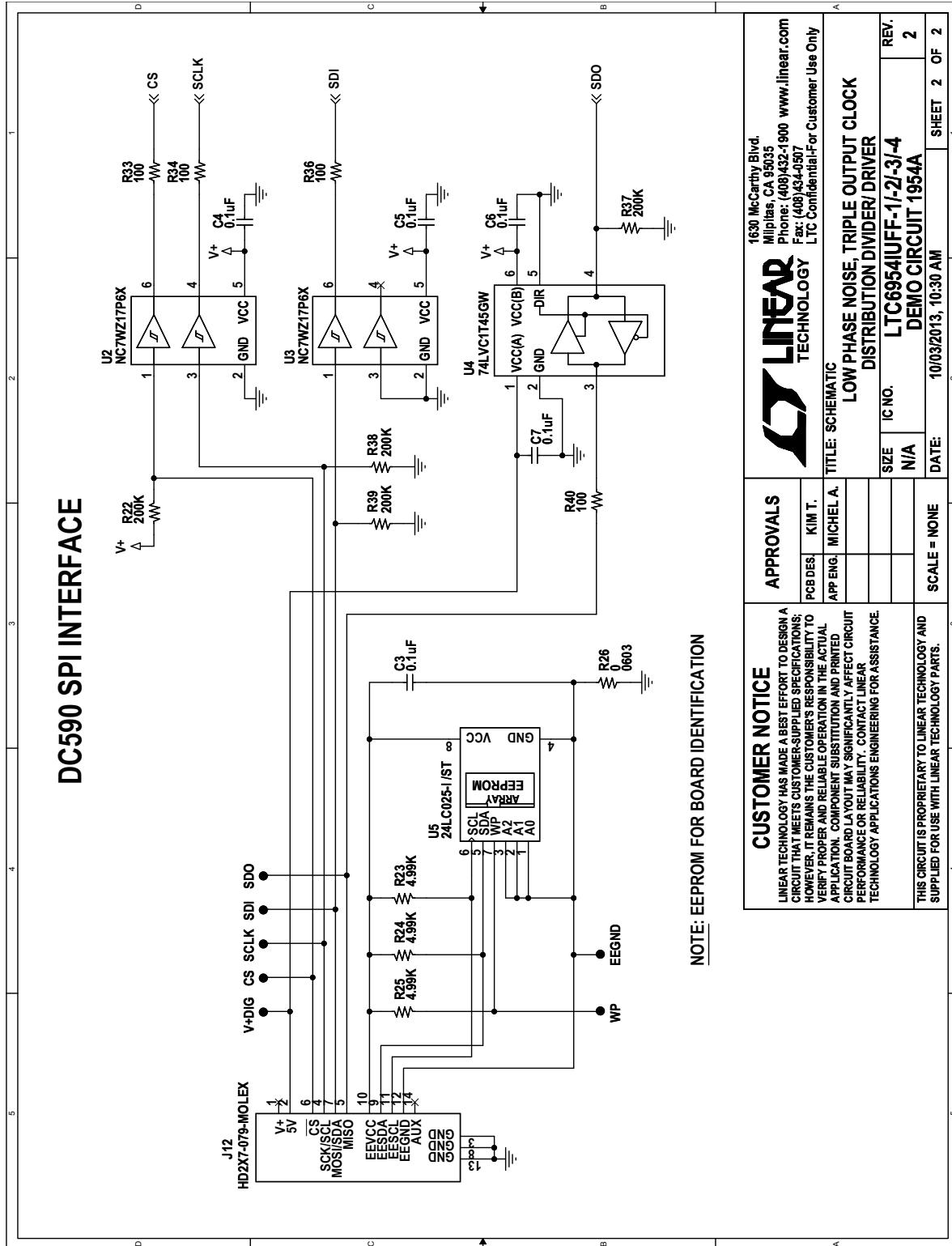
PARTS LIST

| ITEM | QTY | REFERENCE | PART DESCRIPTION | MANUFACTURER/PART NUMBER |
|--|-----|------------------------|----------------------------------|---------------------------------|
| DC1954A-B Required Circuit Components | | | | |
| 1 | 1 | | GENERAL BOM | |
| 2 | 0 | R1, R6 | RES., CHIP, 0402 | OPT |
| 3 | 1 | R11 | RES., CHIP, 100Ω 1/16W, 5%, 0402 | NIC, NRC04J101TRF |
| 4 | 4 | Z1-Z4 | CAP., X7R, 0.1μF 16V, 10%, 0402 | AVX, 0402YC104KAT2A |
| 5 | 2 | Z5, Z6 | RES., CHIP, 0Ω, 0402 | NIC, NRC04Z0TRF |
| 6 | 1 | U1 | I.C., QFN36UFF-4X7 | LINEAR TECH., LTC6954IUFF-2#PBF |
| DC1954A-C Required Circuit Components | | | | |
| 1 | 1 | | GENERAL BOM | |
| 2 | 0 | R1 | RES., CHIP, 0402 | OPT |
| 3 | 2 | R6, R11 | RES., CHIP, 100Ω 1/16W, 5%, 0402 | NIC, NRC04J101TRF |
| 4 | 2 | Z1-Z2 | CAP., X7R, 0.1μF 16V, 10%, 0402 | AVX, 0402YC104KAT2A |
| 5 | 4 | Z3, Z4, Z5, Z6 | RES., CHIP, 0Ω, 0402 | NIC, NRC04Z0TRF |
| 6 | 1 | U1 | I.C., QFN36UFF-4X7 | LINEAR TECH., LTC6954IUFF-3#PBF |
| DC1954A-D Required Circuit Components | | | | |
| 1 | 1 | | GENERAL BOM | |
| 2 | 3 | R1, R6, R11 | RES., CHIP, 100Ω 1/16W, 5%, 0402 | NIC, NRC04J101TRF |
| 3 | 6 | Z1, Z2, Z3, Z4, Z5, Z6 | RES., CHIP, 0Ω, 0402 | NIC, NRC04Z0TRF |
| 4 | 1 | U1 | I.C., QFN36UFF-4X7 | LINEAR TECH., LTC6954IUFF-4#PBF |

SCHEMATIC DIAGRAM



SCHEMATIC DIAGRAM



Note: The buffers shown on sheet 2 of 2 of the schematic are used to protect the LTC6954 when connected to the DC590 before the LTC6954 is powered up. There is no need for such circuitry if the SPI bus is not active before powering up the LTC6954. The EEPROM is for identification and is not needed to program the LTC6954.

| | | | |
|--|-----------|--|------------------------|
| | | 1630 McCarthy Blvd. Milpitas, CA 95035 Phone: (408)432-1900 www.linear.com Fax: (408)434-0507 LTC Confidential-For Customer-Use Only | |
| APPROVALS | | TITLE: SCHEMATIC | |
| PCB DES. | KIM T. | LOW PHASE NOISE, TRIPLE OUTPUT CLOCK DISTRIBUTION DIVIDER/ DRIVER | |
| APP ENG. | MICHEL A. | SIZE | IC NO. |
| | | N/A | LTC6954UIFF-1/-2/-3/-4 |
| | | DATE: | REV. |
| | | 10/03/2013, 10:30 AM | 2 |
| SCALE = NONE | | SHEET 2 OF 2 | |
| CUSTOMER NOTICE LINEAR TECHNOLOGY HAS MADE A BEST EFFORT TO DESIGN A CIRCUIT THAT MEETS CUSTOMER-SUPPLIED SPECIFICATIONS; HOWEVER, IT REMAINS THE CUSTOMER'S RESPONSIBILITY TO VERIFY PROPER AND RELIABLE OPERATION IN THE ACTUAL APPLICATION. COMPONENT SUBSTITUTION AND PRINTED CIRCUIT BOARD LAYOUT MAY SIGNIFICANTLY AFFECT CIRCUIT PERFORMANCE OR RELIABILITY. CONTACT LINEAR TECHNOLOGY APPLICATIONS ENGINEERING FOR ASSISTANCE. | | | |
| THIS CIRCUIT IS PROPRIETARY TO LINEAR TECHNOLOGY AND SUPPLIED FOR USE WITH LINEAR TECHNOLOGY PARTS. | | | |

DEMO MANUAL DC1954A

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