

# NUS3116MT

## Main Switch Power MOSFET and Dual Charging BJT

-12 V, -6.2 A, Single P-Channel with Dual PNP low  $V_{ce(sat)}$  Transistors, 3x3 mm WDFN Package

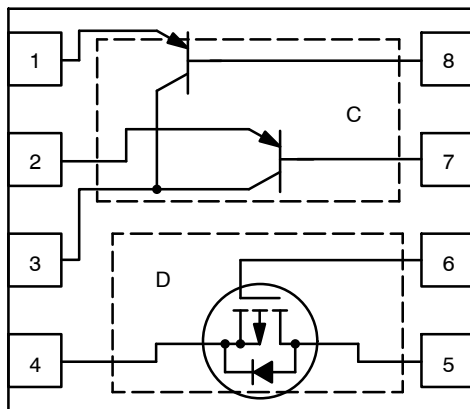
This device integrates one high performance power MOSFET and two low  $V_{ce(sat)}$  transistors, greatly reducing the layout space and optimizing charging performance in the battery-powered portable electronics.

### Features

- High Performance Power MOSFET
- Dual-Low  $V_{ce(sat)}$  Transistors as Charging Power Mux
- 3.0x3.0x0.8 mm WDFN Package
- Independent Pin-out Provides Circuit Flexibility
- Low Profile (<0.8 mm) for Easy Fit in Thin Environments
- This is a Pb-Free Device

### Applications

- Main Switch and Battery Charging Mux for Portable Electronics
- Optimized for Commercial PMUs from Top Suppliers (See Figure 2)



DFN8 3x3 Pin Connections  
(Top View)

Figure 1. Simple Schematic



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### MOSFET

$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	$I_D$ MAX
-12 V	32 mΩ @ -4.5 V	-6.2 A
	44 mΩ @ -2.5 V	

### Low $V_{ce(sat)}$ PNP (Wall)

$V_{CE0}$ MAX	$V_{EBO}$ MAX	$I_C$ MAX
-30 V	-8.0 V	-2.0 A

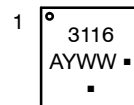
### Low $V_{ce(sat)}$ PNP (USB)

$V_{CE0}$ MAX	$V_{EBO}$ MAX	$I_C$ MAX
-30 V	-8.0 V	-2.0 A



DFN8  
CASE 506BC

### MARKING DIAGRAM



3116 = Device Code  
 A = Assembly Location  
 Y = Year  
 WW = Work Week  
 ■ = Pb-Free Package  
 (Note: Microdot may be in either location)

### ORDERING INFORMATION

Device	Package	Shipping†
NUS3116MTR2G	WDFN8 (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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## P-Channel Power MOSFET Maximum Ratings ( $T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter		Symbol	Value	Units	
Drain-to-Source Voltage		$V_{DSS}$	-12	V	
Gate-to-Source Voltage		$V_{GS}$	$\pm 8.0$	V	
Continuous Drain Current (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	-5.47	A	
		$T_A = 85^\circ\text{C}$	-4.0		
	$t \leq 5\text{ s}$	$T_A = 25^\circ\text{C}$	-6.2		
Power Dissipation (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	1.7	W	
	$t \leq 5\text{ s}$		2.2		
Continuous Drain Current (Note 2, Minimum Pad)	Steady State	$T_A = 25^\circ\text{C}$	-4.4	A	
		$T_A = 85^\circ\text{C}$	-3.2		
Power Dissipation (Note 2)		$T_A = 25^\circ\text{C}$	1.14	W	
Pulsed Drain Current	$t_p = 10\ \mu\text{s}$		$I_{DM}$	-25	A
Operating Junction and Storage Temperature		$T_J, T_{STG}$	-55 to 150	$^\circ\text{C}$	
Source Current (Body Diode) <sup>2</sup>		$I_S$	-2.8	A	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		$T_L$	260	$^\circ\text{C}$	

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Units
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	110	$^\circ\text{C}/\text{W}$
Junction-to-Ambient – $t < 10\text{ s}$ (Note 2)	$R_{\theta JA}$	56	$^\circ\text{C}/\text{W}$
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	72	$^\circ\text{C}/\text{W}$
Junction-to-Ambient – $t < 10\text{ s}$ (Note 1)	$R_{\theta JA}$	40	$^\circ\text{C}/\text{W}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces)
- Surface-mounted on FR4 board using the minimum recommended pad size of 0.5 in sq, 1 oz. Cu.

## P-Channel MOSFET Electrical Characteristics ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
<b>OFF CHARACTERISTICS</b>						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-12.0			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = -250\ \mu\text{A}, \text{ref to } 25^\circ\text{C}$		-10.1		$\text{mV}/^\circ\text{C}$
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = -12\text{ V}$	$T_J = 25^\circ\text{C}$		-1.0	$\mu\text{A}$
			$T_J = 125^\circ\text{C}$		-10	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 8\text{ V}$			$\pm 200$	nA

### ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = -250\ \mu\text{A}$	-0.45	-0.67	-1.1	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			2.68		$\text{mV}/^\circ\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}, I_D = -3.0\text{ A}$		32	40	m $\Omega$
		$V_{GS} = -2.5\text{ V}, I_D = -3.0\text{ A}$		44	50	
Forward Transconductance	$g_{FS}$	$V_{DS} = -16\text{ V}, I_D = -3.0\text{ A}$		5.9		S

- Pulsed Condition: Pulse Width = 300  $\mu\text{sec}$ , Duty Cycle  $\leq 2\%$

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## P-Channel MOSFET Electrical Characteristics (T<sub>J</sub> = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
<b>CHARGES, CAPACITANCES AND GATE RESISTANCE</b>						
Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> = 0 V, f = 1.0 MHz, V <sub>DS</sub> = -12 V		1329		pF
Output Capacitance	C <sub>OSS</sub>			200		
Reverse Transfer Capacitance	C <sub>RSS</sub>			116		
Total Gate Charge	Q <sub>G(tot)</sub>	V <sub>GS</sub> = -4.5 V, V <sub>DS</sub> = -12 V, I <sub>D</sub> = -3.0 A		13		nC
Threshold Gate Charge	Q <sub>G(th)</sub>			1.5		
Gate-to-Source Charge	Q <sub>GS</sub>			2.2		
Gate-to-Drain Charge	Q <sub>GD</sub>			2.9		

## SWITCHING CHARACTERISTICS

Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>GS</sub> = -4.5 V, V <sub>DD</sub> = -12 V, I <sub>D</sub> = -3.0 A, R <sub>G</sub> = 3.0		8		ns
Rise Time	t <sub>r</sub>			17.5		
Turn-Off Delay Time	t <sub>d(off)</sub>			80		
Fall Time	t <sub>f</sub>			56.5		

## DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Recovery Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = -1.0 A	T <sub>J</sub> = 25°C		-0.66	-1.2	V
			T <sub>J</sub> = 125°C		-0.54		
Reverse Recovery Time	t <sub>rr</sub>	V <sub>GS</sub> = 0 V, dI <sub>SD</sub> /dt = 100 A/μs, I <sub>S</sub> = -1.0 A		70.8		ns	
Charge Time	t <sub>a</sub>			14.3			
Discharge Time	t <sub>b</sub>			56.4			
Reverse Recovery Charge	Q <sub>RR</sub>			44			nC

3. Pulsed Condition: Pulse Width = 300 μsec, Duty Cycle ≤ 2%

## Dual-PNP Transistors Maximum Ratings (T<sub>J</sub> = 25°C unless otherwise stated)

Parameter	Symbol	Value	Units
Collector-Emitter Voltage	V <sub>CEO</sub>	-30	V
Collector-Base Voltage	V <sub>CB0</sub>	-30	V
Emitter-Base Voltage	V <sub>EBO</sub>	-8.0	V
Collector Current, Continuous	I <sub>C</sub>	-2.0	A
Collector Current, Pulsed (Note 4)	I <sub>C</sub>	-6.0	A
Operating Junction and Storage Temperature	T <sub>J</sub> , T <sub>STG</sub>	-55 to 150	°C
Thermal Resistance Dissipation	P <sub>D</sub>	1.5	W
Thermal Resistance (Note 5)	R <sub>θJA</sub>	83	°C/W
Thermal Resistance Dissipation	P <sub>D</sub>	810	mW
Thermal Resistance (Note 6)	R <sub>θJA</sub>	155	°C/W

4. Single Pulse: Pulse Width = 1 ms

5. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces)

6. Surface-mounted on FR4 board using the minimum recommended pad size of 100 mm<sup>2</sup>, 1 oz. Cu.

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## Dual-PNP Transistors Electrical Characteristics ( $T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
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### OFF CHARACTERISTICS

Collector-Emitter Voltage	$V_{CE0}$	$I_C = -10\text{ mA}, I_B = 0$	-30			V
Collector-Base Voltage	$V_{CBO}$	$I_C = -0.1\text{ mA}, I_E = 0$	-30			V
Emitter-Base Voltage	$V_{EBO}$	$I_E = -0.1\text{ mA}, I_C = 0$	-8.0			V
Collector-Emitter Cutoff Current	$I_{CES}$	$V_{CES} = -30\text{ V}$			-0.1	$\mu\text{A}$

### ON CHARACTERISTICS

DC Current Gain (Note 7)	$h_{FE}$	$I_C = -1.0\text{ A}, V_{CE} = -2.0\text{ V}$	100	200		-
DC Current Gain (Note 7)	$h_{FE}$	$I_C = -2.0\text{ A}, V_{CE} = -2.0\text{ V}$	100	200		-
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = -1.0\text{ A}, I_B = -0.01\text{ A}$			0.22	V
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = -1.0\text{ A}, I_B = -0.1\text{ A}$			0.12	V
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = -2.0\text{ A}, I_B = -0.2\text{ A}$			0.24	V
Input Capacitance	$C_{ibo}$	$V_{EB} = -0.5\text{ V}, f = 1.0\text{ MHz}$		240	400	pF
Output Capacitance	$C_{obo}$	$V_{CB} = -3.0\text{ V}, f = 1.0\text{ MHz}$		50	100	pF

7. Pulsed Condition: Pulse Width = 300  $\mu\text{sec}$ , Duty Cycle  $\leq 2\%$

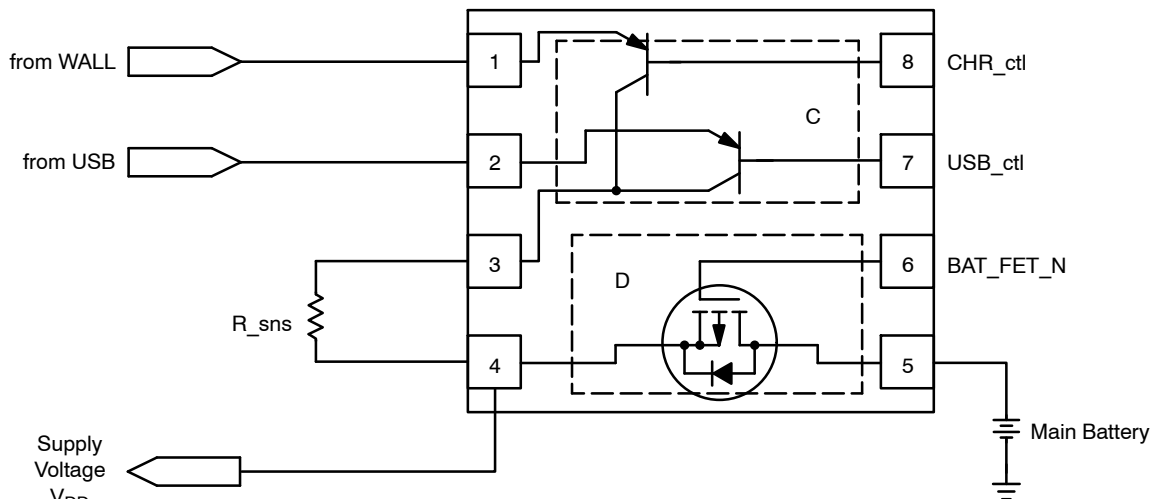


Figure 2. Typical Application Circuit

TYPICAL CHARACTERISTICS - MOSFET

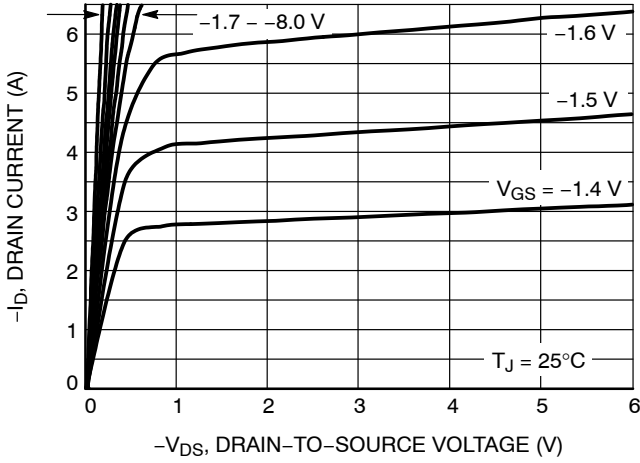


Figure 3. On-Region Characteristics

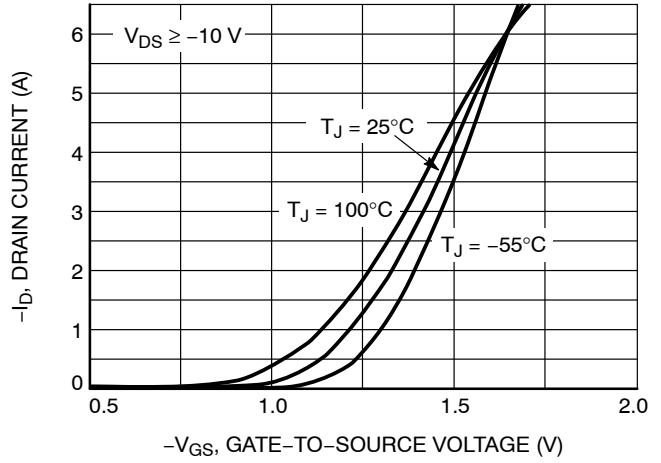


Figure 4. Transfer Characteristics

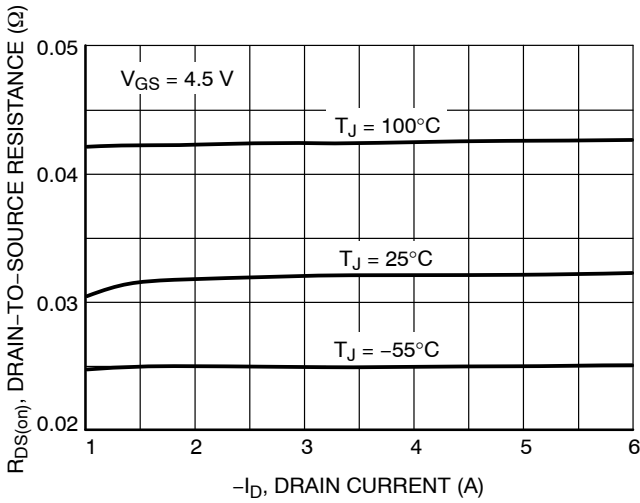


Figure 5. On-Resistance vs. Drain Current

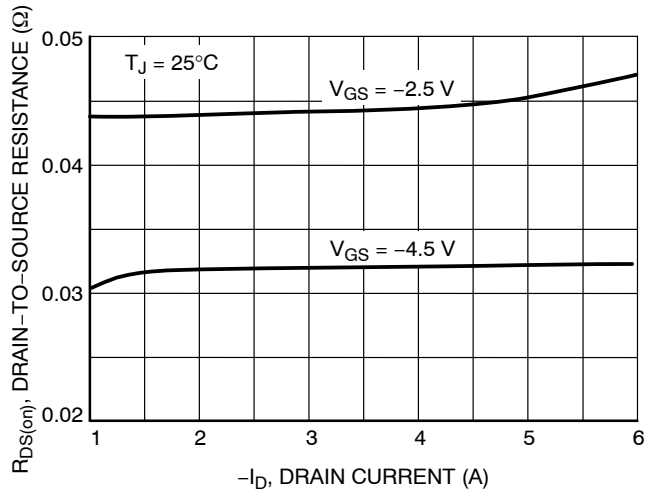


Figure 6. On-Resistance vs. Drain Current and Gate Voltage

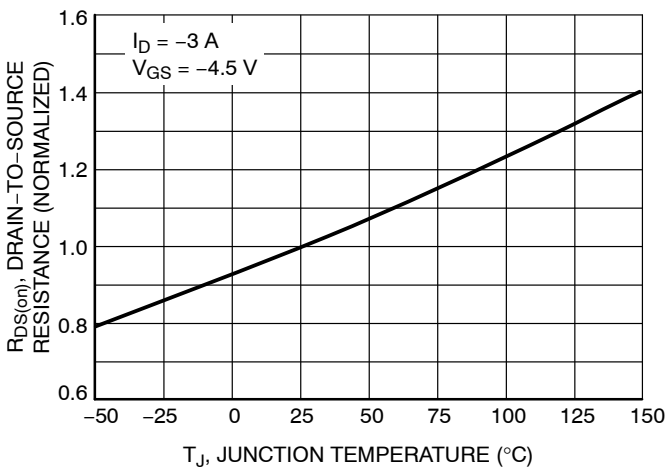


Figure 7. On-Resistance Variation with Temperature

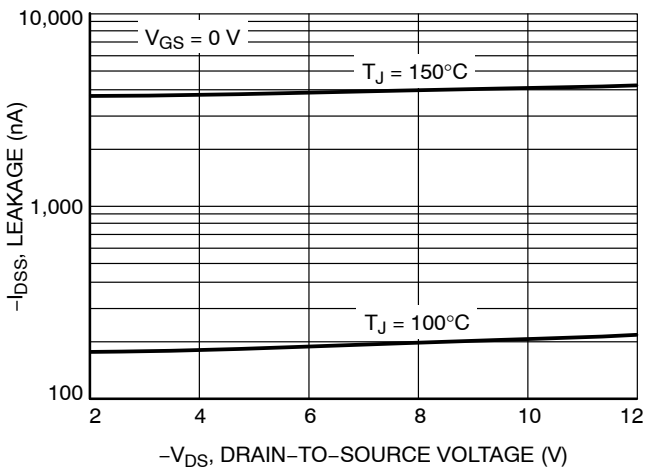


Figure 8. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS - MOSFET

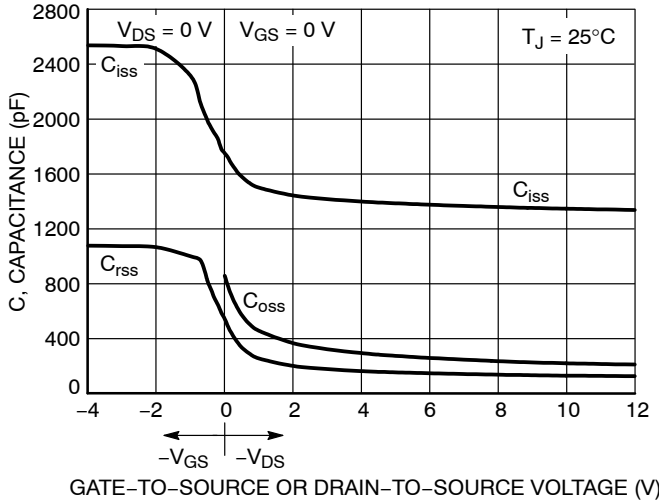


Figure 9. Capacitance Variation

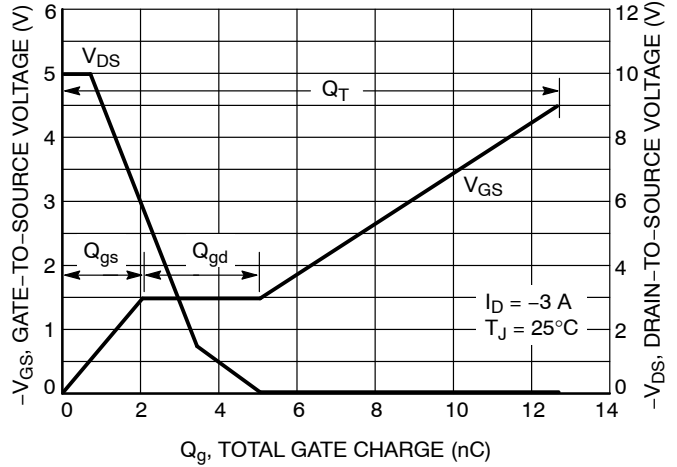


Figure 10. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

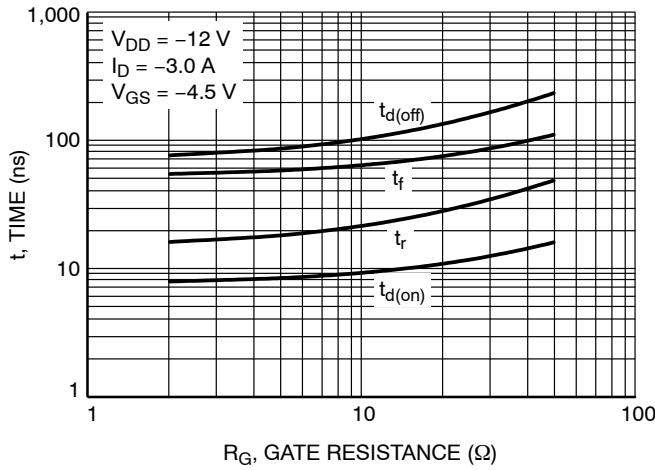


Figure 11. Resistive Switching Time Variation vs. Gate Resistance

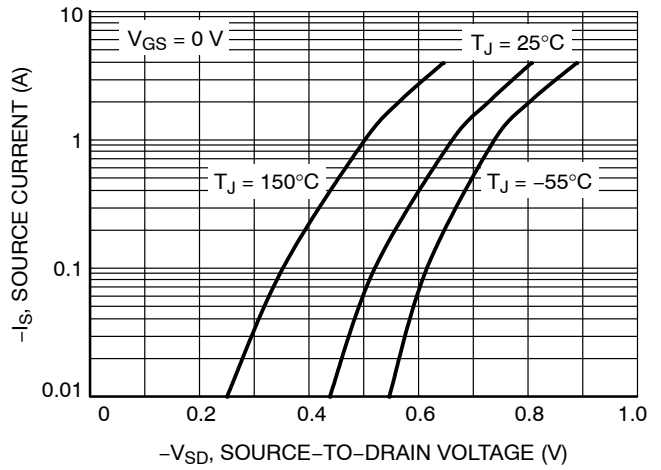
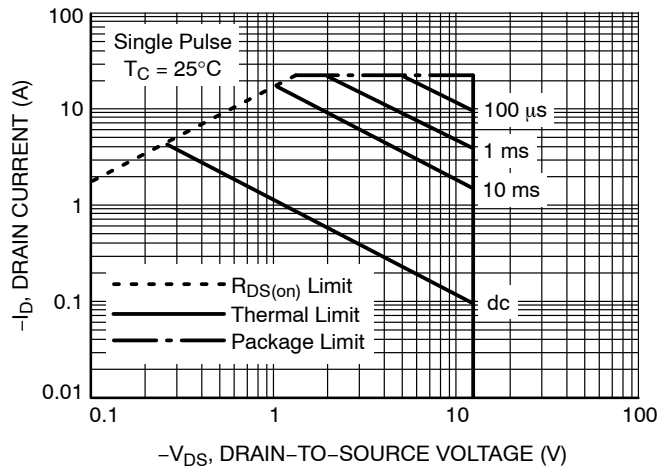


Figure 12. Diode Forward Voltage vs. Current



Mounted on 2" sq. FR4 board (0.5" sq. 2 oz. Cu single sided) with MOSFET die operating.

Figure 13. Maximum Rated Forward Biased Safe Operating Area

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## TYPICAL CHARACTERISTICS - MOSFET

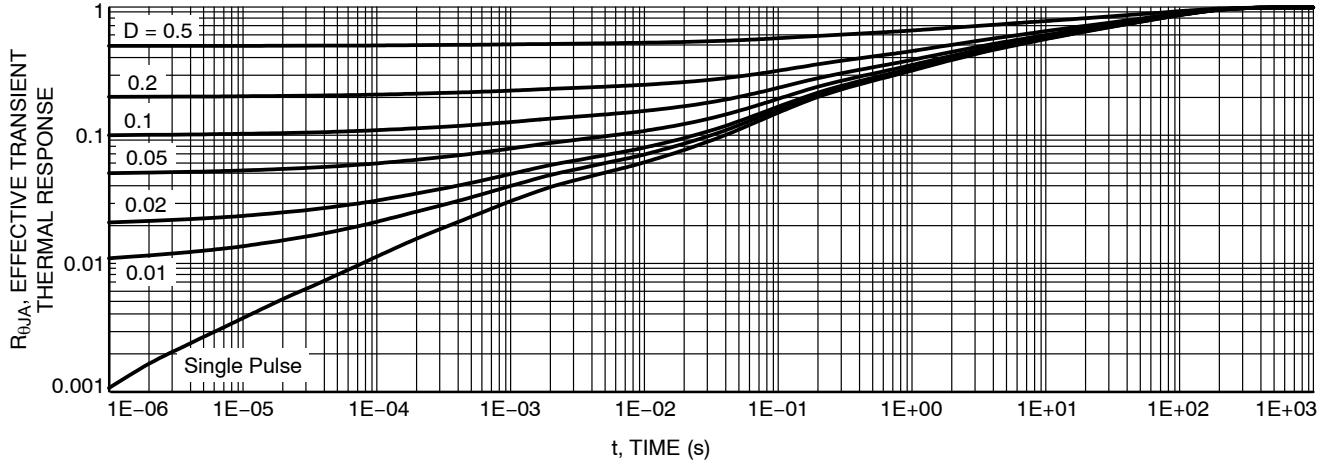


Figure 14. FET Thermal Response

TYPICAL CHARACTERISTICS - BJT

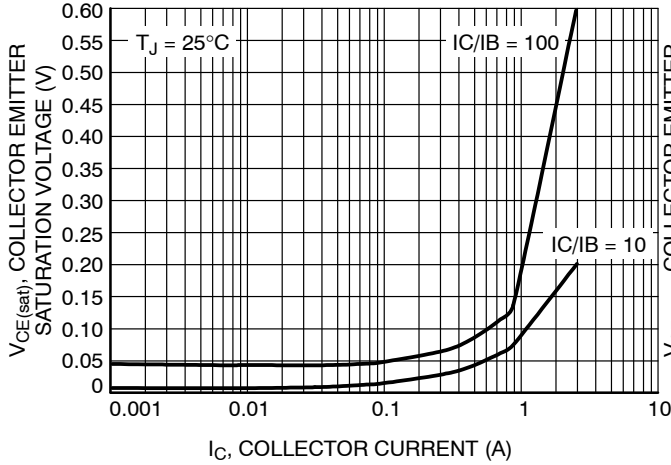


Figure 15. Collector Emitter Saturation Voltage vs. Collector Current

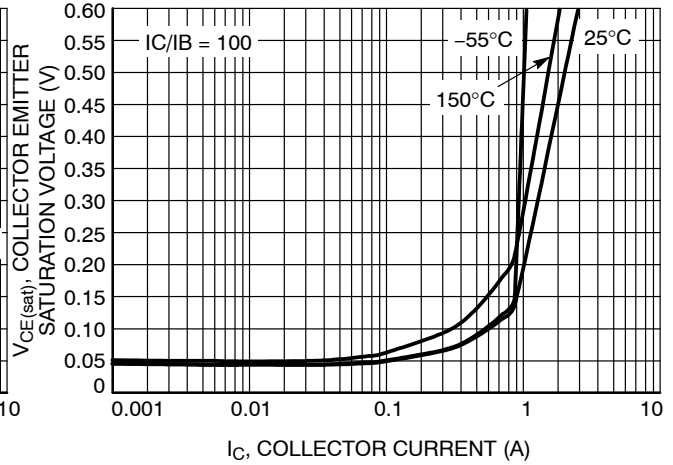


Figure 16. Collector Emitter Saturation Voltage vs. Collector Current

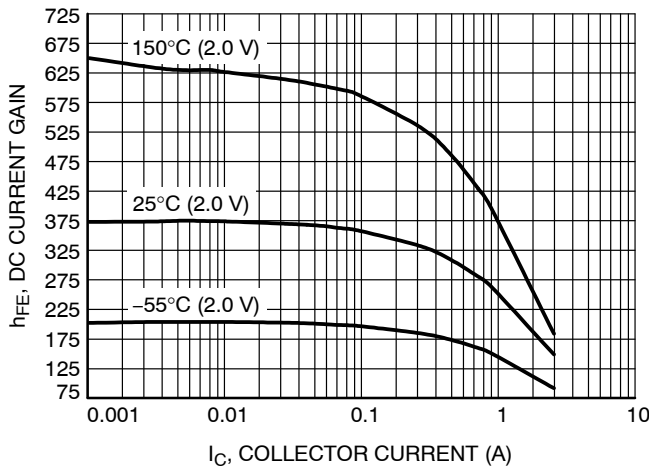


Figure 17. DC Current Gain vs. Collector Current

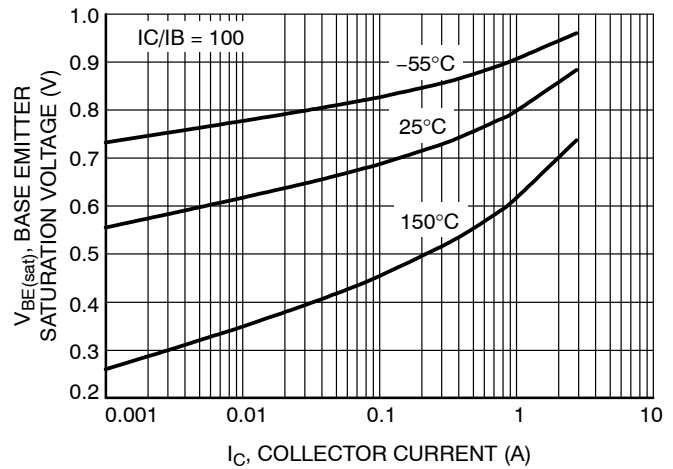


Figure 18. Base Emitter Saturation Voltage vs. Collector Current

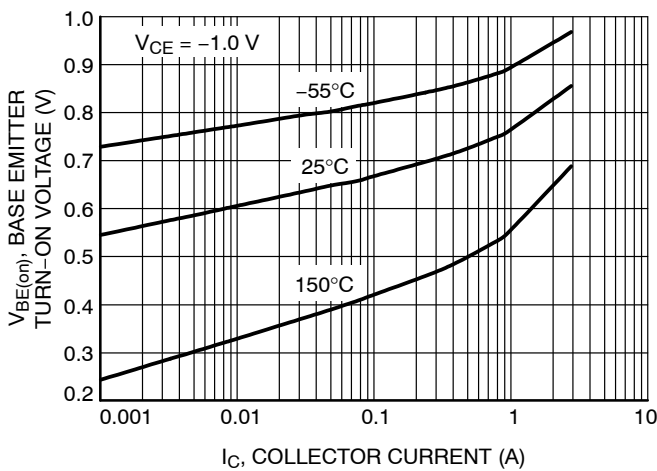


Figure 19. Base Emitter Turn-On Voltage vs. Collector Current

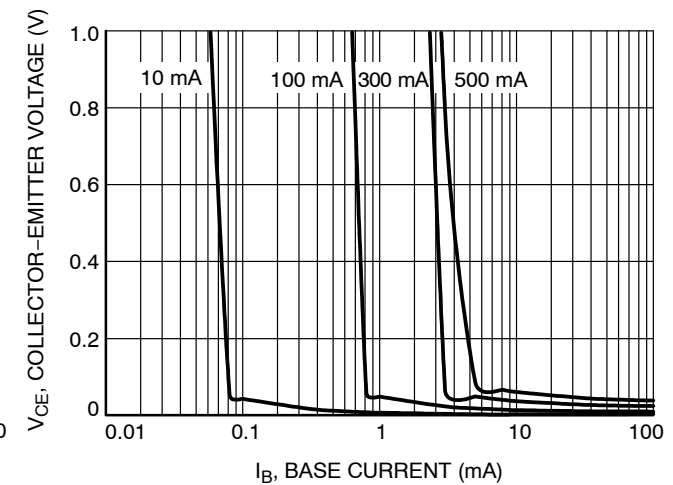


Figure 20. Saturation Region



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## TYPICAL CHARACTERISTICS - BJT

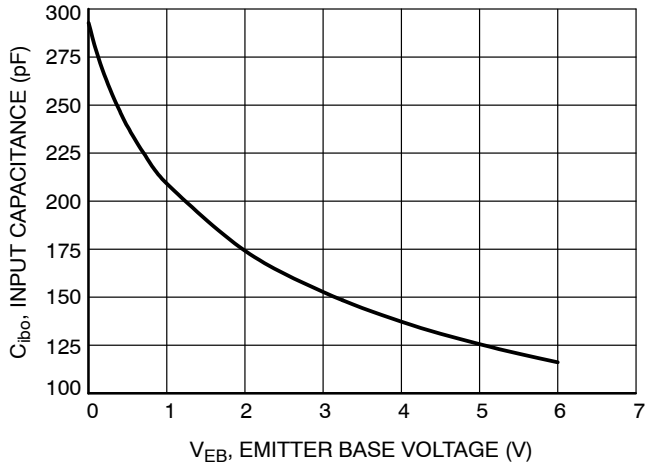


Figure 21. Input Capacitance

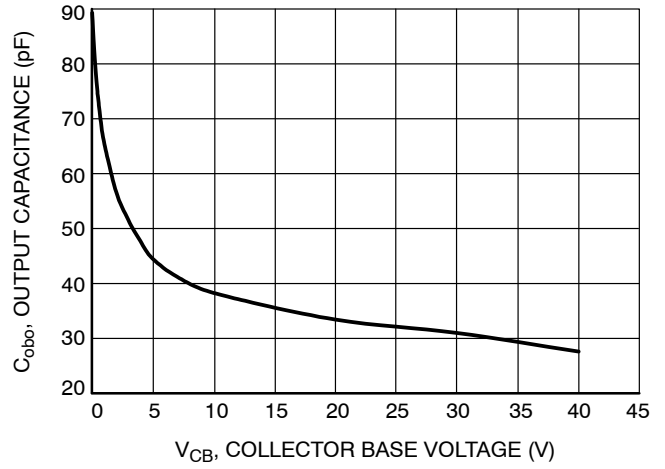
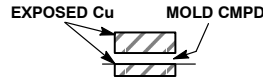
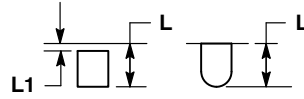
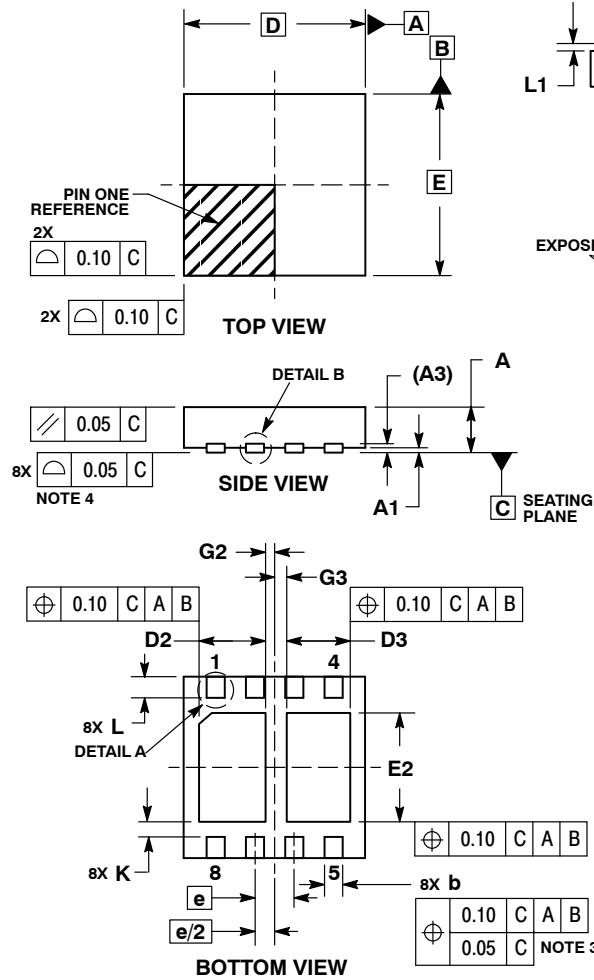


Figure 22. Output Capacitance

# NUS3116MT

## PACKAGE DIMENSIONS

WDFN8, 3x3, 0.65P  
CASE 506BC-01  
ISSUE A

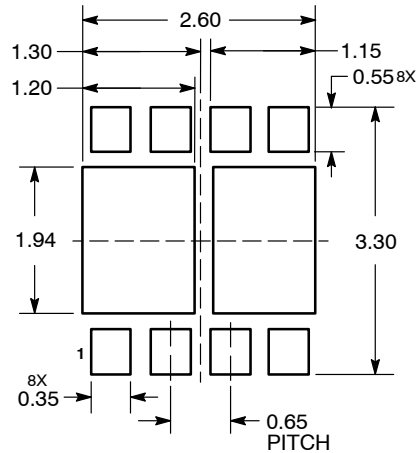


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	3.00 BSC	
D2	1.00	1.20
D3	0.95	1.15
E	3.00 BSC	
E2	1.70	1.90
e	0.65 BSC	
G2	0.15 BSC	
G3	0.20 BSC	
K	0.20	---
L	0.25	0.45
L1	---	0.15

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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