2.5/3.3V 220MHz High-Speed, Low-Jitter, Low-Skew, Zero-Delay Clock Buffer with 9 Outputs

Features

- Phase-Lock Loop Clock Distribution (Zero Input-to-Output Delay)
- Internal feedback connection
- Distributes one-to-two banks of four outputs w/ one CLKOUT (9 - outputs total)
- High-Performance
  - 30 MHz to 220 MHz operation frequency range
  - <100ps output-to-output skew
  - <100ps cycle-to-cycle jitter
  - Low Power Configuration - 26mA (outputs unloaded)
- Spread-spectrum capable
- Power supply: +2.5V ±5% ; +3.3V ±10%
- Industrial temperature range parts available
- Packaging (Pb-free & Green):
  — 16-pin TSSOP (L)
  — 16-pin SOIC (W)

Description

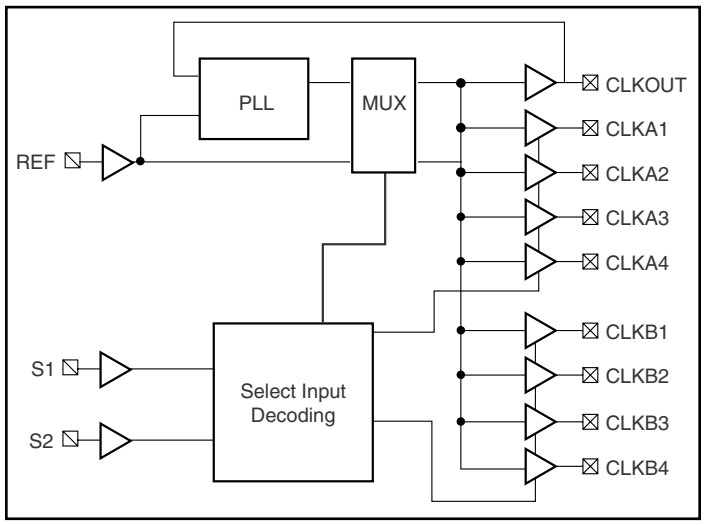
The PI6C22409-1H is a low-jitter, low-skew, high-speed Zero-Delay Buffer with 9 outputs designed to address high-speed clock distribution applications.

The PI6C22409-1H features an internal patented Phase Lock Loop (PLL) with high drive output capability and internal feedback.

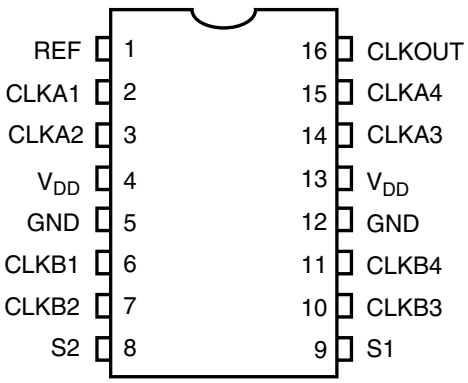
The PI6C22409-1H operates from a 2.5V ±5% or 3.3V ±10% supply. All support documentation can be found on Pericom's web site at: www.pericom.com.

Pericom can customize these devices for specific requirements.

Block Diagram



Pin Configuration



Pin Description

Pin	Signal	Description
1	REF	Reference clock input with weak pull down.
2,3,6,7, 10,11,14,15	CLKA1, CLKA2, CLKB1, CLKB2, CLKB3, CLKB4, CLKA3, CLKA4, CLKOUT	Clock output. Clock outputs with weak pull-down.
16	CLKOUT	Clock output. Internal feedback on this pin.
5,12	GND	Ground
4,13	V_{DD}	Power
8,9	S2, S1	Select input with weak pull-ups.

Select Input Decoding

S2	S1	Clock A1 - A4	Clock B1 - B4	CLKOUT	Output Source	PLL shutdown
0	0	Tri-State	Tri-State	Driven	PLL	N
0	1	Driven	Tri-State	Driven	PLL	N
1	0	Driven	Driven	Driven	Reference	Y
1	1	Driven	Driven	Driven	PLL	N

Maximum Ratings(1)

Supply Voltage
- V_{DD} .....-0.5V to +4.6V
- REF……. .....-0.5V to +4.6V

Input Current ……. .....-50mA
Output Current ..... ……..±50mA
Lead Temperature (cap soldering, 10 sec.) .....+260°C
Storage Temperature (Ts) .....-65°C to +150°C
Junction Temperature…..…….. .....+150°C
Operating Temperature (cap industrial)… ....-40°C to +85°C
Operating Temperature (cap commercial)…... .0°C to +70°C

Operation Ratings(2)

Supply voltage
- V_{DD}…….. ……..+3.0V to +3.6V
- V_{DD}……..….. ……+2.375V to +2.625V

Ambient Temperature (T_A)…....……..0°C to +70°C
Package Thermal Resistance(2)
θJA
- Still-Air (SOIC-16)….....……89°C/W
- Still-Air (SOIC-16).....90°C/W

θJB
- Junction-to-Board (SOIC-16)..... 26°C
- Junction-to-Board (TSSOP-16) ..... 24°C

Notes:

1. Stresses greater then those listed under Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. θJA and θJB values are determined for a 4-layer board in still-air, unless otherwise stated.

DC Electrical Characteristics

Parameter	Description	Test Conditions		Min.	Max.	Units
V_{IL}	Input LOW Voltage	V_{DD} = 3.3V			0.8	V
		V_{DD} = 2.5V			0.7	
V_{IH}	Input HIGH Voltage	V_{DD} = 3.3V		2.0		
		V_{DD} = 2.5V		1.7		
I_{IL}	Input LOW Current	V_{IN} = 0V			50	µA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}			125	
V_{OL}	Output LOW Voltage	I_{OL} = 12mA	V_{DD} = 3.3V		0.25	V
			V_{DD} = 2.5V		0.35	
V_{OH}	Output HIGH Voltage	V_{DD} = 2.5V, I_{OH} = –12mA		1.9		
		V_{DD} = 3.3V, I_{OH} = –12mA		2.55		
I_{DD}	Supply Current	Unloaded outputs 66 MHz			32	mA

AC Electrical Characteristics

Parameter	Description	Test Conditions		Min.	Typ.	Max.	Units
F_O	Output Frequency	V_{DD} = 2.5V		10		200	MHz
		V_{DD} = 3.3V		10		220	MHz
BW	Bandwidth for PLL	V_{DD} = 2.5V			0.8		MHz
		V_{DD} = 3.3V			1.5		
t_{DC}	Duty Cycle(4)	Measured at V_{DD}/2, 10 pF load		45	50	55	%
t_R	Rise Time(1)(4)	For 3.3V: Measured between 0.8V and 2.0V; @10pF				1	ns
		For 2.5V: Measured between 0.6V and 1.8V; @10pF				1.8	
t_F	Fall Time(1)(4)	For 3.3V: Measured between 0.8V and 2.0V; @10pF				1	
		For 2.5V: Measured between 0.6V and 1.8V; @10pF				1.8	
$t_{sk(o)}$	Output to Output skew(1)	All Outputs Equally Loaded	V_{DD} = 3.3V			100	ps
			V_{DD} = 2.5V			100	
t_0	Delay, REF Rising Edge to CLKOUT Rising Edge(1)(2)(5)	Measured at V_{DD}/2, 66MHz	V_{DD} = 3.3V	-100		100	
			V_{DD} = 2.5V	-200	0	200	
$t_{SK(D)}$	Device-to-device skew(1)(3)	Measured at V_{DD}/2 on CLKx pins of device		-300	0	+300	
t_{JIT}	Cycle-to-Cycle Jitter	15pF load, >66MHz, standard drive	V_{DD} = 3.3V		47	110	ps
			V_{DD} = 2.5V		42	90	
		15pF load, >66MHz, high drive	V_{DD} = 3.3V		45	100	
			V_{DD} = 2.5V		40	80	
		30pF load, >66MHz, standard drive	V_{DD} = 3.3V		63	120	
			V_{DD} = 2.5V		83	130	
		30pF load, >66MHz, high drive	V_{DD} = 3.3V		51	115	
			V_{DD} = 2.5V		66	115	
t_{PJ}	Period Jitter (Peak)	15pF load, >66MHz, standard drive	V_{DD} = 3.3V		39	90	ps
			V_{DD} = 2.5V		28	60	
		15pF load, >66MHz, high drive	V_{DD} = 3.3V		39	85	
			V_{DD} = 2.5V		27	55	
		30pF load, >66MHz, standard drive	V_{DD} = 3.3V		48	85	
			V_{DD} = 2.5V		75	90	
		30pF load, >66MHz, high drive	V_{DD} = 3.3V		43	75	
			V_{DD} = 2.5V		60	80	
t_{LOCK}	PLL Lock time (1)	Stable power supply, valid clocks presented on CLKOUT pin				1	ms

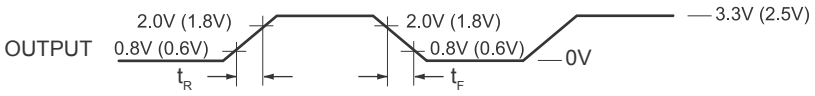
Note:

1. See Switching Waveforms
2. All clock output should have the same loading to achieve zero delay between the input and outputs and zero output-to-output skew. Since the CLKOUT pin is the internal feedback to the PLL, its relative loading can adjust to input-to-output delay. If input-to-output delay adjustments are needed, the CLKOUT load may be changed to vary the delay between the REF input to the clock outputs. Output-to-output skew includes CLKA1-4 and CLKB1-4.
3. Specifications are guaranteed by design and not production tested.
4. Measured at 100MHz.
5. Measured with 16-Pin SOIC package

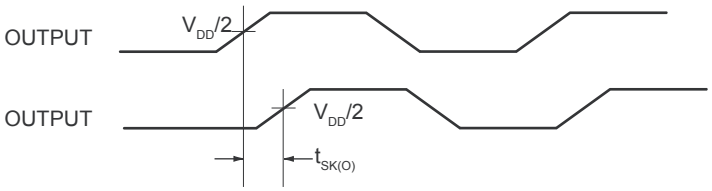
Switching Waveforms

Duty Cycle Timing

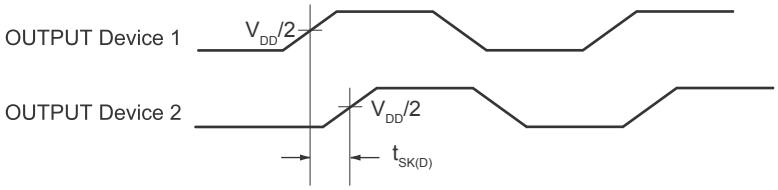
All Outputs Rise/Fall Time



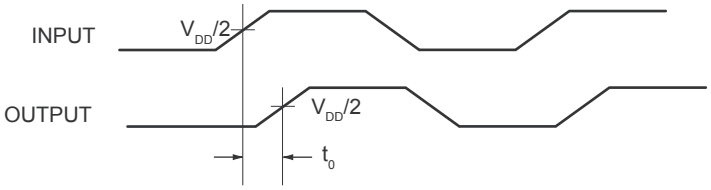
Output – Output Skew



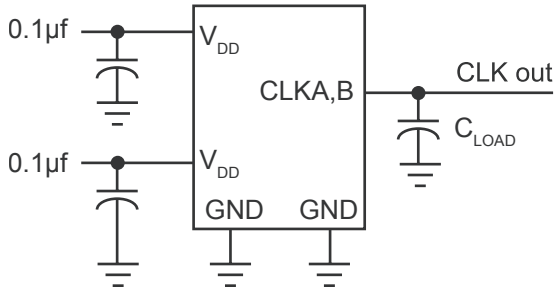
Device – Device Skew



Input-Output Propagation Delay

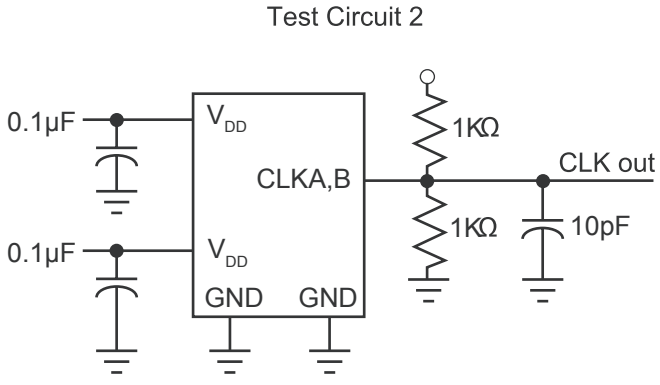


Test Circuit 1



Test Circuit for all parameters except t_{SLEW}

Test Circuit 2

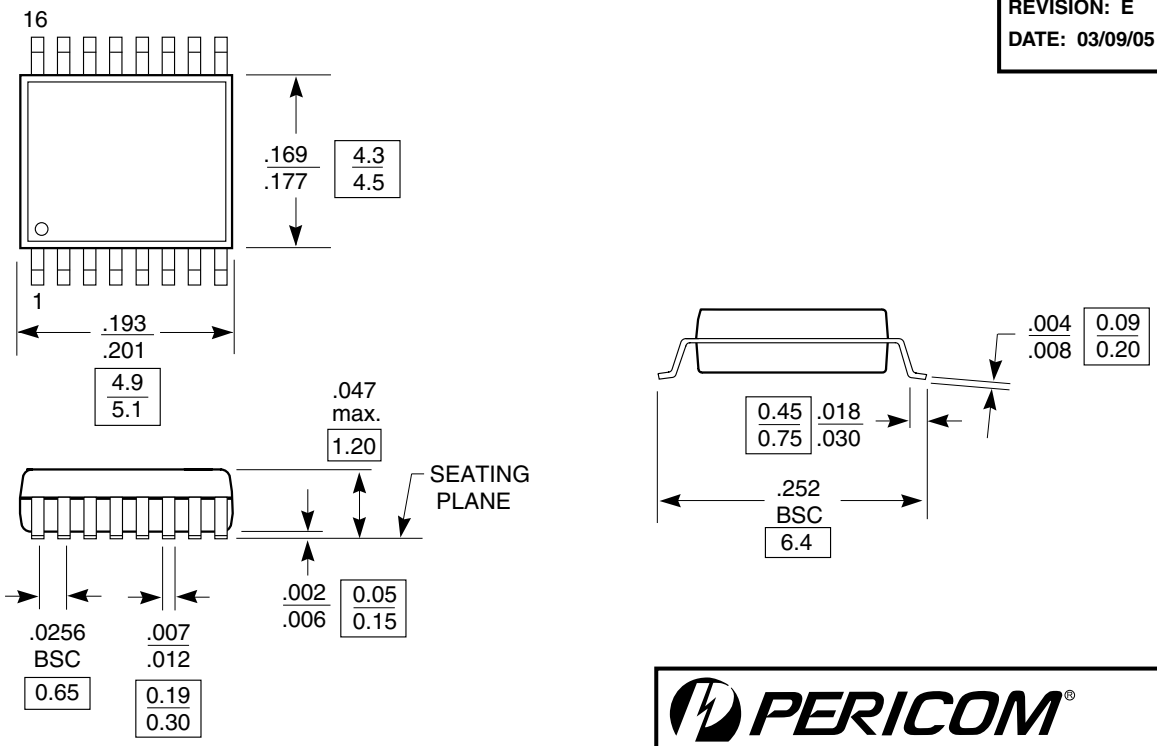


Test Circuit for t_{SLEW} Output slew

Packaging Mechanical: 16-Pin TSSOP (L)

DOCUMENT CONTROL NO.
PD - 1310

REVISION: E
DATE: 03/09/05



Note:
1. Package Outline Exclusive of Mold Flash and Metal Burr
2. Controlling dimentions in millimeters
3. Ref: JEDEC MO-153F/AB

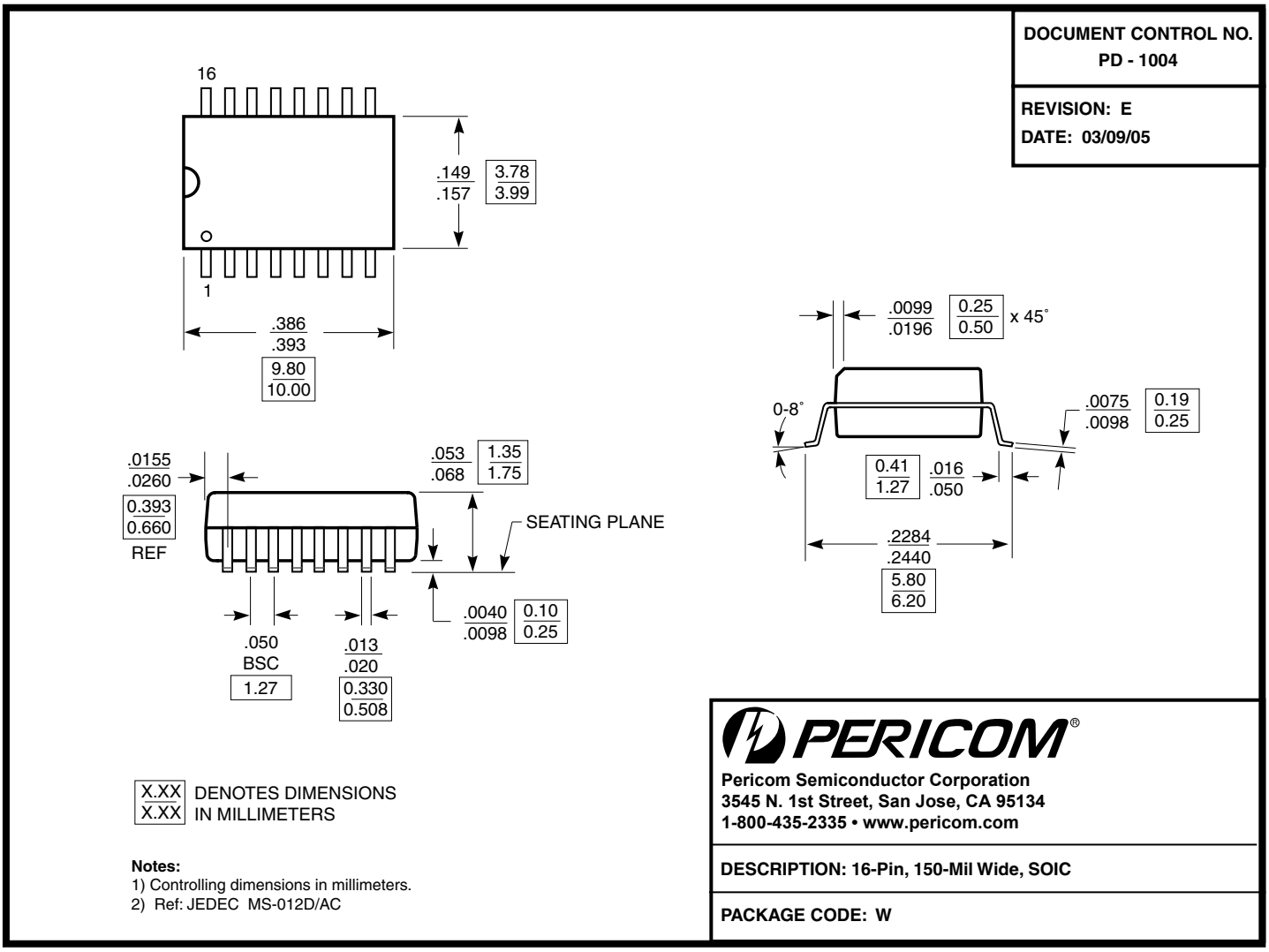
Pericom Semiconductor Corporation
3545 N. 1st Street, San Jose, CA 95134
1-800-435-2335 • www.pericom.com

DESCRIPTION: 16-Pin, 173-Mil Wide, TSSOP

PACKAGE CODE: L

Note:
• For latest package info, please check: http://www.pericom.com/products/packaging/mechanicals.php

Packaging Mechanical: 16-Pin SOIC (W)



Note:
• For latest package info, please check: http://www.pericom.com/products/packaging/mechanicals.php

Ordering Information[1,2,3]

Ordering Code	Package Code	Package Type
PI6C22409-1HLE	L	Pb-free & Green, 16-pin TSSOP
PI6C22409-1HLIE	L	Pb-free & Green, 16-pin TSSOP, Industrial temp range
PI6C22409-1HWE	W	Pb-free & Green, 16-pin SOIC
PI6C22409-1HWIE	W	Pb-free & Green, 16-pin SOIC, Industrial temp range

Notes:
1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. E = Pb-free and Green
3. Adding an X suffix = Tape/Reel