Low Voltage, 1.15 V to 5.5 V, 4-Channel, Bidirectional Logic Level Translator

ADG3304-EP

FEATURES

- Bidirectional level translation
- Operates from 1.15 V to 5.5 V
- Low quiescent current < 5 µA
- No direction pin
- Supports defense and aerospace applications (AQEC standard)
- Military temperature range: −55°C to +125°C
- Controlled manufacturing baseline
- One assembly and test site
- One fabrication site
- Enhanced product change notification
- Qualification data available on request

APPLICATIONS

- SPI®, MICROWIRE™ level translation
- Low voltage ASIC level translation
- Smart card readers
- Cell phones and cell phone cradles
- Portable communications devices
- Telecommunications equipment
- Network switches and routers
- Storage systems (SAN/NAS)

FUNCTIONAL BLOCK DIAGRAM

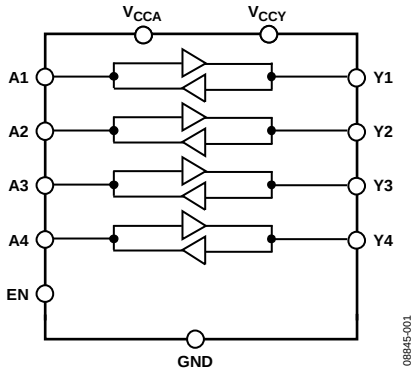

Figure 1.

GENERAL DESCRIPTIONS

The ADG3304-EP is a bidirectional logic level translator that contains four bidirectional channels. It can be used in multivoltage digital system applications, such as data transfer, between a low voltage digital signal processing controller and a higher voltage device using SPI and MICROWIRE interfaces. The internal architecture allows the device to perform bidirectional logic level translation without an additional signal to set the direction in which the translation takes place.

The voltage applied to V_{CCA} sets the logic levels on the A side of the device, while V_{CCY} sets the levels on the Y side. For proper operation, V_{CCA} must always be less than V_{CCY}. The V_{CCA}-compatible logic signals applied to the A side of the device appear as V_{CCY}-compatible levels on the Y side. Similarly, V_{CCY}-compatible logic levels applied to the Y side of the device appear as V_{CCA}-compatible logic levels on the A side.

The enable pin (EN) provides three-state operation on both the A side and the Y side pins. When the EN pin is pulled low, the terminals on both sides of the device are in the high impedance state. The EN pin is referred to the V_{CCA} supply voltage and driven high for normal operation.

The ADG3304-EP is available in compact 14-lead TSSOP package.

Full details about this enhanced product are available in the ADG3304 data sheet, which should be consulted in conjunction with this data sheet.

Rev. 0

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REVISION HISTORY

10/10—Revision 0: Initial Version

SPECIFICATIONS

V_{CCY} = 1.65 V to 5.5 V, V_{CCA} = 1.15 V to V_{CCY}, GND = 0 V, T_A = −55°C to +125°C unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ [1]	Max	Unit
LOGIC INPUTS/OUTPUTS						
A Side						
Input High Voltage[2]	V_{IHA}	V_{CCA} = 1.2 V + 0.1 V/−0.05 V	$V_{CCA} \times 0.88$			V
		V_{CCA} = 1.8 V ± 0.15 V	$V_{CCA} \times 0.72$			V
		V_{CCA} = 2.5 V ± 0.2 V	1.7			V
		V_{CCA} = 3.3 V ± 0.3 V	2.2			V
		V_{CCA} = 5 V ± 0.5 V	$V_{CCA} \times 0.7$			V
Input Low Voltage[2]	V_{ILA}	V_{CCA} = 1.2 V + 0.1 V/−0.05 V			$V_{CCA} \times 0.35$	V
		V_{CCA} = 1.8 V ± 0.15 V			$V_{CCA} \times 0.35$	V
		V_{CCA} = 2.5 V ± 0.2 V			0.7	V
		V_{CCA} = 3.3 V ± 0.3 V			0.8	V
		V_{CCA} = 5 V ± 0.5 V			$V_{CCA} \times 0.3$	V
Output High Voltage	V_{OHA}	$V_Y = V_{CCY}$, I_{OH} = 20 µA	V_{CCA} − 0.4			V
Output Low Voltage	V_{OLA}	V_Y = 0 V, I_{OL} = 20 µA			0.4	V
Capacitance[2]	C_A	f = 1 MHz, EN = 0		9		pF
Leakage Current	$I_{LA, Hi-Z}$	$V_A = 0\ V/V_{CCA}$, EN = 0			±1	µA
Y Side						
Input High Voltage[2]	V_{IHY}	V_{CCY} = 1.8 V ± 0.15 V	$V_{CCY} \times 0.67$			V
		V_{CCY} = 2.5 V ± 0.2 V	1.7			V
		V_{CCY} = 3.3 V ± 0.3 V	2			V
		V_{CCY} = 5 V ± 0.5 V	$V_{CCY} \times 0.7$			V
Input Low Voltage[2]	V_{ILY}	V_{CCY} = 1.8 V ± 0.15 V			$V_{CCY} \times 0.35$	V
		V_{CCY} = 2.5 V ± 0.2 V			0.7	V
		V_{CCY} = 3.3 V ± 0.3 V			0.8	V
		V_{CCY} = 5 V ± 0.5 V			$V_{CCY} \times 0.25$	V
Output High Voltage	V_{OHY}	$V_A = V_{CCA}$, I_{OH} = 20 µA	V_{CCY} − 0.4			V
Output Low Voltage	V_{OLY}	V_A = 0 V, I_{OL} = 20 µA			0.4	V
Capacitance[2]	C_Y	f = 1 MHz, EN = 0		6		pF
Leakage Current	$I_{LY, Hi-Z}$	$V_Y = 0\ V/V_{CCY}$, EN = 0			±1	µA
Enable (EN)						
Input High Voltage[2]	V_{IHEN}	V_{CCA} = 1.2 V + 0.1 V/−0.05 V	$V_{CCA} \times 0.88$			V
		V_{CCA} = 1.8 V ± 0.15 V	$V_{CCA} \times 0.72$			V
		V_{CCA} = 2.5 V ± 0.2 V	1.7			V
		V_{CCA} = 3.3 V ± 0.3 V	2.2			V
		V_{CCA} = 5 V ± 0.5 V	$V_{CCA} \times 0.7$			V
Input Low Voltage[2]	V_{ILEN}	V_{CCA} = 1.2 V + 0.1 V/−0.05 V			$V_{CCA} \times 0.35$	V
		V_{CCA} = 1.8 V ± 0.15 V			$V_{CCA} \times 0.35$	V
		V_{CCA} = 2.5 V ± 0.2 V			0.7	V
		V_{CCA} = 3.3 V ± 0.3 V			0.8	V
		V_{CCA} = 5 V ± 0.5 V			$V_{CCA} \times 0.3$	V
Leakage Current	I_{LEN}	$V_{EN} = 0\ V/V_{CCA}$, V_A = 0 V			±1	µA
Capacitance[2]	C_{EN}			3		pF
Enable Time[2]	t_{EN}	$R_S = R_T$ = 50 Ω $V_A = 0\ V/V_{CCA}$ (A→Y) $V_Y = 0\ V/V_{CCY}$ (Y→A)		1	1.8	µs

Parameter	Symbol	Test Conditions/Comments	Min	Typ [1]	Max	Unit
SWITCHING CHARACTERISTICS[2]						
3.3 V ± 0.3 V ≤ V_{CCA} ≤ V_{CCY}, V_{CCY} = 5 V ± 0.5 V						
A→Y Level Translation		$R_S = R_T = 50\ \Omega$, $C_L = 50$ pF				
Propagation Delay	$t_{P, A\rightarrow Y}$			6	15	ns
Rise Time	$t_{R, A\rightarrow Y}$			2	5	ns
Fall Time	$t_{F, A\rightarrow Y}$			2	5	ns
Maximum Data Rate	$D_{MAX, A\rightarrow Y}$			50		Mbps
Channel-to-Channel Skew	$t_{SKEW, A\rightarrow Y}$			2		ns
Part-to-Part Skew	$t_{PPSKEW, A\rightarrow Y}$			3		ns
Y→A Level Translation		$R_S = R_T = 50\ \Omega$, $C_L = 15$ pF				
Propagation Delay	$t_{P, Y\rightarrow A}$			4	10	ns
Rise Time	$t_{R, Y\rightarrow A}$			1	5	ns
Fall Time	$t_{F, Y\rightarrow A}$			3	10	ns
Maximum Data Rate	$D_{MAX, Y\rightarrow A}$			50		Mbps
Channel-to-Channel Skew	$t_{SKEW, Y\rightarrow A}$			2		ns
Part-to-Part Skew	$t_{PPSKEW, Y\rightarrow A}$			2		ns
1.8 V ± 0.15 V ≤ V_{CCA} ≤ V_{CCY}, V_{CCY} = 3.3 V ± 0.3 V						
A→Y Translation		$R_S = R_T = 50\ \Omega$, $C_L = 50$ pF				
Propagation Delay	$t_{P, A\rightarrow Y}$			8	15	ns
Rise Time	$t_{R, A\rightarrow Y}$			2	8	ns
Fall Time	$t_{F, A\rightarrow Y}$			2	8	ns
Maximum Data Rate	$D_{MAX, A\rightarrow Y}$			50		Mbps
Channel-to-Channel Skew	$t_{SKEW, A\rightarrow Y}$			2		ns
Part-to-Part Skew	$t_{PPSKEW, A\rightarrow Y}$			4		ns
Y→A Translation		$R_S = R_T = 50\ \Omega$, $C_L = 15$ pF				
Propagation Delay	$t_{P, Y\rightarrow A}$			5	12	ns
Rise Time	$t_{R, Y\rightarrow A}$			2	5	ns
Fall Time	$t_{F, Y\rightarrow A}$			2	5	ns
Maximum Data Rate	$D_{MAX, Y\rightarrow A}$			50		Mbps
Channel-to-Channel Skew	$t_{SKEW, Y\rightarrow A}$			2		ns
Part-to-Part Skew	$t_{PPSKEW, Y\rightarrow A}$			3		ns
1.15 V to 1.3 V ≤ V_{CCA} ≤ V_{CCY}, V_{CCY} = 3.3 V ± 0.3 V						
A→Y Translation		$R_S = R_T = 50\ \Omega$, $C_L = 50$ pF				
Propagation Delay	$t_{P, A\rightarrow Y}$			9	27	ns
Rise Time	$t_{R, A\rightarrow Y}$			3	8	ns
Fall Time	$t_{F, A\rightarrow Y}$			2	8	ns
Maximum Data Rate	$D_{MAX, A\rightarrow Y}$			40		Mbps
Channel-to-Channel Skew	$t_{SKEW, A\rightarrow Y}$			2		ns
Part-to-Part Skew	$t_{PPSKEW, A\rightarrow Y}$			10		ns
Y→A Translation		$R_S = R_T = 50\ \Omega$, $C_L = 15$ pF				
Propagation Delay	$t_{P, Y\rightarrow A}$			5	13	ns
Rise Time	$t_{R, Y\rightarrow A}$			2	6	ns
Fall Time	$t_{F, Y\rightarrow A}$			2	6	ns
Maximum Data Rate	$D_{MAX, Y\rightarrow A}$			40		Mbps
Channel-to-Channel Skew	$t_{SKEW, Y\rightarrow A}$			2		ns
Part-to-Part Skew	$t_{PPSKEW, Y\rightarrow A}$			4		ns

Parameter	Symbol	Test Conditions/Comments	Min	Typ [1]	Max	Unit
1.15 V to 1.3 V ≤ V_{CCA} ≤ V_{CCY}, V_{CCY} = 1.8 V ± 0.3 V						
A→Y Translation		$R_S = R_T = 50\ \Omega$, $C_L = 50$ pF				
Propagation Delay	$t_{P, A\rightarrow Y}$			12	35	ns
Rise Time	$t_{R, A\rightarrow Y}$			7	18	ns
Fall Time	$t_{F, A\rightarrow Y}$			3	8	ns
Maximum Data Rate	$D_{MAX, A\rightarrow Y}$			25		Mbps
Channel-to-Channel Skew	$t_{SKEW, A\rightarrow Y}$			2		ns
Part-to-Part Skew	$t_{PPSKEW, A\rightarrow Y}$			15		ns
Y→A Translation		$R_S = R_T = 50\ \Omega$, $C_L = 15$ pF				
Propagation Delay	$t_{P, Y\rightarrow A}$			14	40	ns
Rise Time	$t_{R, Y\rightarrow A}$			5	24	ns
Fall Time	$t_{F, Y\rightarrow A}$			2.5	10	ns
Maximum Data Rate	$D_{MAX, Y\rightarrow A}$			25		Mbps
Channel-to-Channel Skew	$t_{SKEW, Y\rightarrow A}$			3		ns
Part-to-Part Skew	$t_{PPSKEW, Y\rightarrow A}$			23.5		ns
2.5 V ± 0.2 V ≤ V_{CCA} ≤ V_{CCY}, V_{CCY} = 3.3 V ± 0.3 V						
A→Y Translation		$R_S = R_T = 50\ \Omega$, $C_L = 50$ pF				
Propagation Delay	$t_{P, A\rightarrow Y}$			7	15	ns
Rise Time	$t_{R, A\rightarrow Y}$			2.5	6	ns
Fall Time	$t_{F, A\rightarrow Y}$			2	8	ns
Maximum Data Rate	$D_{MAX, A\rightarrow Y}$			60		Mbps
Channel-to-Channel Skew	$t_{SKEW, A\rightarrow Y}$			1.5		ns
Part-to-Part Skew	$t_{PPSKEW, A\rightarrow Y}$			4		ns
Y→A Translation		$R_S = R_T = 50\ \Omega$, $C_L = 15$ pF				
Propagation Delay	$t_{P, Y\rightarrow A}$			5	12	ns
Rise Time	$t_{R, Y\rightarrow A}$			1	6	ns
Fall Time	$t_{F, Y\rightarrow A}$			3	8	ns
Maximum Data Rate	$D_{MAX, Y\rightarrow A}$			60		Mbps
Channel-to-Channel Skew	$t_{SKEW, Y\rightarrow A}$			2		ns
Part-to-Part Skew	$t_{PPSKEW, Y\rightarrow A}$			3		ns
POWER REQUIREMENTS						
Power Supply Voltages	V_{CCA}	$V_{CCA} \le V_{CCY}$	1.15		5.5	V
	V_{CCY}		1.65		5.5	V
Quiescent Power Supply Current	I_{CCA}	V_A = 0 V/V_{CCA}, V_Y = 0 V/V_{CCY}, $V_{CCA} = V_{CCY}$ = 5.5 V, EN = 1		0.17	5	µA
	I_{CCY}	V_A = 0 V/V_{CCA}, V_Y = 0 V/V_{CCY}, $V_{CCA} = V_{CCY}$ = 5.5 V, EN = 1		0.27	5	µA
Three-State Mode Power Supply Current	$I_{Hi\text{-}Z, A}$	$V_{CCA} = V_{CCY}$ = 5.5 V, EN = 0		0.1	5	µA
	$I_{Hi\text{-}Z, Y}$	$V_{CCA} = V_{CCY}$ = 5.5 V, EN = 0		0.1	5	µA

[1] T_A for typical specifications is +25°C.
[2] Guaranteed by design, not production tested.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Rating
V_{CCA} to GND	−0.3 V to +7 V
V_{CCY} to GND	V_{CCA} to +7 V
Digital Inputs (A)	−0.3 V to (V_{CCA} + 0.3 V)
Digital Inputs (Y)	−0.3 V to (V_{CCY} + 0.3 V)
EN to GND	−0.3 V to +7 V
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance (4-Layer Board)	
14-Lead TSSOP	112.6°C/W
Lead Temperature, Soldering	
Vapor phase(60 sec)	215°C
Infrared (15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating can be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

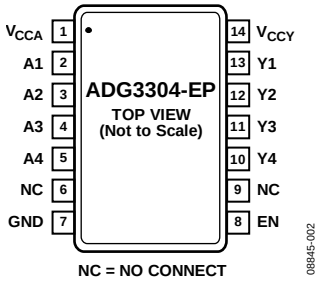

Figure 2. 14-Lead TSSOP Pin Configuration

Table 3. 14-Lead TSSOP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{CCA}	Power Supply Voltage Input for the A1 to A4 I/O Pins (1.15 V ≤ V_{CCA} ≤ V_{CCY}).
2	A1	Input/Output A1. Referenced to V_{CCA}.
3	A2	Input/Output A2. Referenced to V_{CCA}.
4	A3	Input/Output A3. Referenced to V_{CCA}.
5	A4	Input/Output A4. Referenced to V_{CCA}.
6, 9	NC	No Connect.
7	GND	Ground.
8	EN	Active High Enable Input.
10	Y4	Input/Output Y4. Referenced to V_{CCY}.
11	Y3	Input/Output Y3. Referenced to V_{CCY}.
12	Y2	Input/Output Y2. Referenced to V_{CCY}.
13	Y1	Input/Output Y1. Referenced to V_{CCY}.
14	V_{CCY}	Power Supply Voltage Input for the Y1 to Y4 I/O Pins (1.65 V ≤ V_{CC} ≤ 5.5 V).

Table 4. Truth Table

EN	Y I/O Pins	A I/O Pins
0	Hi-Z[1]	Hi-Z[1]
1	Normal operation[2]	Normal operation[2]

[1] High impedance state.
[2] In normal operation, the ADG3304-EP performs level translation.

OUTLINE DIMENSIONS

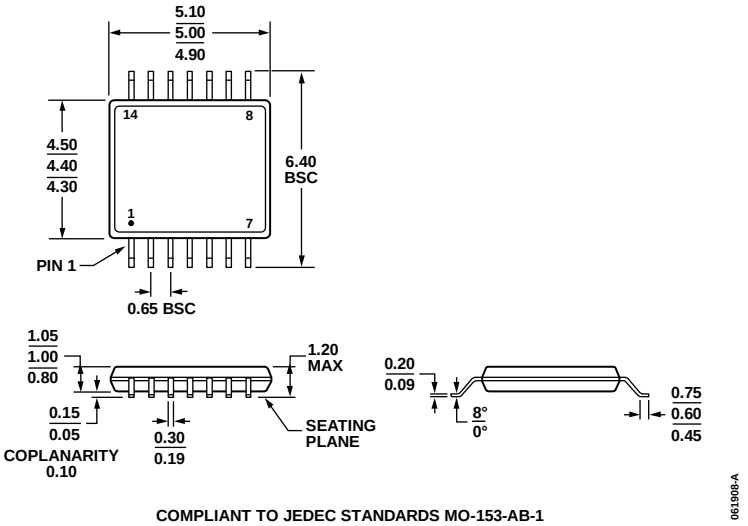

Figure 3. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG3304SRU-EP-RL7	−55°C to +125°C	14-Lead Thin Shrink Small Outline Package [TSSOP]	RU-14

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