

# RF Power Field Effect Transistors

## N-Channel Enhancement-Mode Lateral MOSFETs

Designed for broadband commercial and industrial applications with frequencies from 1930 to 1990 MHz. The high gain and broadband performance of these devices make them ideal for large-signal, common-source amplifier applications in 28 Volt base station equipment.

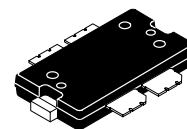
- Typical 2-carrier N-CDMA Performance:  $V_{DD} = 28$  Volts,  $I_{DQ} = 750$  mA,  $P_{out} = 12$  Watts Avg., 1990 MHz, IS-95 (Pilot, Sync, Paging, Traffic Codes 8 Through 13) Channel Bandwidth = 1.2288 MHz. PAR = 9.8 dB @ 0.01% Probability on CCDF.  
Power Gain — 14 dB  
Drain Efficiency — 23%  
IM3 @ 2.5 MHz Offset — -37 dBc in 1.2288 MHz Channel Bandwidth  
ACPR @ 885 kHz Offset — -51 dBc in 30 kHz Channel Bandwidth
- Capable of Handling 5:1 VSWR, @ 28 Vdc, 1960 MHz, 12 Watts CW Output Power

### Features

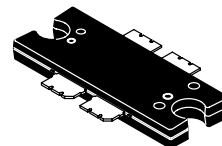
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Internally Matched for Ease of Use
- Integrated ESD Protection
- 200°C Capable Plastic Package
- N Suffix Indicates Lead-Free Terminations. RoHS Compliant.
- In Tape and Reel. R1 Suffix = 500 Units per 44 mm, 13 inch Reel.

**MRF5S19060NR1**  
**MRF5S19060NBR1**

**1930-1990 MHz, 12 W AVG., 28 V**  
**2 x N-CDMA**  
**LATERAL N-CHANNEL**  
**RF POWER MOSFETs**



**CASE 1486-03, STYLE 1**  
**TO-270 WB-4**  
**PLASTIC**  
**MRF5S19060NR1**



**CASE 1484-04, STYLE 1**  
**TO-272 WB-4**  
**PLASTIC**  
**MRF5S19060NBR1**

**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	-0.5, +65	Vdc
Gate-Source Voltage	$V_{GS}$	-0.5, +15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	$P_D$	218.8 1.25	W W/°C
Storage Temperature Range	$T_{stg}$	- 65 to +175	°C
Operating Junction Temperature	$T_J$	200	°C

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value (1,2)	Unit
Thermal Resistance, Junction to Case Case Temperature 75°C, 12 W CW	$R_{\theta JC}$	0.80	°C/W

1. MTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTF calculators by product.
2. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1955.

**Table 3. ESD Protection Characteristics**

Test Methodology	Class
Human Body Model (per JESD22-A114)	1C (Minimum)
Machine Model (per EIA/JESD22-A115)	C (Minimum)
Charge Device Model (per JESD22-C101)	IV (Minimum)

**Table 4. Moisture Sensitivity Level**

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD 22-A113, IPC/JEDEC J-STD-020	3	260	°C

**Table 5. Electrical Characteristics** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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**Off Characteristics**

Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 65\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	10	$\mu\text{Adc}$
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 28\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	1	$\mu\text{Adc}$
Gate-Source Leakage Current ( $V_{GS} = 5\text{ Vdc}$ , $V_{DS} = 0\text{ Vdc}$ )	$I_{GSS}$	—	—	1	$\mu\text{Adc}$

**On Characteristics**

Gate Threshold Voltage ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 225\ \mu\text{Adc}$ )	$V_{GS(th)}$	2.5	—	3.5	Vdc
Gate Quiescent Voltage ( $V_{DS} = 28\text{ Vdc}$ , $I_D = 750\text{ mAdc}$ )	$V_{GS(Q)}$	—	3.8	—	Vdc
Drain-Source On-Voltage ( $V_{GS} = 5\text{ Vdc}$ , $I_D = 2.25\text{ Adc}$ )	$V_{DS(on)}$	—	0.26	—	Vdc
Forward Transconductance ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 2.25\text{ Adc}$ )	$g_{fs}$	—	5	—	S

**Dynamic Characteristics (1)**

Reverse Transfer Capacitance ( $V_{DS} = 28\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$ )	$C_{rss}$	—	1.5	—	pF
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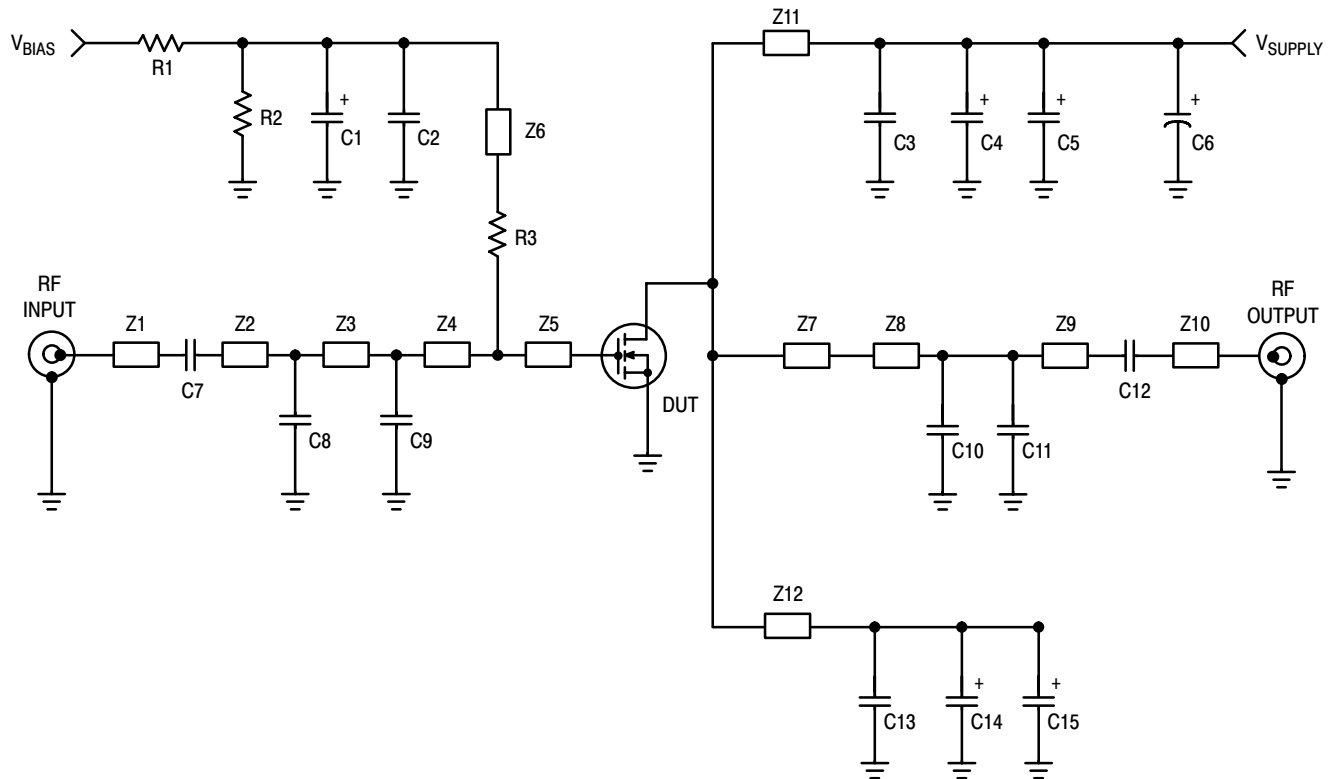
**Functional Tests** (In Freescale Test Fixture, 50 ohm system)  $V_{DD} = 28\text{ Vdc}$ ,  $I_{DQ} = 750\text{ mA}$ ,  $P_{out} = 12\text{ W Avg.}$ ,  $f_1 = 1987.5\text{ MHz}$ ,  $f_2 = 1990\text{ MHz}$ , 2-carrier N-CDMA, 1.2288 MHz Channel Bandwidth Carriers. ACPR measured in 30 kHz Channel Bandwidth @  $\pm 885\text{ kHz}$  Offset. IM3 measured in 1.2288 MHz Channel Bandwidth @  $\pm 2.5\text{ MHz}$  Offset. PAR = 9.8 dB @ 0.01% Probability on CCDF.

Power Gain	$G_{ps}$	12.5	14	16	dB
Drain Efficiency	$\eta_D$	21	23	—	%
Intermodulation Distortion	IM3	—	-37	-35	dBc
Adjacent Channel Power Ratio	ACPR	—	-51	-48	dBc
Input Return Loss	IRL	—	-12	-9	dB

**Typical RF Performance** (50 ohm system)

Pulse Peak Power ( $V_{DD} = 28\text{ Vdc}$ , 1-Tone CW Pulsed, $I_{DQ} = 750\text{ mA}$ , $t_{ON} = 8\ \mu\text{s}$ , 1% Duty Cycle)	$P_{sat}$	—	110	—	W
Video Bandwidth ( $V_{DD} = 28\text{ Vdc}$ , $P_{out} = 60\text{ W PEP}$ , $I_{DQ} = 750\text{ mA}$ , Tone Spacing = 1 MHz to VBW, $\Delta\text{IM3} < 2\text{ dB}$ )	VBW	—	35	—	MHz

1. Part is internally matched both on input and output.



Z1 0.250" x 0.083" Microstrip  
 Z2\* 0.500" x 0.083" Microstrip  
 Z3\* 0.500" x 0.083" Microstrip  
 Z4\* 0.515" x 0.083" Microstrip  
 Z5 0.480" x 1.000" Microstrip  
 Z6 1.140" x 0.080" Microstrip  
 Z7 0.600" x 1.000" Microstrip

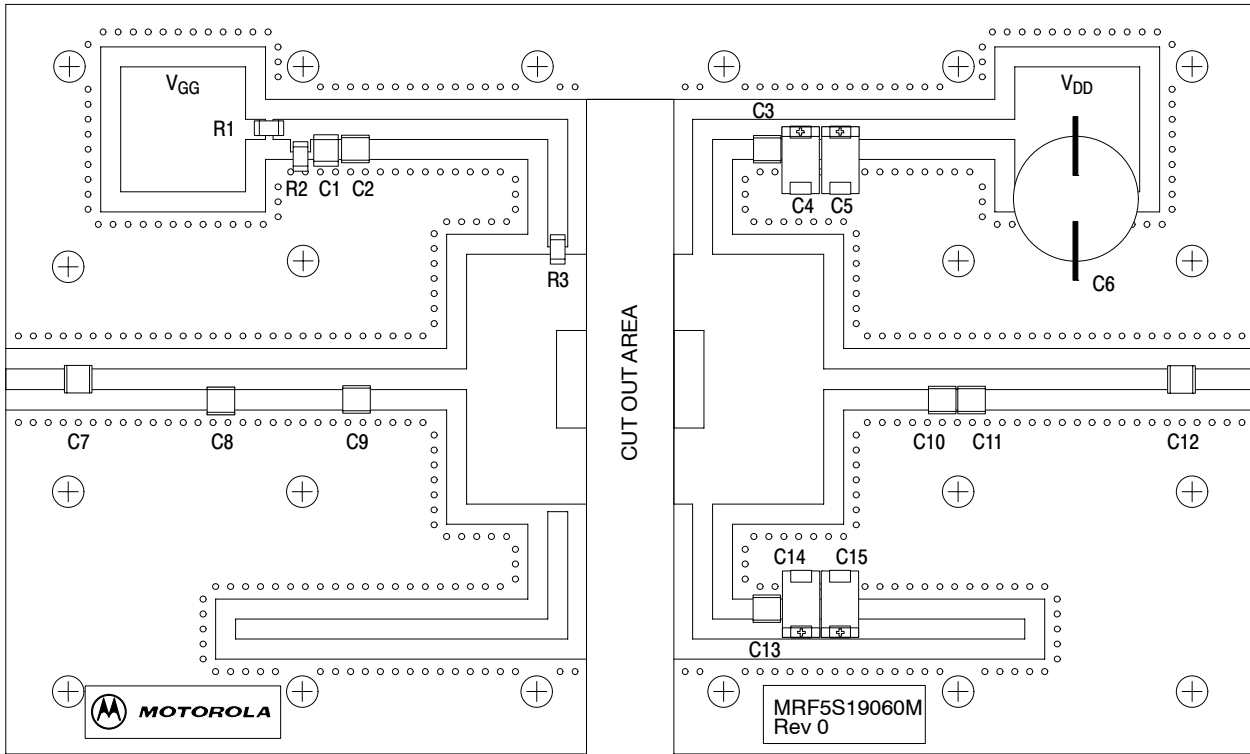
Z8\* 0.420" x 0.083" Microstrip  
 Z9\* 0.975" x 0.083" Microstrip  
 Z10 0.250" x 0.083" Microstrip  
 Z11 0.700" x 0.080" Microstrip  
 Z12 0.700" x 0.080" Microstrip  
 PCB Taconic TLX8-0300, 0.030",  $\epsilon_r = 2.55$

\* Variable for tuning

**Figure 1. MRF5S19060NR1/NBR1 Test Circuit Schematic**

**Table 6. MRF5S19060NR1/NBR1 Test Circuit Component Designations and Values**

Part	Description	Part Number	Manufacturer
C1	1 $\mu$ F, 35 V Tantalum Capacitor	TAJB105K35S	AVX
C2	10 pF 100B Chip Capacitor	ATC100B10R0CT500XT	ATC
C3, C7, C12, C13	6.8 pF 100B Chip Capacitors	ATC100B6R8CT500XT	ATC
C4, C5, C14, C15	10 $\mu$ F, 35 V Tantalum Capacitors	TAJD106K035S	AVX
C6	220 $\mu$ F, 63 V Electrolytic Capacitor, Radial	2222-136-68221	Vishay
C8	0.8 pF 100B Chip Capacitor	ATC100B0R8BT500XT	ATC
C9	1.5 pF 100B Chip Capacitor	ATC100B1R5BT500XT	ATC
C10	1.0 pF 100B Chip Capacitor	ATC100B1R0BT500XT	ATC
C11	0.2 pF 100B Chip Capacitor	ATC100B0R2BT500XT	ATC
R1, R2	10 k $\Omega$ , 1/4 W Chip Resistors	CRCW12061002FKEA	Vishay
R3	10 $\Omega$ , 1/4 W Chip Resistors	CRCW120610R0FKEA	Vishay



Freescall has begun the transition of marking Printed Circuit Boards (PCBs) with the Freescall Semiconductor signature/logo. PCBs may have either Motorola or Freescall markings during the transition period. These changes will have no impact on form, fit or function of the current product.

**Figure 2. MRF5S19060NR1/NBR1 Test Circuit Component Layout**

### TYPICAL CHARACTERISTICS

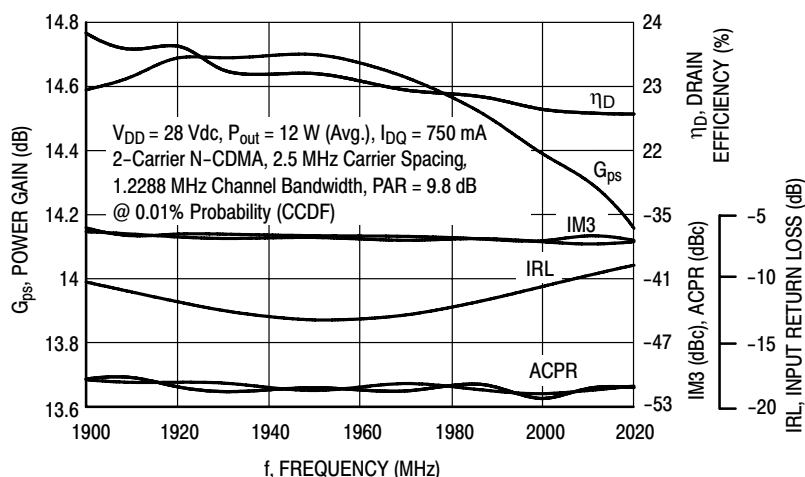


Figure 3. 2-Carrier N-CDMA Broadband Performance @  $P_{out} = 12 \text{ Watts Avg.}$

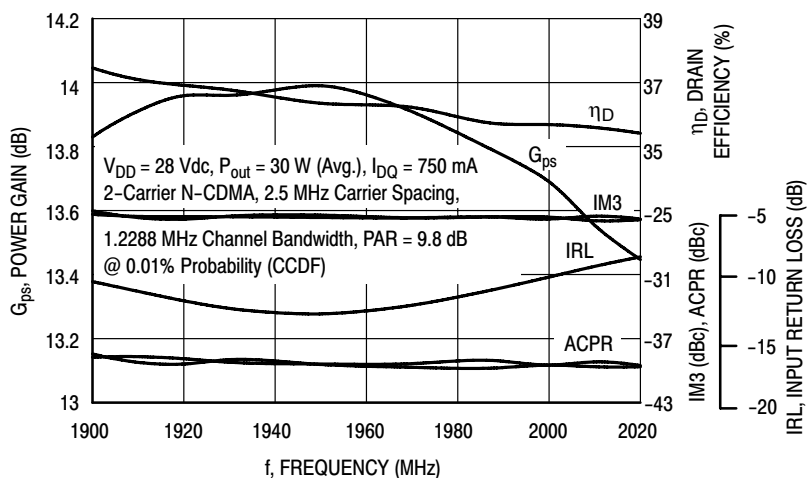


Figure 4. 2-Carrier N-CDMA Broadband Performance @  $P_{out} = 30 \text{ Watts Avg.}$

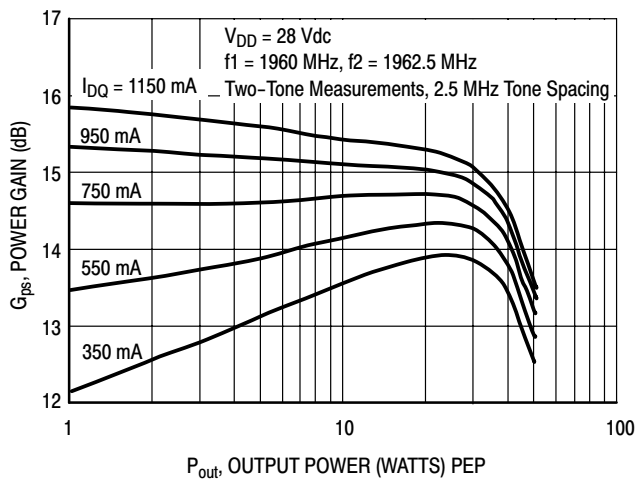


Figure 5. Two-Tone Power Gain versus Output Power

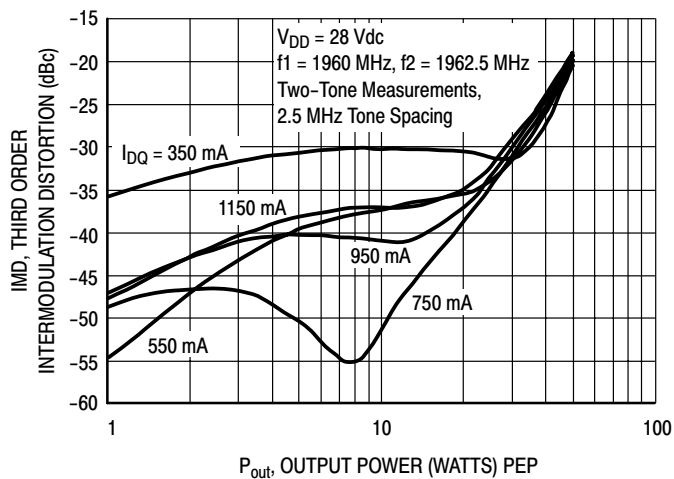
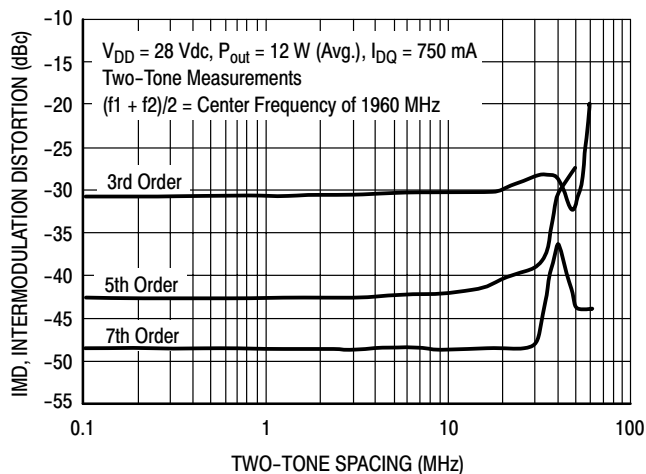
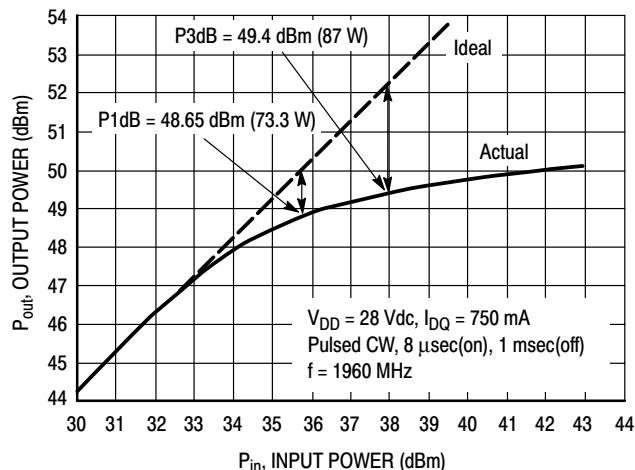


Figure 6. Third Order Intermodulation Distortion versus Output Power

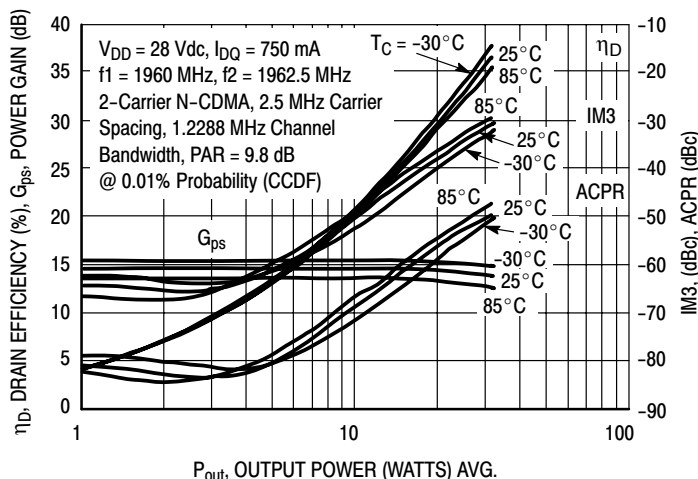
## TYPICAL CHARACTERISTICS



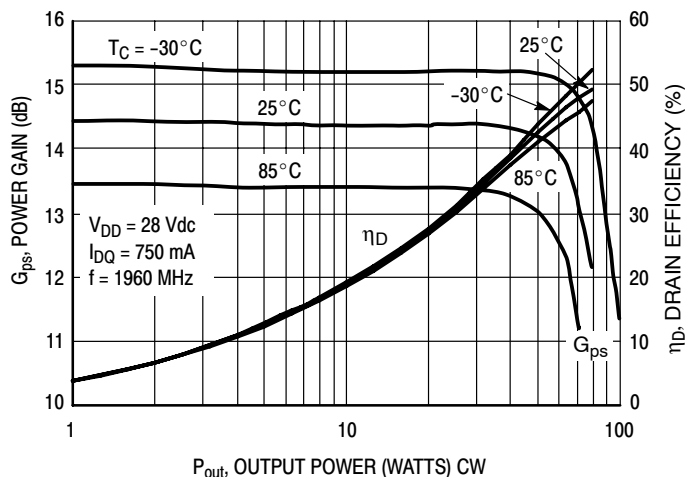
**Figure 7. Intermodulation Distortion Products versus Tone Spacing**



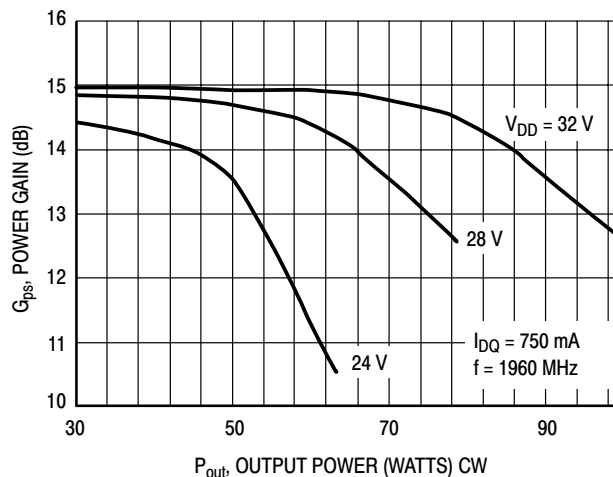
**Figure 8. Pulse CW Output Power versus Input Power**



**Figure 9. 2-Carrier N-CDMA ACPR, IM3, Power Gain and Drain Efficiency versus Output Power**



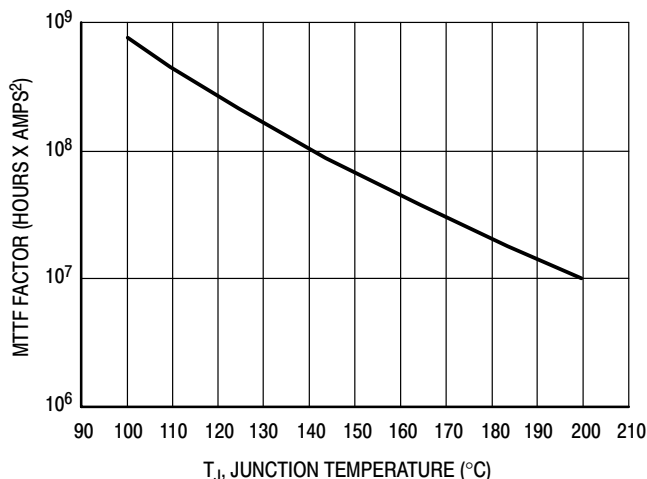
**Figure 10. Power Gain and Drain Efficiency versus CW Output Power**



**Figure 11. Power Gain versus Output Power**

MRF5S19060NR1 MRF5S19060NBR1

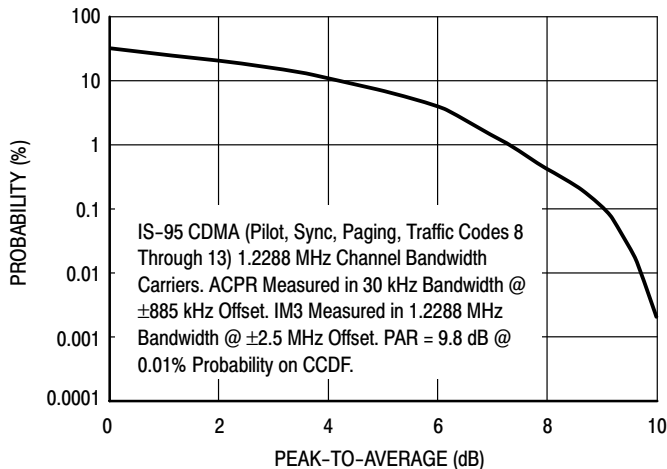
## TYPICAL CHARACTERISTICS



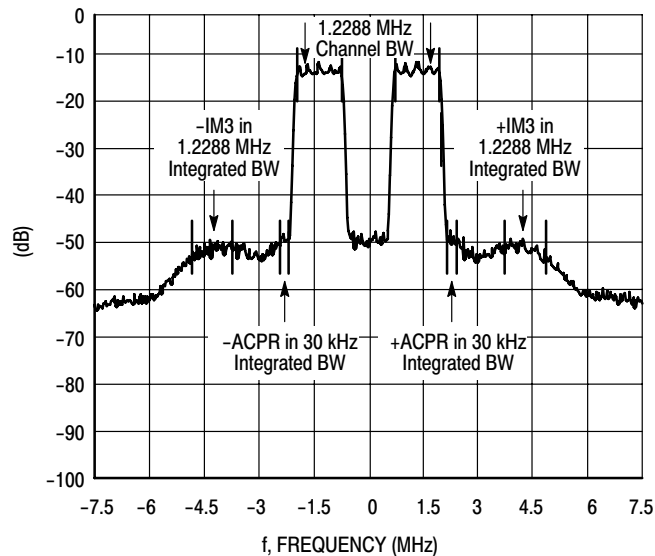
This above graph displays calculated MTTF in hours x ampere<sup>2</sup> drain current. Life tests at elevated temperatures have correlated to better than ±10% of the theoretical prediction for metal failure. Divide MTTF factor by  $I_D^2$  for MTTF in a particular application.

**Figure 12. MTTF Factor versus Junction Temperature**

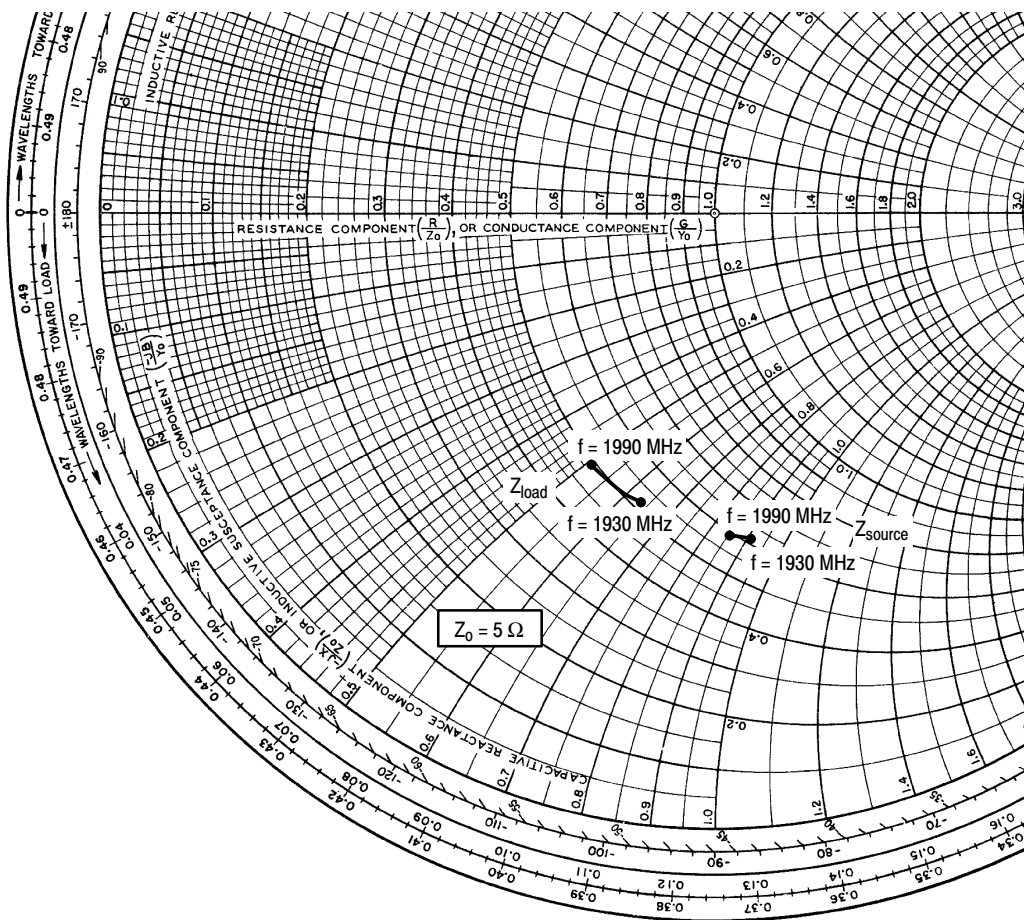
## N-CDMA TEST SIGNAL



**Figure 13. 2-Carrier CCDF N-CDMA**



**Figure 14. 2-Carrier N-CDMA Spectrum**



$V_{DD} = 28 \text{ Vdc}$ ,  $I_{DQ} = 750 \text{ mA}$ ,  $P_{out} = 12 \text{ W Avg.}$

f MHz	$Z_{source}$ $\Omega$	$Z_{load}$ $\Omega$
1930	$3.11 - j4.55$	$2.60 - j3.18$
1960	$3.06 - j4.38$	$2.50 - j2.85$
1990	$2.93 - j4.28$	$2.44 - j2.53$

$Z_{source}$  = Test circuit impedance as measured from gate to ground.

$Z_{load}$  = Test circuit impedance as measured from drain to ground.

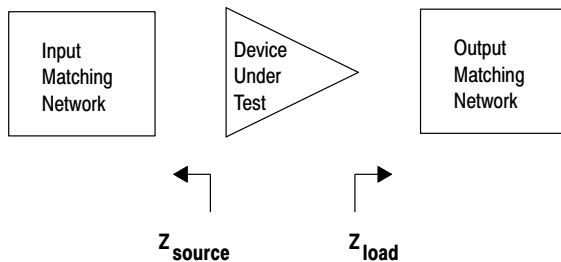
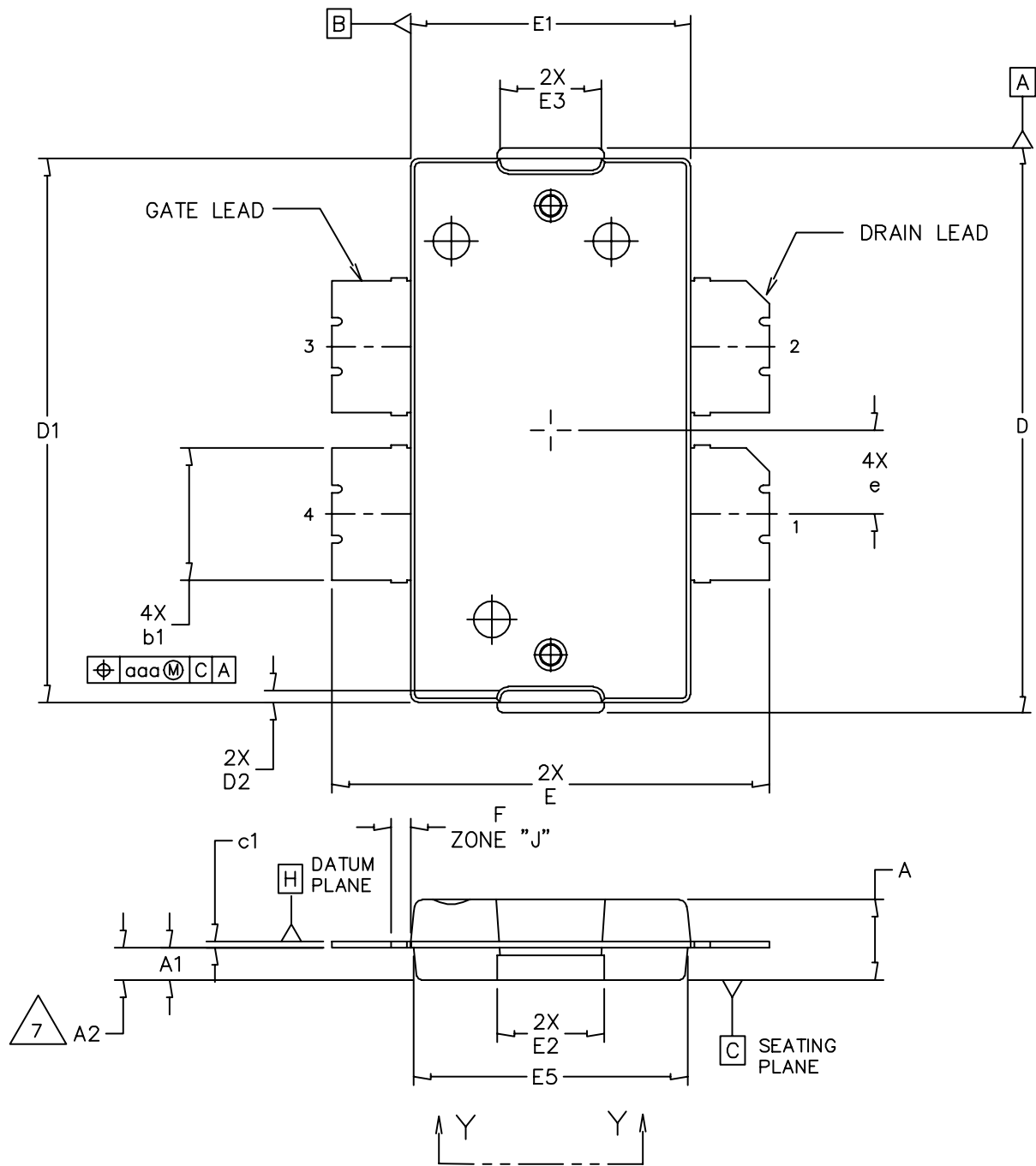


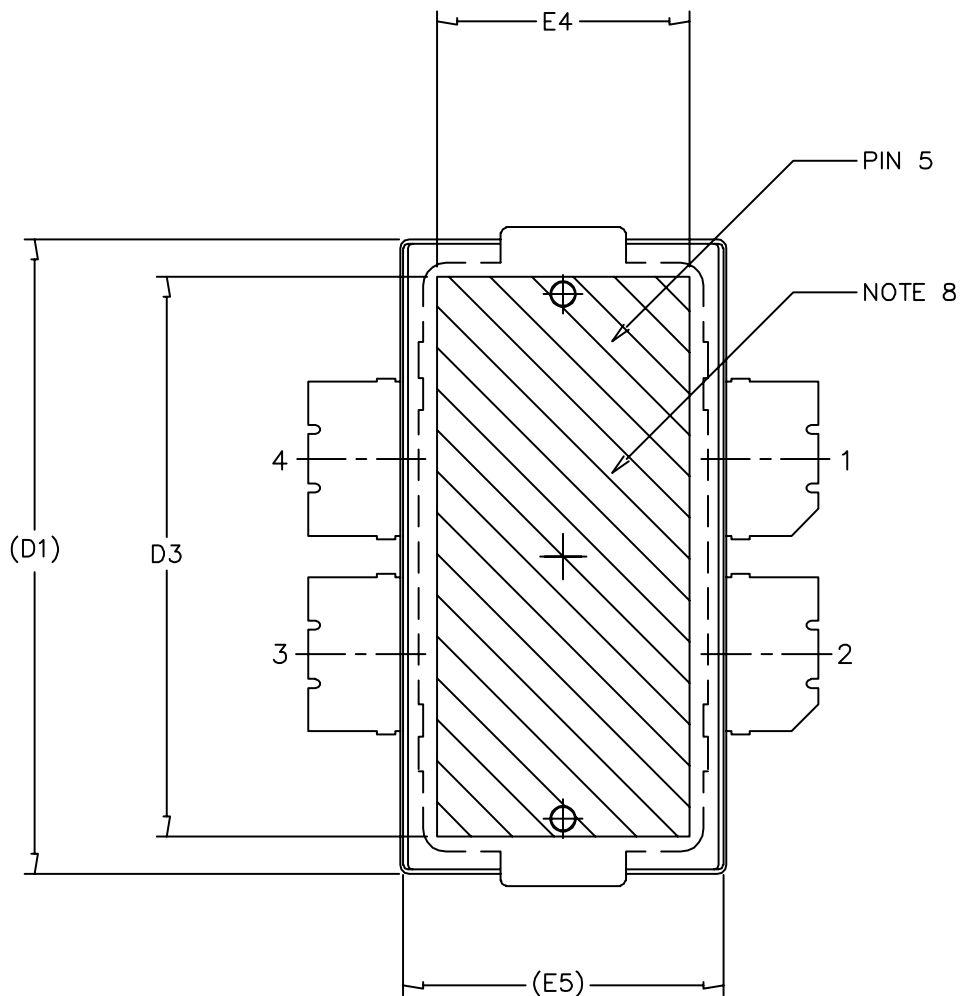
Figure 15. Series Equivalent Source and Load Impedance



**PACKAGE DIMENSIONS**



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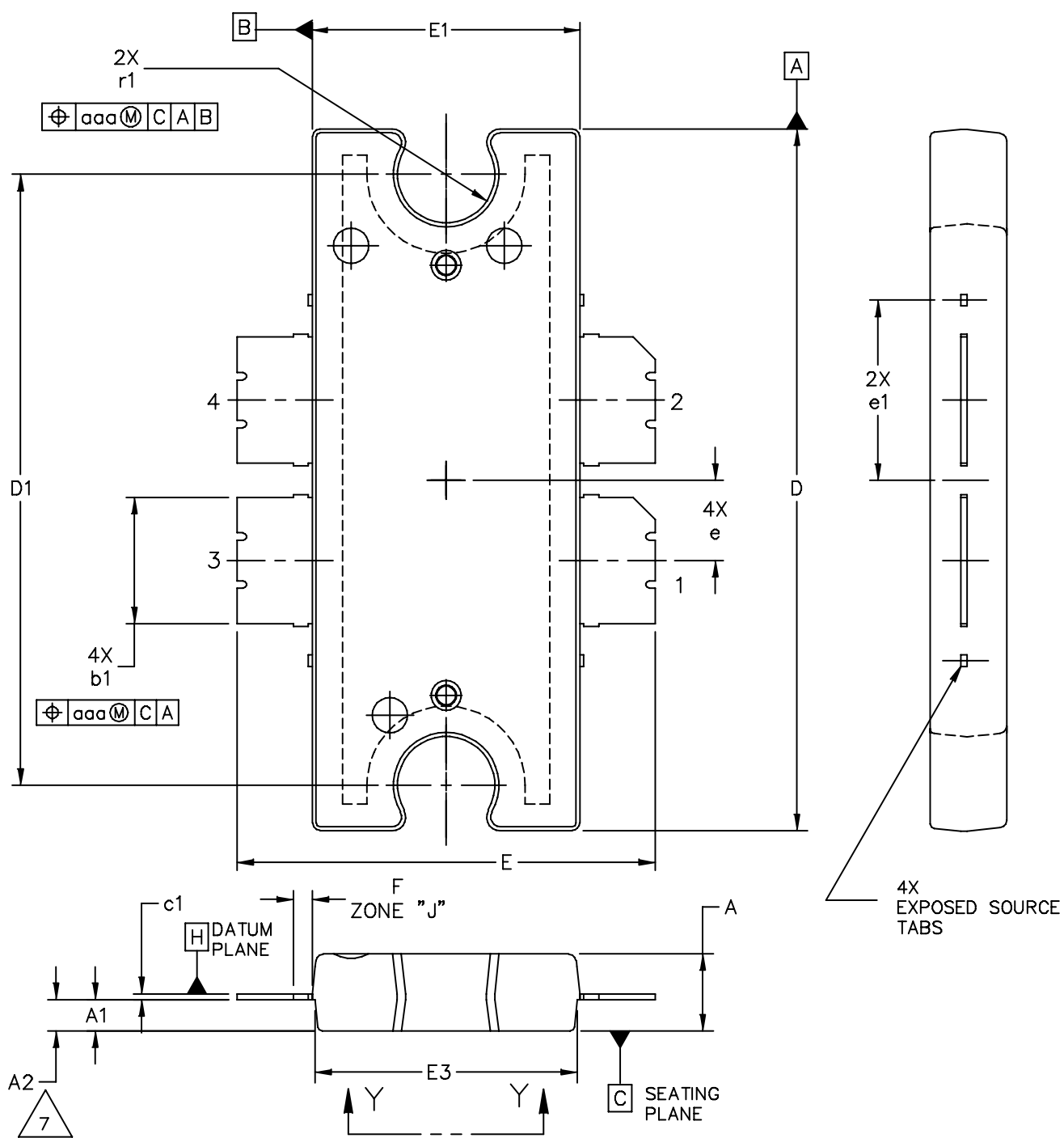
NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.
8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

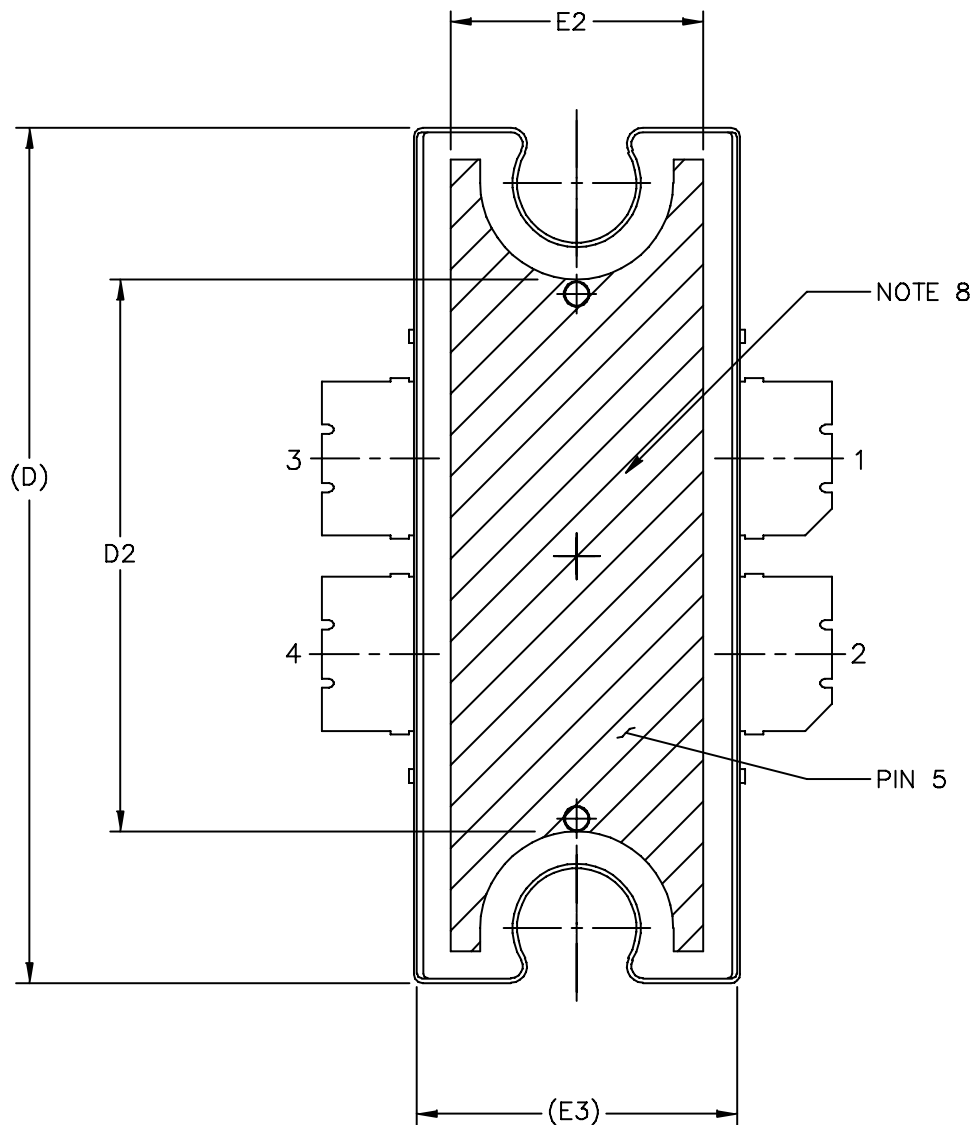
STYLE 1:

PIN 1 - DRAIN      PIN 2 - DRAIN  
 PIN 3 - GATE      PIN 4 - GATE  
 PIN 5 - SOURCE

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	F	.025 BSC		0.64 BSC	
A1	.039	.043	0.99	1.09	b1	.164	.170	4.17	4.32
A2	.040	.042	1.02	1.07	c1	.007	.011	.18	.28
D	.712	.720	18.08	18.29	e	.106 BSC		2.69 BSC	
D1	.688	.692	17.48	17.58	aaa	.004		.10	
D2	.011	.019	0.28	0.48					
D3	.600	---	15.24	---					
E	.551	.559	14	14.2					
E1	.353	.357	8.97	9.07					
E2	.132	.140	3.35	3.56					
E3	.124	.132	3.15	3.35					
E4	.270	---	6.86	---					
E5	.346	.350	8.79	8.89					
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NOTES:

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2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE H IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUM A AND B TO BE DETERMINED AT DATUM PLANE H.
7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.
8. HATCHING REPRESENTS EXPOSED AREA OF THE HEAT SLUG. HATCHED AREA SHOWN IS ON THE SAME PLANE.

STYLE 1:  
 PIN 1 - DRAIN      PIN 2 - DRAIN  
 PIN 3 - GATE      PIN 4 - GATE  
 PIN 5 - SOURCE

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	b1	.164	.170	4.17	4.32
A1	.039	.043	0.99	1.09	c1	.007	.011	.18	.28
A2	.040	.042	1.02	1.07	r1	.063	.068	1.60	1.73
D	.928	.932	23.57	23.67	e	.106 BSC		2.69 BSC	
D1	.810 BSC		20.57 BSC		e1	.239 INFO ONLY		6.07 INFO ONLY	
D2	.600	---	15.24	---	aaa	.004		.10	
E	.551	.559	14	14.2					
E1	.353	.357	8.97	9.07					
E2	.270	---	6.86	---					
E3	.346	.350	8.79	8.89					
F	.025 BSC		0.64 BSC						

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	STANDARD: NON-JEDEC		

## PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

### Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

### Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

## REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
7	Oct. 2008	<ul style="list-style-type: none"> <li>• Modified data sheet to reflect RF Test Reduction described in Product and Process Change Notification number, PCN12779, p. 1, 2</li> <li>• Updated Part Numbers in Table 6, Component Designations and Values, to RoHS compliant part numbers, p. 3</li> <li>• Replaced Case Outline 1486-03, Issue C, with 1486-03, Issue D, p. 9-11. Added pin numbers 1 through 4 on Sheet 1.</li> <li>• Replaced Case Outline 1484-04, Issue D, with 1484-04, Issue E, p. 12-14. Added pin numbers 1 through 4 on Sheet 1, replacing Gate and Drain notations with Pin 1 and Pin 2 designations.</li> <li>• Added Product Documentation and Revision History, p. 15</li> </ul>

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