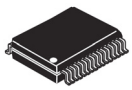
Document Number: MC12XSFD1
Rev. 1.0, 8/2016

17 mOhm and 7.0 mOhm high-side switches

12XSFD1

HIGH-SIDE SWITCHES

EK SUFFIX (PB-FREE)
98ASA00367D
54-PIN SOIC-EP



EK SUFFIX (PB-FREE)
98ASA00368D
32-PIN SOIC-EP

The 12XSF is the latest SMARTMOS achievement in DC motors and lighting drivers. It belongs to an expanding family that helps to control and diagnose incandescent lamps and light-emitting diodes (LEDs), with enhanced precision. It combines flexibility through daisy chainable SPI 5.0 MHz, extended digital and analog feedbacks, safety, and robustness.

Output edge shaping helps to improve electromagnetic performance. To avoid shutting off the device upon inrush current, while still being able to closely track the load current, a dynamic overcurrent threshold profile is featured. Current of each channel can be sensed with a programmable sensing ratio. Whenever communication with the external microcontroller is lost, the device enters a Fail operation mode, but remains operational, controllable, and protected.

This new generation of high-side switch products family facilitates ECU design due to compatible MCU software and PCB foot prints for each device variant.

Features

- Quad or penta high-side switches with high transient capability
- 16-bit 5.0 MHz SPI control of overcurrent profiles, channel control including PWM duty-cycles, output-ON and -OFF open load detections, thermal shutdown and prewarning, and fault reporting
- Output current monitoring with programmable synchronization signal and supply voltage feedback
- Limp home mode
- External smart power switch control
- Operating voltage is 7.0 V to 18 V with sleep current < 5.0 µA, extended mode from 6.0 V to 28 V
- -16 V reverse polarity and ground disconnect protections
- Compatible PCB foot print and SPI software driver among the family

Applications

- Low-voltage exterior lighting
- Low-voltage industrial lighting
- Halogen lamps
- Incandescent bulbs
- Light-emitting diodes (LEDs)
- HID Xenon ballasts
- DC motors
- Low voltage automation systems

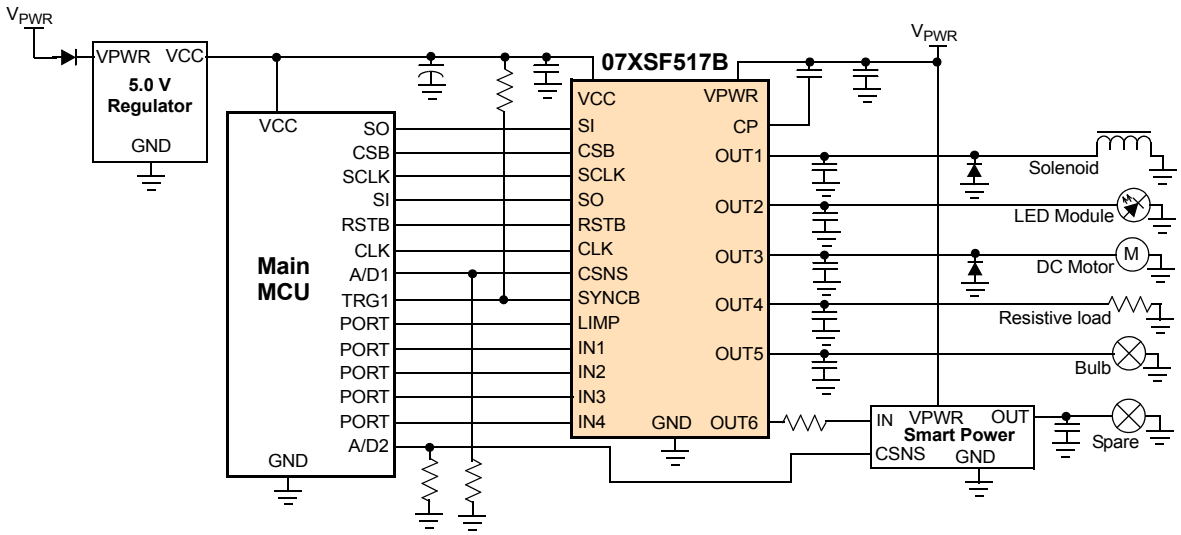


Figure 1. Triple 7.0 mΩ and dual 17 mΩ high-side simplified application diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

1 Orderable parts

This section describes the part numbers available to be purchased along with their differences. Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to http://www.nxp.com and perform a part number search for the following device numbers.

Table 1. Orderable part variations

Part number	Notes	Temperature (T_A)	Package	OUT1 $R_{DS(on)}$	OUT2 $R_{DS(on)}$	OUT3 $R_{DS(on)}$	OUT4 $R_{DS(on)}$	OUT5 $R_{DS(on)}$	OUT6
MC07XSF517BEK	(1)	-40 °C to 125 °C	SOIC54 pins exposed pad	17 mΩ	17 mΩ	7.0 mΩ	7.0 mΩ	7.0 mΩ	Yes
MC17XSF500BEK			SOIC32 pins exposed pad	17 mΩ	17 mΩ	17 mΩ	17 mΩ	17 mΩ	Yes
MC17XSF400EK				17 mΩ	17 mΩ	17 mΩ	17 mΩ	No	Yes

Notes

1. To order parts in Tape and Reel, add the R2 suffix to the part number.

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2 Internal block diagram

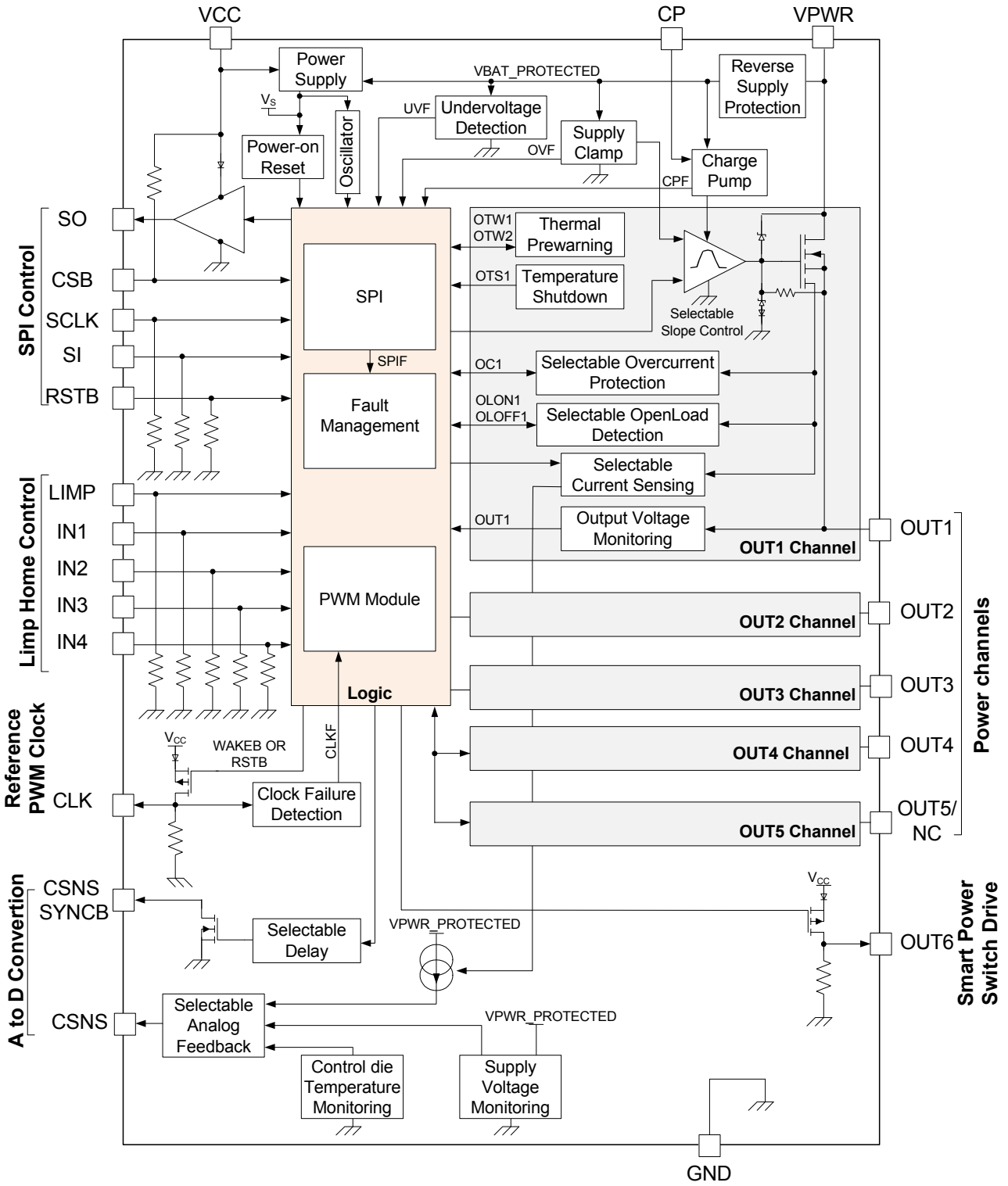


Figure 2. 12XSF simplified internal block diagram (penta version)

3 Pin connections

3.1 Pinout diagram

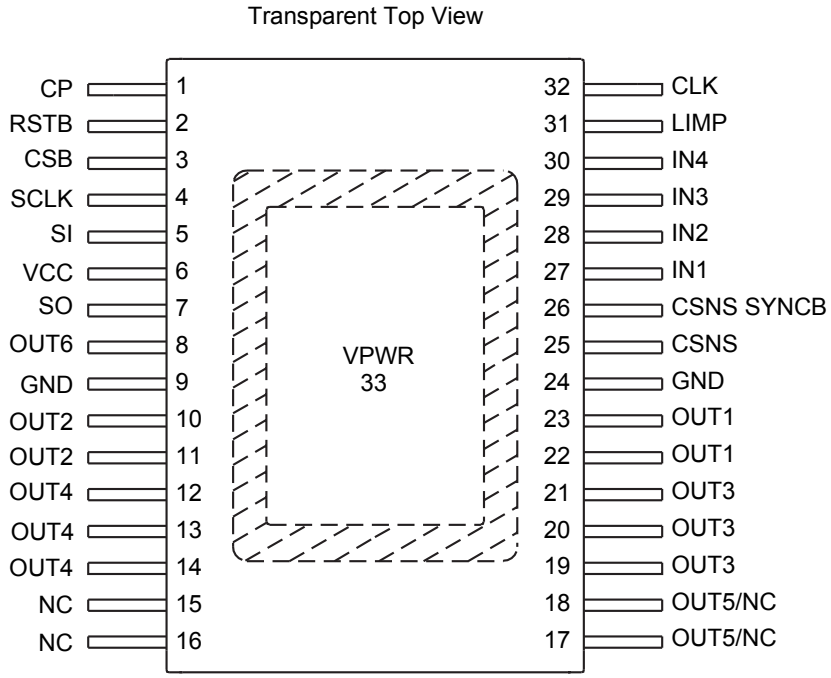


Figure 3. Pinout diagram for 32 pin SOIC-EP package

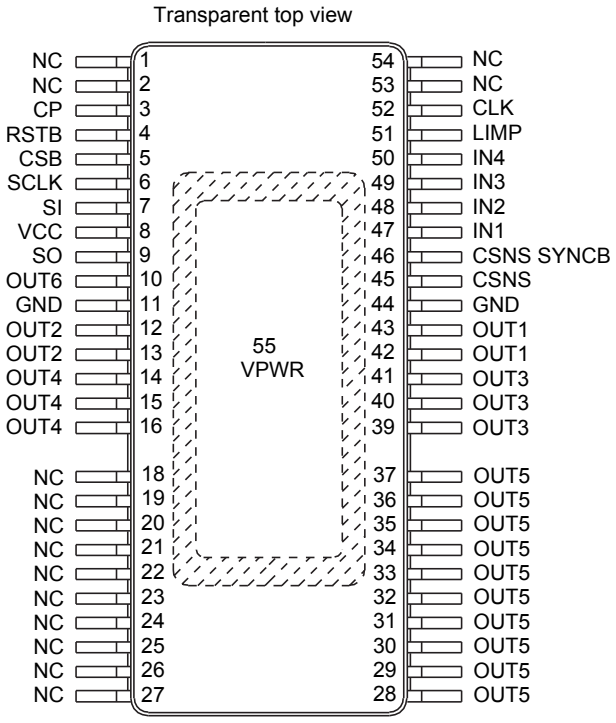


Figure 4. Pinout diagram for 54 pin SOIC-EP Package

3.2 Pin definitions

Table 2. 12XSF Pin definitions

Pin number 32 SOIC-EP	Pin number 54 SOIC-EP [(2)]	Pin name	Pin function	Formal name	Definition
1	3	CP	Internal supply	Charge-pump	This pin is the connection for an external capacitor for charge pump use only.
2	4	RSTB	SPI	Reset	This input pin is used to initialize the device configuration and fault registers, as well as place the device in a low-current Sleep mode. This pin has a passive internal pull-down.
3	5	CSB	SPI	Chip select	This input pin is connected to a chip select output of a master microcontroller (MCU). When this digital signal is high, SPI signals are ignored. Asserting this pin low starts an SPI transaction. The transaction is indicated as completed when this signal returns to high level. This pin has a passive internal pull-up to VCC through a diode
4	6	SCLK	SPI	Serial clock	This input pin is connected to the MCU providing the required bit shift clock for SPI communication. This pin has an passive internal pull-down.
5	7	SI	SPI	Serial input	This pin is the data input of the SPI communication interface. The data at the input are sampled on the positive edge of the SCLK. This pin has a passive internal pull-down.
6	8	VCC	Power supply	MCU power supply	This pin is a power supply pin for internal logic, the SPI I/Os and the OUT6 driver.
7	9	SO	SPI	Serial Output	This output pin is connected to the SPI Serial Data Input pin of the MCU or to the SI pin of the next device of a daisychain of devices. The SPI changes on the negative edge of SCLK. When CSB is high, this pin is high-impedance.
8	10	OUT6	Output	External Solid State	This output pin controls an external Smart Power Switch by logic level. This pin has a passive internal pull-down.
9 and 24	11 and 14	GND	Ground	Ground	These pins are the ground for the logic and analog circuitries of the device. For ESD and electrical parameter accuracy purpose, the ground pins must be shorted on the board.
10 to 11	12 to 13	OUT2	Output	Channel #2	Protected high-side power output pins to the load.
12 to 14	14 to 16	OUT4	Output	Channel #4	Protected high-side power output pins to the load.
15, 16	1, 2, 18 to 27, 53, 54	NC	N/A	Not connected	These pins are not connected. It is recommended to connect these pint to ground
17 to 18	28 to 37	OUT5	Output	Channel #5	Protected high-side power output pins to the load. This channel is not connected for the Quad version 17XS6400. It is recommended to connect those pins to ground for this device.
19 to 21	39 to 41	OUT3	Output	Channel #3	Protected high-side power output pins to the load.
22 to 23	42 to 43	OUT1	Output	Channel #1	Protected high-side power output pins to the load.
25	45	CSNS	Feedback	Current sense	This pin reports an analog value proportional to the designated OUT[1:5] output current or the temperature of the exposed pad or the supply voltage. It is used externally to generate a ground-referenced voltage for the microcontroller (MCU). Current recopy and analog voltage feedbacks are SPI programmable.
26	46	CSNS SYNCB	Feedback	Current sense synchronization	This open drain output pin allows synchronizing the MCU A/D conversion. This pin requires an external pull-up resistor to VCC.
27	47	IN1	Input	Direct input #1	This input wakes up the device. This input pin is used to directly control corresponding channel in Fail mode. During Normal mode the control of the outputs by the control inputs is SPI programmable.This pin has a passive internal pull-down.
28	48	IN2	Input	Direct input #2	This input wakes up the device. This input pin is used to directly control corresponding channel in Fail mode. During Normal mode the control of the outputs by the control inputs is SPI programmable.This pin has a passive internal pull-down.

Table 2. 12XSF Pin definitions (continued)

Pin number 32 SOIC-EP	Pin number 54 SOIC-EP (2)	Pin name	Pin function	Formal name	Definition
29	49	IN3	Input	Direct input #3	This input wakes up the device. This input pin is used to directly control corresponding channel in Fail mode. During Normal mode the control of the outputs by the control inputs is SPI programmable.This pin has a passive internal pull-down.
30	50	IN4	Input	Direct input #4	This input wakes up the device. This input pin is used to directly control corresponding channel in Fail mode. During Normal mode the control of the outputs by the control inputs is SPI programmable.This pin has a passive internal pull-down.
31	51	LIMP	Input	Limp Home	The Fail mode can be activated by this digital input. This pin has a passive internal pull-down.
32	52	CLK	Input/Output	Device mode feedback Reference PWM clock	This pin is an input/output pin. It is used to report the device sleep-state information. It is also used to apply reference PWM clock which is divided by 2^8 in Normal operating mode. This pin has a passive internal pull-down.
33	55	VPWR	Power supply	Power supply	This exposed pad connects to the positive power supply and is the source of operational power for the device.

Notes

2. Pins 17 and 38 are omitted.

4 General product characteristics

4.1 Relationship between ratings and operating requirements

The analog portion of device is supplied by the voltage applied to the VPWR exposed pad. Thereby the supply of internal circuitry (logic in case of a V_{CC} disconnect, charge pump, gate drive,...) is derived from the VPWR pin.

In case of a reverse supply:

- the internal supply rail is protected (max. -16 V)
- the output drivers (OUT1:OUT4/5) are switched on, to reduce the power consumption in the drivers when using incandescent bulbs

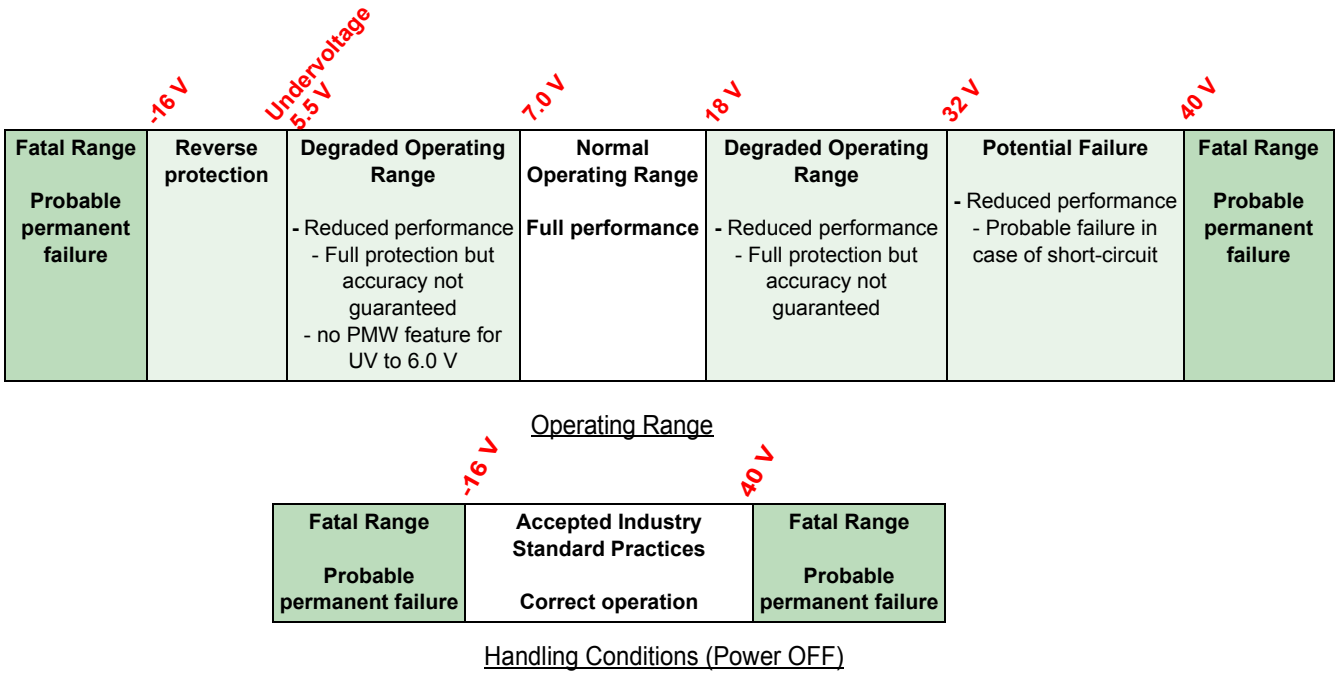


Figure 5. Ratings vs. operating requirements (VPWR pin)

The device's digital circuitry is powered by the voltage applied to the VCC pin. If VCC is disconnected, the logic part is supplied by the VPWR pin.

The output driver for SPI signals, CLK pin (wake feedback), and OUT6 are supplied by the VCC pin only. This pin shall be protected externally in case of a reverse polarity, and in case of a high-voltage disturbance.

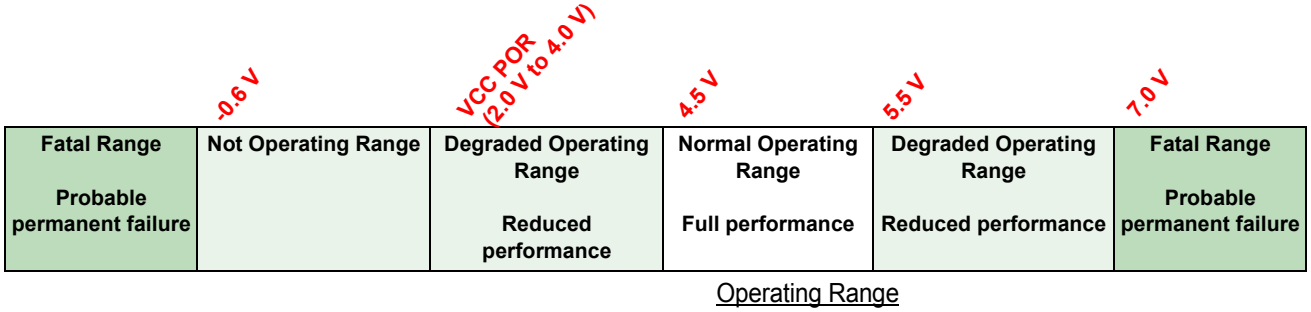


Figure 6. Ratings vs. operating requirements (VCC pin)

4.2 Maximum ratings

Table 3. Maximum ratings

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Description (rating)	Min.	Max.	Unit	Notes
Electrical ratings					
V_{PWR}	VPWR Voltage Range	-16	40	V	
V_{CC}	VCC Logic Supply Voltage	-0.3	7.0	V	
V_{IN}	Digital Input Voltage • IN1:IN4 and LIMP • CLK, SI, SCLK, CSB, and RSTB	 -0.3 -0.3	 40 20	V	(3)
V_{OUT}	Digital Output Voltage • SO, CSNS, SYNC, OUT6, CLK	-0.3	20	V	(3)
I_{CL}	Negative Digital Input Clamp Current	–	5.0	mA	(4)
I_{OUT}	Power Channel Current • 7.0 mΩ channel • 17 mΩ channel	 – –	 11 5.5	A	(5)
E_{CL}	Power Channel Clamp Energy Capability • 7.0 mΩ channel - Initial T_J = 25 °C • 7.0 mΩ channel - Initial T_J = 150 °C • 17 mΩ channel - Initial T_J = 25 °C • 17 mΩ channel - Initial T_J = 150 °C	 – – – –	 200 100 100 50	mJ	(6)
V_{ESD}	ESD Voltage • Human Body Model (HBM) - VPWR, Power Channel, and GND pins • Human Body Model (HBM) - All other pins • Charge Device Model (CDM) - Corner pins • Charge Device Model (CDM) - All other pins	 -8000 -2000 -750 -500	 +8000 +2000 +750 +500	V	(7)

Notes

3. Exceeding voltage limits on those pins may cause a malfunction or permanent damage to the device.
4. Maximum current in negative clamping for IN1:IN4, LIMP, RSTB, CLK, SI, SO, SCLK, and CSB pins.
5. Continuous high-side output current rating so long as maximum junction temperature is not exceeded. Calculation of maximum output current using package thermal resistance is required.
6. Active clamp energy using single-pulse method (L = 2.0 mH, R_L = 0 Ω, V_{PWR} = 14 V). Refer to Output clamps section.
7. ESD testing is performed in accordance with the Human Body Model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), and the Charge Device Model.

4.3 Thermal characteristics

Table 4. Thermal ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Description (rating)	Min.	Max.	Unit	Notes
Thermal ratings					
T_A T_J	Operating Temperature • Ambient • Junction	 -40 -40	 +125 +150	°C	(8)
T_{STG}	Storage Temperature	-55	+ 150	°C	
T_{PPRT}	Peak Package Reflow Temperature During Reflow	–	260	°C	(9) (10)
Thermal resistance and package dissipation ratings					
$R_{\Theta JB}$	Junction-to-Board	–	2.5	°C/W	(11)
$R_{\Theta JA}$	Junction-to-Ambient, Natural Convection, Four-Layer Board (2s2p) $R_{\Theta JA}$ - 54 SOIC-EP $R_{\Theta JA}$ - 32 SOIC-EP	 – –	 17.4 19.4	°C/W	(12) (13)
$R_{\Theta JC}$	Junction-to-Case (Case top surface)	–	10.6	°C/W	(14)

Notes

8. To achieve high reliability over 10 years of continuous operation, the device's continuous operating junction temperature should not exceed 125 °C.
9. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
10. NXP's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.NXP.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.
11. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
12. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
13. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
14. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

4.4 Operating conditions

This section describes the operating conditions of the device. Conditions apply to all the following data, unless otherwise noted.

Table 5. Operating conditions

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Min.	Max.	Unit	Notes
V_{PWR}	Functional operating supply voltage - Device is fully functional. All features are operating.	7.0	18	V	
	Overvoltage range • Jump Start • Load dump	 – –	 28 40	V	
	Reverse supply	-16	–	V	
V_{CC}	Functional operating supply voltage - Device is fully functional. All features are operating.	4.5	5.5	V	

4.5 Supply currents

This section describes the current consumption characteristics of the device.

Table 6. Supply currents

Characteristics noted under conditions 4.5 V ≤ V_{CC} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Ratings	Min.	Typ.	Max.	Unit	Notes
VPWR current consumptionS						
I_{QVPWR}	Sleep mode measured at V_{PWR} = 12 V • T_A = 25 °C • T_A = 125 °C	 – –	 1.2 10	 5.0 30	µA	(15) (16)
I_{VPWR}	Operating mode measured at V_{PWR} = 18 V	–	7.0	8.0	mA	(16)
VCC current consumptionS						
I_{QVCC}	Sleep mode measured at V_{CC} = 5.5 V	–	0.05	5.0	µA	
I_{VCC}	Operating mode measured at V_{PWR} = 5.5 V (SPI frequency 5.0 MHz)	–	2.8	4.0	mA	

Notes

15. With the OUT1:OUT4/5 power channels grounded.
16. With the OUT1:OUT4/5 power channels opened.

5 General IC functional description and application information

5.1 Introduction

The 12XSF is an evolution of the successful 12XSC by providing improved features of a complete family of devices using NXP's latest and unique technologies for the controller and the power stages.

The 12XSF consists of a scalable family of devices with different $R_{DS(on)}$ and different number of outputs, compatible in terms of software driver and package footprint. It allows diagnosing the light-emitting diodes (LEDs) with an enhanced current sense precision with synchronization pin as well as driving high power motors with a perfect control of its current consumption. It combines flexibility through daisy chainable SPI 5.0 MHz, extended digital and analog feedback, safety, and robustness. It integrates an enhanced PWM module with 8-bit duty cycle capability and PWM frequency prescaler per power channel.

5.2 Features

The main attributes of the 12XSF are:

- Quad or Penta high-side switches with overload, overtemperature, and undervoltage protection
- Control output for one external smart power switch
- 16-bit SPI communication interface with daisy chain capability
- Dedicated control inputs for use in Fail mode
- Analog feedback pin with SPI programmable multiplexer and sync signal
- Channel diagnosis by SPI communication
- Advanced current sense mode for LED usage
- Synchronous PWM module with external clock, prescaler and multiphase feature
- Excellent EMC behavior
- Power net and reverse polarity protection
- Ultra Low-power mode
- Scalable and flexible family concept
- Board layout compatible SOIC54 and SOIC32 package with exposed pad

5.3 Block diagram

The choice of multi-die technology in an SOIC exposed pad package, including a low cost vertical trench FET power die associated with Smart Power control die, lead to an optimized solution.

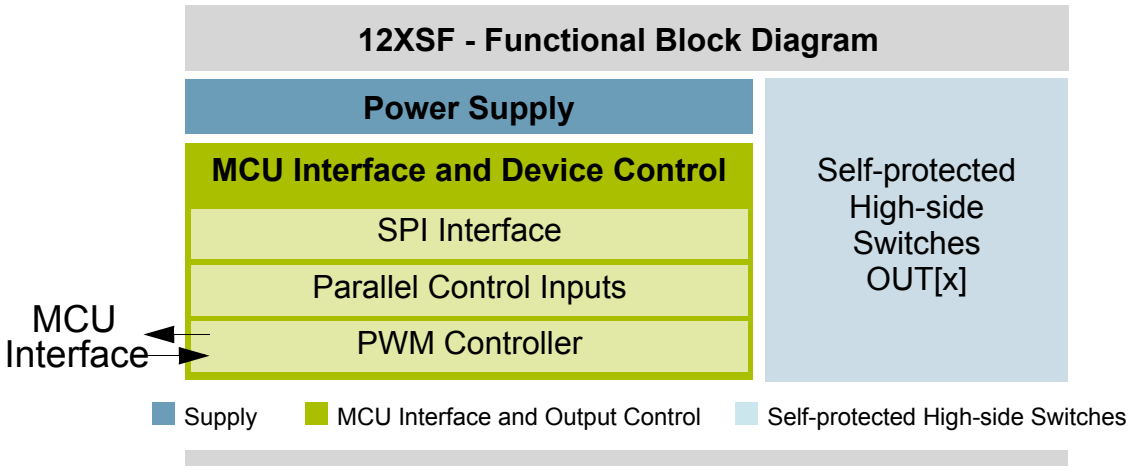


Figure 7. Functional block diagram

5.3.1 Self-protected high-side switches

OUT1: OUT4/5 are the output pins of the power switches. The power channels are protected against various kinds of short-circuits, and have active clamp circuitry which may be activated when switching off inductive loads. Many protective and diagnostic functions are available.

5.3.2 Power supply

The device operates with supply voltages from 5.5 V to 40 V (V_{PWR}), but is full spec. compliant only between 7.0 V and 18 V. The VPWR pin supplies power to the internal regulator, analog, and logic circuit blocks. The VCC pin (5.0 V typ.) supplies the output register of the serial peripheral interface (SPI). Consequently, the SPI registers cannot be read without presence of V_{CC}. The employed IC architecture guarantees a low quiescent current in Sleep mode.

5.3.3 MCU interface and device control

In Normal mode the power output channels are controlled by the embedded PWM module, which is configured by the SPI register settings. For bidirectional SPI communication, V_{CC} has to be in the authorized range. Failure diagnostics and configuration are also performed through the SPI port. The reported failure types are: open load, short-circuit to supply, severe short-circuit to ground, overcurrent, overtemperature, clock-fail, and under and overvoltage.

The device allows driving loads at different frequencies up to 400 Hz.

5.4 Functional description

The device has four fundamental operating modes: Sleep, Normal, Fail, and Power off. It possesses multiple high-side switches (power channels) each of which can be controlled independently:

- In Normal mode by SPI interface. A second supply voltage (V_{CC}) is required for bidirectional SPI communication
- In Fail mode by the corresponding direct inputs IN1:IN4. The OUT5 for the Penta version and the OUT6 are off in this mode

5.5 Modes of operation

The operating modes are based on the signals:

- wake = (IN1_ON) OR (IN2_ON) OR (IN3_ON) OR (IN4_ON) OR (RSTB). More details in the Logic I/O plausibility check section
- fail = (SPI_fail) OR (LIMP). More details in the Loss of communication interface section

The following chapters provide information for a five output device. (Do not consider OUT5 for the Quad version.)

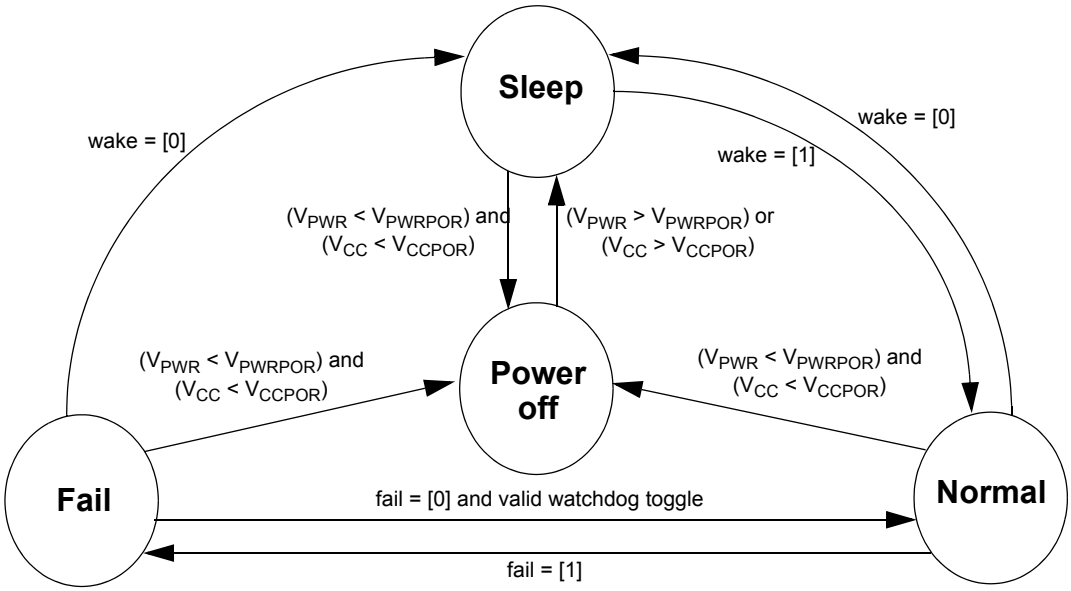


Figure 8. General IC operating modes

5.5.1 Power off mode

The power off mode is applied when V_{PWR} and V_{CC} are below the power on reset threshold ($V_{PWR\ POR}$, $V_{CC\ POR}$). No functionality is available, but the device is protected by the clamping circuits In power off. Refer to Supply voltages disconnection.

5.5.2 Sleep mode

The Sleep mode is used to provide ultra low-current consumption. During Sleep mode:

- the component is inactive and all outputs are disabled
- the outputs are protected by the clamping circuits
- the pull-up/pull-down resistors are present

Sleep mode is the default mode of the device after applying the supply voltages (V_{PWR} or V_{CC}) prior to any wake-up condition (wake = [0]). Wake-up from Sleep mode is provided by the wake signal.

5.5.3 Normal mode

The Normal mode is the regular operating mode of the device. The device is in Normal mode, when the device is in the wake state (wake = [1]) and no fail condition (fail = [0]) is detected.

During Normal mode:

- the power outputs are under control of the SPI
- the power outputs are controlled by the programmable PWM module
- the power outputs are protected by the overload protection circuit
- the control of the power outputs by SPI programming
- the digital diagnostic feature transfers status of the smart switch via the SPI
- the analog feedback output (CSNS and CSNS SYNC) can be controlled by the SPI

The channel control (CHx) can be summarized:

- CH1:4 controlled by ONx or iINx (if it is programmed by the SPI)
- CH5:6 controlled by ONx
- Rising CHx by definition means starting overcurrent window for OUT1:5

5.5.4 Fail mode

The device enters the Fail mode, when:

- the LIMP input pin is high (logic [1])
- or a SPI failure is detected

During Fail mode (wake = [1] & fail = [1]):

- the OUT1:OUT4 outputs are directly controlled by the corresponding control inputs (IN1:IN4)
- the OUT5:OUT6 are turned off
- the PWM module is not available
- while no SPI control is feasible, the SPI diagnosis is functional (depending on the Fail mode condition):
  - SO reports the content of SO register defined by SOA0 to 3 bits
- the outputs are fully protected in case of an overload, overtemperature, and undervoltage
- no analog feedback is available
- the max. output overcurrent profile is activated (OCLO and window times)
- in case of an overload condition or undervoltage, the autorestart feature controls the OUT1:OUT4 outputs
- in case of an overtemperature condition, OCHI1 detection, or severe short-circuit detection, the corresponding output is latched OFF until a new wake-up event

The channel control (CHx) can be summarized:

- CH1:4 controlled by iINx, while the overcurrent windows are controlled by IN_ONx
- CH5:6 are off

5.5.5 Mode transitions

After a wake-up:

- a power on reset is applied and all SPI SI and SO registers are cleared (logic[0])
- the faults are blanked during $t_{BLANKING}$

The device enters in Normal mode after start-up if following sequence is provided:

- V_{PWR} and V_{CC} power supplies must be above their undervoltage thresholds (Sleep mode)
- generate wake-up event (wake =1) setting RSTB from 0 to 1

The device initialization is completed after 50 µsec (typ). During this time, the device is robust in case of V_{PWR} interrupts higher than 150 nsec. The transition from “Normal mode” to “Fail mode” is executed immediately when a fail condition is detected. During the transition, the SPI SI settings are cleared and the SPI SO registers are not cleared.

When the Fail mode condition is a:

- LIMP input, WD toggle timeout, WD toggle sequence, or a SPI modulo 16 error, the SPI diagnosis is available during Fail mode
- SI/SO stuck to static level, the SPI diagnosis is not available during Fail mode

The transition from “Fail mode” to “Normal mode” is enabled when:

- the fail condition is removed and
- two SPI commands are sent within a valid watchdog cycle (first WD=[0] and then WD=[1])

During this transition:

- all SPI SI and SO registers are cleared (logic[0])
- the DSF (device status flag) in the registers #1:#7 and the RCF (Register Clearer flag) in the device status register #1 are set (logic[1])

To delatch the RCF diagnosis, a read command of the quick status register #1 must be performed.

5.6 SPI interface and configurations

5.6.1 Introduction

The SPI is used to:

- control the device in case of Normal mode
- provide diagnostics in case of Normal and Fail mode

The SPI is a 16-bit full-duplex synchronous data transfer interface with daisy chain capability.

The interface consists of four I/O lines with 5.0 V CMOS logic levels and termination resistors:

- The SCLK pin clocks the internal shift registers of the device
- The SI pin accepts data into the input shift register on the rising edge of the SCLK signal
- The SO pin changes its state on the rising edge of SCLK and reads out on the falling edge
- The CSB enables the SPI interface:
  - with the leading edge of CSB, the registers loads
  - while CSB is logic [0], SI/SO data shifts
  - with the trailing edge of the CSB signal, SPI data latches into the internal registers
  - when CSB is logic [1], the signals at the SCLK and SI pins are ignored and SO is high-impedance

When the RSTB input is:

- low (logic [0]), the SPI and the fault registers are reset. The Wake state then depends on the status of the input pins (IN_ON1:IN_ON4)
- high (logic[1]), the device is in Wake status and the SPI is enabled

The functionality of the SPI is checked by a plausibility check. During a SPI failure, the device enters Fail mode.

5.6.2 SPI input register and bit descriptions

The first nibble of the 16-bit data word (D15:D12) serves as address bits.

Register	SI address					SI data											
	#	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
name	8	4 Bit address				WD	11 Bit address										

11 bits (D10:D1) are used as data bits.

The D11 bit is the WD toggle bit. This bit has to be toggled with each write command.

When the toggling of the bit is not executed within the WD timeout, a SPI fail is detected.

All register values are logic [0] after a reset. The predefined value is off/inactive unless otherwise noted.

Register	SI address					SI data											
	#	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Initialisation 1	0	0	0	0	0	WD	WD SEL	SYNC EN1	SYNC EN0	MUX2	MUX1	MUX0	SOA MODE	SOA3	SOA2	SOA1	SOA0
initialisation 2	1	0	0	0	1	WD	OCHI THERMAL	OCHI TRANSIENT	NO HID1	NO HID0	X	OCHI OD4	OCHI OD3	OCHI OD2	OCHI OD1	PWM sync	OTW SEL
CH1 control	2	0	0	1	0	WD	PH11	PH01	ON1	PWM71	PWM61	PWM51	PWM41	PWM31	PWM21	PWM11	PWM01
CH2 control	3	0	0	1	1	WD	PH12	PH02	ON2	PWM72	PWM62	PWM52	PWM42	PWM32	PWM22	PWM12	PWM02
CH3 control	4	0	1	0	0	WD	PH13	PH03	ON3	PWM73	PWM63	PWM53	PWM43	PWM33	PWM23	PWM13	PWM03
CH4 control	5	0	1	0	1	WD	PH14	PH04	ON4	PWM74	PWM64	PWM54	PWM44	PWM34	PWM24	PWM14	PWM04
CH6 control	7	0	1	1	1	WD	PH16	PH06	ON6	PWM76	PWM66	PWM56	PWM46	PWM36	PWM26	PWM16	PWM06
output control	8	1	0	0	0	WD	X	PSF4	PSF3	PSF2	PSF1	ON6	X	ON4	ON3	ON2	ON1
Global PWM control	9-1	1	0	0	1	WD	0	X	X	X	X	GPWM EN6	X	GPWM EN4	GPWM EN3	GPWM EN2	GPWM EN1
	9-2	1	0	0	1	WD	1	X	X	GPWM7	GPWM6	GPWM5	GPWM4	GPWM3	GPWM2	GPWM1	GPWM0
over current control	10-1	1	0	1	0	WD	0	X	OCLO4	OCLO3	OCLO2	OCLO1	X	ACM EN4	ACM EN3	ACM EN2	ACM EN1
	10-2	1	0	1	0	WD	1	X	NO OCHI4	NO OCHI3	NO OCHI2	NO OCHI1	X	SHORT OCHI4	SHORT OCHI3	SHORT OCHI2	SHORT OCHI1
input enable	11	1	0	1	1	WD	0	X	X	INEN14	INEN04	INEN13	INEN03	INEN12	INEN02	INEN11	INEN01
prescaler settings	12-1	1	1	0	0	WD	0	X	X	PRS14	PRS04	PRS13	PRS03	PRS12	PRS02	PRS11	PRS01
	12-2	1	1	0	0	WD	1	X	X	X	X	X	X	X	X	PRS16	PRS06
OL control	13-1	1	1	0	1	WD	0	X	OLON DGL4	OLON DGL3	OLON DGL2	OLON DGL1	X	OLOFF EN4	OLOFF EN3	OLOFF EN2	OLOFF EN1
OLLED control	13-2	1	1	0	1	WD	1	res	res	res	res	OLLED TRIG	X	OLLED EN4	OLLED EN3	OLLED EN2	OLLED EN1
increment / dercrement	14	1	1	1	0	WD	INCR SGN	X	X	INCR14	INCR04	INCR13	INCR03	INCR12	INCR02	INCR11	INCR01
testmode	15	1	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X

WD	#0~#14	= watchdog toggle bit
SOA0 ~ SOA3	#0	= address of next SO data word
SOA MODE	#0	= single read address of next SO data word
MUX0 ~ MUX2	#0	= CSNS multiplexer setting
SYNC EN0~ SYNC EN1	#0	= SYNC delay setting
WD SEL	#0	= watchdog timeout select
OTW SEL	#1	= over temperature warning threshold selection
PWM SYNC	#1	= reset clock module
OCHI ODx	#1	= OCHI window on load demand
NO HIDx	#1	= HID outputs selection
OCHI THERMAL	#1	= OCHI1 level depending on control die temperature
OCHI TRANSIENT	#1	= OCHIx levels adjusted during OFF-to-ON transition
PWM0x ~ PWM7x	#2~#7	= PWM value (8Bit)
PH0x ~ PH1x	#2~#7	= phase control
ONx	#2~#8	= channel on/off incl. OCHI control
PSFx	#8	= pulse skipping feature for power output channels
GPWM ENx	#9-1	= global PWM enable
GPWM1 ~ GPWM7	#9-2	= global PWM value (8Bit)
ACM ENx	#10-1	= advanced current sense mode enable
OCLOx	#10-1	= OCLO level control
SHORT OCHIx	#10-2	= use short OCHI window time
NO OCHIx	#10-2	= start with OCLO threshold
INEN0x ~ INEN1x	#11	= input enable control
PRS0x ~ PRS1x	#12	= pre scaler setting
OLOFF ENx	#13-1	= OL load in off state enable
OLON DGLx	#13-1	= OL ON deglitch time
OLLED ENx	#13-2	= OL LED mode enable
OLLED TRIG	#13-2	= trigger for OLLED detetcion in 100% d.c.
INCR SGN	#14	= PWM increment / decrement sign
INCR0x ~ INCR1x	#14	= PWM increment / decrement setting

#1

NO HID1	NO HID0	HID Selection
0	0	available for all channels
0	1	available for channel 3 only
1	0	available for channels 3 and 4 only
1	1	unavailable for all channels

#0

MUX2	MUX1	MUX0	CSNS
0	0	0	off
0	0	1	OUT1 current
0	1	0	OUT2 current
0	1	1	OUT3 current
1	0	0	OUT4 current
1	0	1	unused
1	1	0	VPWR monitor
1	1	1	control die temp.monitor

#0

SYNC EN1	SYNC EN0	Sync status
0	0	sync off
0	1	valid
1	0	trig0
1	1	trig1/2

#2~#7

PH 1x	PH 0x	Phase
0	0	0°
0	1	90°
1	0	180°
1	1	270°

#11

ONx	INEN1x	INEN0x	GPWM ENx	INx=0 OUTx	INx=0 PWMx	INx=1 OUTx	INx=1 PWMx
0	x	x	x	OFF	x	OFF	x
1	0	0	0	ON	individual	ON	individual
			1	ON	global	ON	global
	0	1	0	OFF	individual	ON	individual
			1	OFF	global	ON	global
	1	0	0	OFF	individual	ON	individual
			1	OFF	global	ON	global
	1	1	0	ON	individual	ON	global
			1	ON	global	ON	individual

#12

PRS 1x	PRS 0x	PRS divider	
0	0	/4	25Hz 100Hz
0	1	/2	50Hz 200Hz
1	x	/1	100Hz 400Hz

#14

INCR SGN	increment/decrement
0	decrement
1	increment

#14

INCR 1x	INCR 0x	increment/decrement
0	0	no increment/decrement
0	1	4 LSB
1	0	8 LSB
1	1	16 LSB

5.6.3 SPI output register and bit descriptions

The first nibble of the 16-bit data word (D12:D15) serves as address bits. All register values are logic [0] after a reset, except DSF and RCF bits. The predefined value is off/inactive unless otherwise noted.

Register	SO address					SO data											
	#	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
not used	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X
quick status	1	0	0	0	1	FM	DSF	OVLF	OLF	CPF	RCF	CLKF	X	QSF4	QSF3	QSF2	QSF1
CH1 status	2	0	0	1	0	FM	DSF	OVLF	OLF	res	OTS1	OTW1	OC21	OC11	OC01	OLON1	OLOFF1
CH2 status	3	0	0	1	1	FM	DSF	OVLF	OLF	res	OTS2	OTW2	OC22	OC12	OC02	OLON2	OLOFF2
CH3 status	4	0	1	0	0	FM	DSF	OVLF	OLF	res	OTS3	OTW3	OC23	OC13	OC03	OLON3	OLOFF3
CH4 status	5	0	1	0	1	FM	DSF	OVLF	OLF	res	OTS4	OTW4	OC24	OC14	OC04	OLON4	OLOFF4
device status	7	0	1	1	1	FM	DSF	OVLF	OLF	res	res	res	TMF	OVF	UVF	SPIF	iLIMP
I/O status	8	1	0	0	0	FM	res	TOGGLE	iIN4	iIN3	iIN2	iIN1	X	OUT4	OUT3	OUT2	OUT1
device ID	9	1	0	0	1	FM	res	res	res	DEVID 7	DEVID 6	DEVID 5	DEVID 4	DEVID 3	DEVID 2	DEVID 1	DEVID 0
not used	10-14	adress from 1010 to 1110				X	X	X	X	X	X	X	X	X	X	X	X
testmode	15	1	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X

QSFx	*#1*	*= quick status (OC or OTW or OTS or OLON or OLOFF)*
CLKF	*#1*	*= PWM clock fail flag*
RCF	*#1*	*= registers clear flag*
CPF	*#1*	*= charge pump flag*
OLF	*#1~#7*	*= open load flag (wired or of all OL signals)*
OVLF	*#1~#7*	*= over load flag (wired or of all OC and OTS signals)*
DSF	*#1~#7*	*= device status flag (RCF or UVF or OVF or CPF or CLKF or TMF)*
FM	*#1~#8*	*= fail mode flag*
OLOFFx	*#2~#6*	*= open load in off state status bit*
OLONx	*#2~#6*	*= open load in on state status bit*
OTWx	*#2~#6*	*= over temperature warning bit*
OTSx	*#2~#6*	*= over temperature shutdown bit*
iLIMP	*#7*	*= limp input pin status*
SPIF	*#7*	*= SPI fail flag*
UVF	*#7*	*= under voltage flag*
OVF	*#7*	*= over voltage flag*
TMF	*#7*	*= testmode activation flag*
OUTx	*#8*	*= status of VPWR/2 comparator (reported in real time)*
iINx	*#8*	*= status of iINx signal (reported in real time)*
TOGGLE	*#8*	*= status of INx_ON signals (IN1_ON or IN2_ON or IN3_ON or IN4_ON)*
DEVID0 ~ DEVID2	*#9*	*= device type*
DEVID3 ~ DEVID4	*#9*	*= device family*
DEVID5 ~ DEVID7	*#9*	*= design status (incremented number)*

	OC2x	OC1x	OC0x	over current status
#2~#6	0	0	0	no overcurrent
	0	0	1	OCHI1
	0	1	0	OCHI2
	0	1	1	OCHI3
	1	0	0	OCLO
	1	0	1	OCHIOD
	1	1	0	SSC
	1	1	1	not used

	DEVID2	DEVID1	DEVID0	device type
#9	0	0	0	Penta3/2
	0	0	1	Penta0/5
	0	1	0	Quad2/2
	0	1	1	Quad0/4
	1	0	0	Triple1/2
	1	0	1	Triple0/3
	1	1	0	res
	1	1	1	res

5.6.4 Timing diagrams

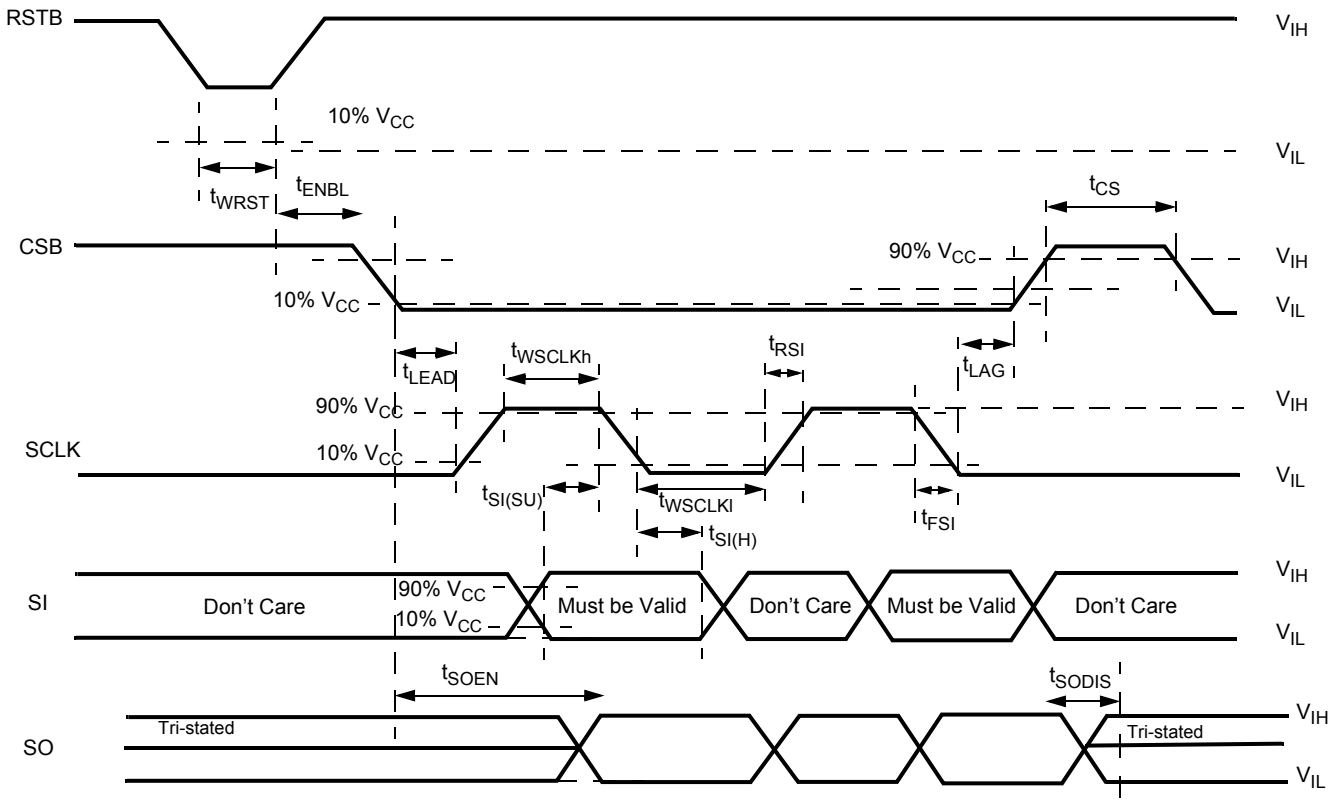


Figure 9. Timing requirements during SPI communication

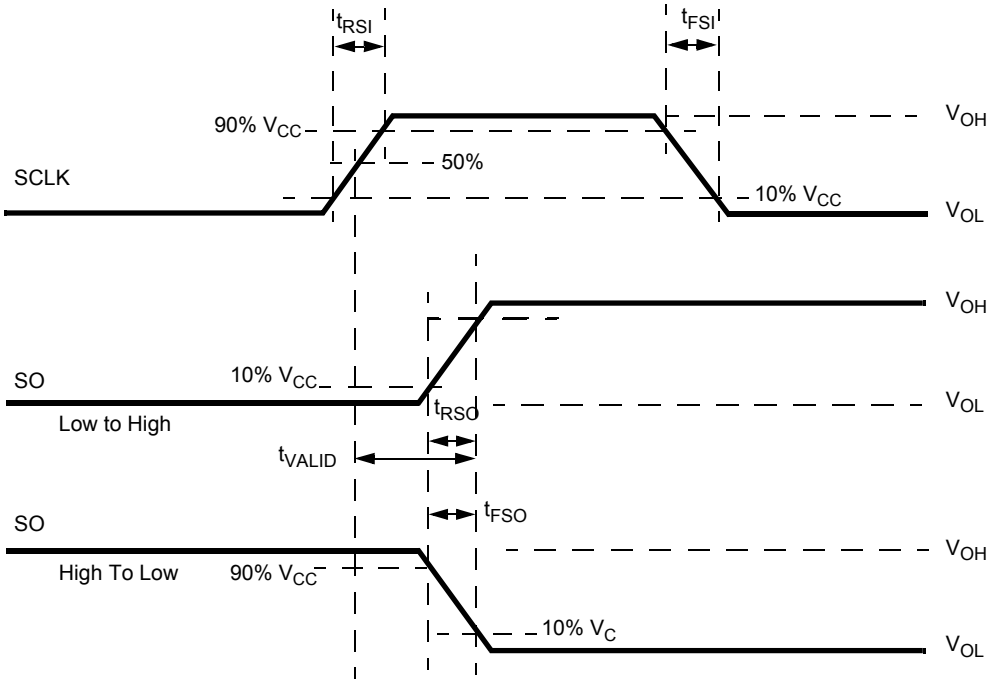


Figure 10. Timing diagram for serial output (SO) data communication

5.6.5 Electrical characterization

Table 7. Electrical characteristics

Characteristics noted under conditions 4.5 V ≤ V_{CC} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
SPI signals CSB, SI, SO, SCLK, SO						
f_{SPI}	SPI Clock Frequency	0.5	–	5.0	MHz	
V_{IH}	Logic Input High State Level (SI, SCLK, CSB, RSTB)	3.5	–	–	V	
$V_{IH(WAKE)}$	Logic Input High State Level for wake-up (RSTB)	3.75	–	–	V	
V_{IL}	Logic Input Low State Level (SI, SCLK, CSB, RSTB)	–	–	0.85	V	
V_{OH}	Logic Output High State Level (SO)	VCC - 0.4	–	–	V	
V_{OL}	Logic Output Low State Level (SO)	–	–	0.4	V	
I_{IN}	Logic Input Leakage Current in Inactive State (SI = SCLK = RSTB = [0] and CSB = [1])	-0.5	–	+0.5	µA	
I_{OUT}	Logic Output Tri-state Leakage Current (SO from 0 V to V_{CC})	-10	–	+1.0	µA	
R_{PULL}	Logic Input Pull-up/Pull-down Resistor	25	–	100	kΩ	
C_{IN}	Logic Input Capacitance	–	–	20	pF	(17)
t_{RST_DGL}	RSTB Deglitch Time	7.5	10	12.5	µs	
t_{SO}	SO Rising and Falling Edges with 80 pF	–	–	20	ns	
t_{WCLKh}	Required High State Duration of SCLK (Required Setup Time)	80	–	–	ns	
t_{WCLKl}	Required Low State Duration of SCLK (Required Setup Time)	80	–	–	ns	
t_{CS}	Required Duration from the Rising to the Falling Edge of CSB (Required Setup Time)	1.0	–	–	µs	
t_{RST}	Required Low State Duration for reset RST\	1.0	–	–	µs	
t_{LEAD}	Falling Edge of CSB to Rising Edge of SCLK (Required Setup Time)	320	–	–	ns	
t_{LAG}	Falling Edge of SCLK to Rising Edge of CSB (Required Setup Lag Time)	100	–	–	ns	
$t_{SI(SU)}$	SI to Falling Edge of SCLK (Required Setup Time)	20	–	–	ns	
$t_{SI(H)}$	Falling Edge of SCLK to SI (Required hold Time of the SI Signal)	20	–	–	ns	
t_{RSI}	SI, CSB, SCLK, Max. Rise Time Allowing Operation at Maximum f_{SPI}	–	20	50	ns	
t_{FSI}	SI, CSB, SCLK, Max. Fall Time Allowing Operation at Maximum f_{SPI}	–	20	50	ns	
$t_{SO(EN)}$	Time from Falling Edge of CSB to Reach Low-impedance on SO (access time)	–	–	60	ns	
$t_{SO(DIS)}$	Time from Rising Edge of CSB to Reach Tri-state on SO	–	–	60	ns	

Notes

17. Parameter is derived from simulations.

6 Functional block requirements and behaviors

6.1 Self-protected high-side switches description and application information

6.1.1 Features

Up to five power outputs are foreseen to drive light as well as DC motor applications. The outputs are optimized for driving bulbs, HID ballasts, LEDs, and other resistive or low inductive loads. The smart switches are controlled by use of high sophisticated gate drivers. The gate drivers provide:

- output pulse shaping
- output protections
- active clamps
- output diagnostics

6.1.2 Output pulse shaping

The outputs are controlled with a closed loop active pulse shaping to provide the best compromise between:

- low switching losses
- low EMC emission performance
- minimum propagation delay time

Depending on the programming of the prescaler setting register #12-1, #12-2, the switching speeds of the outputs are adjusted to the output frequency range of each channel. The edge shaping shall be designed according the following table:

Divider factor	PWM freq. (Hz)		PWM period (ms)		d.c. range (hex)		D.C. range (LSB)		min. on/off duty cycle time (µs)
	min.	max.	min.	max.	min.	max.	min.	max	
4	25	100	10	40	03	FB	4	252	156
2	50	200	5	20	07	F7	8	248	156
1	100	400	2.5	10	07	F7	8	248	78

The edge shaping provides full symmetry for rising and falling transition:

- the slopes for the rising and falling edge are matched to provide the best EMC emission performance
- the shaping of the upper edges and the lower edges are matched to provide the best EMC emission performance
- the propagation delay time for the rising edge and the falling edge is matched to provide true duty cycle control of the output duty cycle error, ≤ 1 LSB at max. frequency
- a digital regulation loop is used to minimize the duty cycle error of the output signal

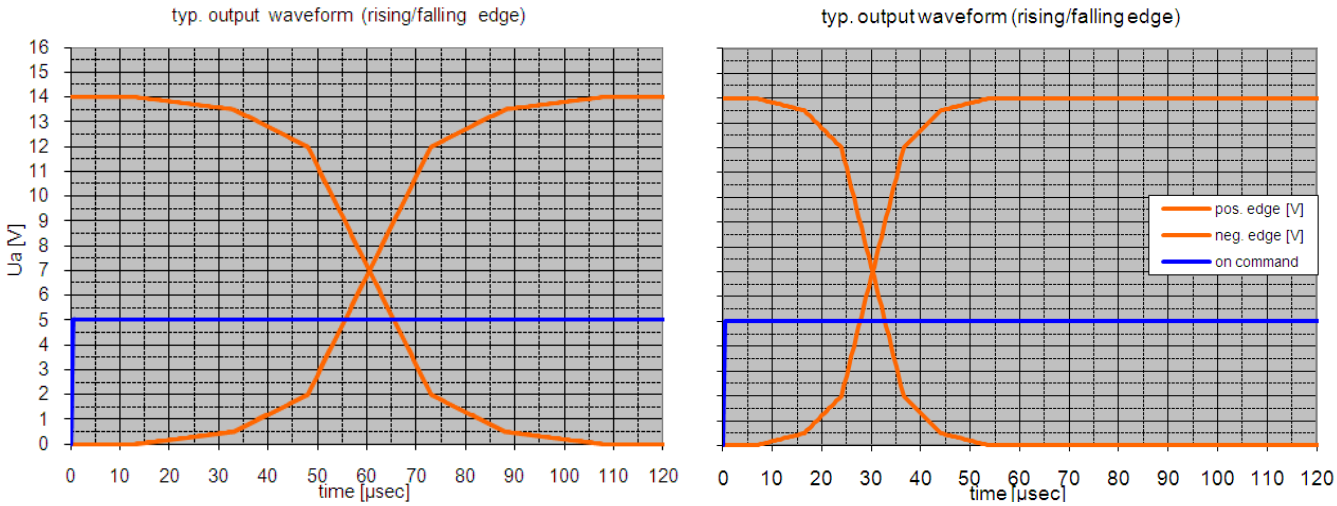


Figure 11. Typical power output switching (slow and fast slew rate)

6.1.2.1 SPI control and configuration

For optimized control of the outputs, a synchronous clock module is integrated. The PWM frequency and output timing during Normal mode are generated from the clock input (CLK) by the integrated PWM module. In case of clock fail (very low frequency, very high frequency), the output duty cycle is 100%.

Each output (OUT1:OUT6) can be controlled by an individual channel control register:

Register	SI address					SI data											
	#	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CHx control	2-7	channel address				WD	PH1x	PH0x	Onx	PWM7x	PWM6x	PWM5x	PWM4x	PWM3x	PWM2x	PWM1x	PWM0x

Where:

- PH0x:PH1x: phase assignment of the output channel x
- ONx: on/off control including overcurrent window control of the output channel x
- PWM0x:PWM7x: 8-bit PWM value individually for each output channel x

The ONx bits are duplicated in the output control register #8 to control the outputs with either the CHx control register or the output control register. The PRS1x:PRS0x prescaler settings can be set in the prescaler settings register #12-1 and #12-2. The following changes of the duty cycle are performed asynchronous (with positive edge of CSB signal):

- turn on with 100% duty cycle (CHx = ON)
- change of duty cycle value to 100%
- turn off (CHx = OFF)
- phase setting (PH0x:PH1x)
- prescaler setting (PRS1x:PRS0x)

A change in phase setting or prescaler setting during CHx = ON may cause an unwanted long ON-time. Therefore it is recommended to turn off the output(s) before execution of this change. The following changes of the duty cycle are performed synchronous (with the next PWM cycle):

- turn on with less than 100% duty cycle (OUTx = ONx)
- change of duty cycle value to less than 100%

A change of the duty cycle value can be achieved by a change of the:

- PWM0x: PWM7x bits in individual channel control register #2:#7
- GPWM EN1: GPWM EN6 bits (change between individual PWM and global PWM settings) in global PWM control register #9-1
- incremental/decremental register #14

The synchronization of the switching phases between different devices is provided by the PWM SYNC bit in the initialization 2 register #1.

On a SPI write into initialization 2 register (#1):

- initialization when the bit D1 (PWM SYNC) is logic[1], all counters of the PWM module are reset with the positive edge of the CSB, i.e. the phase synchronization is performed immediately within one SPI frame. It could help to synchronize different 12XSF devices in the board
- when the bit D1 is logic[0], no action is executed

The switching frequency can be adjusted for the corresponding channel as described in the following table:

CLK freq. (kHz)		prescaler setting		divider factor	PWM freq. (Hz)		slew rate	PWM resolution)	
min.	max.	PRS1x	PRS0x		min.	max.		(Bit)	(steps)
25.6	102.4	0	0	4	25	100	slow	8	256
		0	1	2	50	200	slow		
		1	X	1	100	400	fast		

No PWM feature is provided in case of:

- Fail mode
- clock input signal failure

6.1.2.2 Global PWM control

In addition to the individual PWM register, each channel can be assigned independently to a global PWM register. The setting is controlled by the GPWM EN bits inside the global PWM control register #9-1. When no control by direct input pin is enabled and the GPWM EN bit is:

- low (logic[0]), the output is assigned to individual PWM (default status)
- high (logic[1]), the output is assigned to global PWM

The PWM value of the global PWM channel is controlled by the global PWM control register #9-2.

Table 8. Global PWM register

ONx	INEN1x	INEN0x	GPWM ENx	INx = 0		INx = 1	
				CHx	PWMx	CHx	PWMx
0	x	x	x	OFF	x	OFF	x
1	0	0	0	ON	individual	ON	individual
			1	ON	global	ON	global
	0	1	0	OFF	individual	ON	individual
	1	0	1	OFF	global	ON	global
	1	1	0	ON	individual	ON	global
			1	ON	global	ON	individual

When a channel is assigned to global PWM, the switching phase the prescaler and the pulse skipping are according the corresponding output channel setting.

6.1.2.3 Incremental PWM control

To reduce the control overhead during soft start/stop of bulbs or DC motors (e.g. theatre dimming), an incremental PWM control feature is implemented. With the incremental PWM control feature the PWM values of all internal channels OUT1:OUT4/5 can be incremented or decremented with one SPI frame.

The incremental PWM feature is not available for:

- the global PWM channel
- the external channel OUT6

The control is according the increment/decrement register #14:

- INCR SGN: sign of incremental dimming (valid for all channels)
- INCR 1x, INCR 0x increment/decrement

INCR SGN	increment/decrement
0	decrement
1	increment

INCR 1x	INCR 0x	increment/decrement
0	0	no increment/decrement
0	1	4
1	0	8
1	1	16

This feature limits the duty cycle to the rails (00 resp. FF) to avoid any overflow.

6.1.2.4 Pulse skipping

Due to the output pulse shaping feature and the resulting switching delay time of the smart switches, duty cycles close to 0% resp. 100% can not be generated by the device. Therefore the pulse skipping feature (PSF) is integrated to interpolate this output duty cycle range in Normal mode.

The pulse skipping provides a fixed duty cycle pattern with eight states to interpolate the duty cycle values between F7 (Hex) and FF (Hex). The range between 00 (Hex) and 07 (Hex) is not considered to be provided.

The pulse skipping feature:

- is available individually for the power output channels (OUT1:OUT5)
- is not available for the external channel (OUT6)

The feature is enabled with the PSF bits in the output control register #8. When the corresponding PSF bit is:

- low (logic[0]), the pulse skipping feature is disabled on this channel (default status)
- high (logic[1]), the pulse skipping feature is enabled on this channel

PWM duty cycle			pulse skipping frame							
hex	dec	[%]	S0	S1	S2	S3	S4	S5	S6	S7
FF	256	100,00%	FF	FF	FF	FF	FF	FF	FF	FF
FE	255	99,61%	F7	FF	FF	FF	FF	FF	FF	FF
FD	254	99,22%	F7	FF	FF	FF	F7	FF	FF	FF
FC	253	98,83%	F7	FF	F7	FF	F7	FF	FF	FF
FB	252	98,44%	F7	FF	F7	FF	F7	FF	F7	FF
FA	251	98,05%	F7	F7	F7	FF	F7	FF	F7	FF
F9	250	97,66%	F7	F7	F7	FF	F7	F7	F7	FF
F8	249	97,27%	F7	F7	F7	F7	F7	F7	F7	FF
F7	248	96,88%								
F6	247	96,48%								
F5	246	96,09%								
F4	245	95,70%								
.	.	.								
.	.	.								
.	.	.								
.	.	.								
03	4	1,56%								
02	3	1,17%								
01	2	0,78%								
00	1	0,39%								

6.1.2.5 Input control

Up to four dedicated control inputs (IN1:IN4) are foreseen to:

- wake-up the device
- fully control the corresponding output in case of Fail mode
- control the corresponding output in case of Normal mode

The control during Normal mode is according the INEN0x and INEN1x bits in the input enable register #11 and according the logic table in Table 8. An input deglitcher is provided at each control input to avoid high frequency control of the outputs. The internal signal is called iINx. The channel control (CHx) can be summarized:

- Normal mode:
  - CH1: 4 controlled by ONx or INx (if it is programmed by the SPI)
  - CH5: 6 controlled by ONx
  - Rising CHx by definition means starting overcurrent window for OUT1:5
- Fail mode:
  - CH1: 4 controlled by iINx, while the overcurrent windows are controlled by IN_ONx
  - CH5: 6 are off

Even so, the input thresholds are logic level compatible, the input structure of the pins is able to withstand supply voltage levels (max.40 V) without damage. External current limit resistors (i.e. 1.0 kΩ:10 kΩ) can be used to handle reverse current conditions. The inputs have an integrated pull-down resistor.

6.1.2.6 Electrical characterization

Table 9. Electrical characteristics

Characteristics noted under conditions 7.0 V ≤ V_{PWR} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Power outputs OUT1:OUT5						
$R_{DS(on)}$	ON-Resistance, Drain-to-Source for 7.0 mΩ Power Channel • T_J = 25 °C, V_{PWR} ≥ -12 V • T_J = 150 °C, V_{PWR} ≥ -12 V • T_J = 25 °C, V_{PWR} = 7.0 V • T_J = 25 °C, V_{PWR} = -12 V • T_J = 150 °C, V_{PWR} = -12 V	 – – – – –	 7.0 – – – –	 8.0 12.9 10.5 13 18.2	mΩ	
$R_{DS(on)}$	ON-Resistance, Drain-to-Source for 17 mΩ Power Channel • T_J = 25 °C, V_{PWR} ≥ -12 V • T_J = 150 °C, V_{PWR} ≥ -12 V • T_J = 25 °C, V_{PWR} = 7.0 V • T_J = 25 °C, V_{PWR} = -12 V • T_J = 150 °C, V_{PWR} = -12 V	 – – – – –	 17 – – – –	 19 30.9 25.5 31 43.5	mΩ	
$I_{LEAK\ SLEEP}$	Sleep Mode Output Leakage Current (Output shorted to GND) per Channel • T_J = 25 °C, V_{PWR} = 12 V • T_J = 125 °C, V_{PWR} = 12 V • T_J = 25 °C, V_{PWR} = 35 V • T_J = 125 °C, V_{PWR} = 35 V	 – – – –	 – – – –	 0.5 5.0 5.0 25	µA	
$I_{OUT\ OFF}$	Operational Output Leakage Current in OFF-State per Channel • T_J = 25 °C, V_{PWR} = 18 V • T_J = 125 °C, V_{PWR} = 18 V	 – –	 – –	 10 20	µA	
δ_{PWM}	Output PWM Duty Cycle Range (measured at V_{OUT} = $V_{PWR/2}$) • Low Frequency Range (25 to 100 Hz) • Medium Frequency Range (50 to 200 Hz) • High Frequency Range (100 to 400 Hz)	 4.0 8.0 8.0	 – – –	 252 248 248	LSB	

Table 9. Electrical characteristics (continued)

Characteristics noted under conditions 7.0 V ≤ V_{PWR} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
SR	Rising and Falling Edges Slew-Rate at V_{PWR}= 14 V (measured from V_{OUT} = 2.5 V to V_{PWR} - 2.5 V) • Low Frequency Range • Medium Frequency Range • High Frequency Range	 0.25 0.25 0.55	 0.42 0.42 0.84	 0.6 0.6 1.25	V/µs	(18)
ΔSR	Rising and Falling Edges Slew Rate Matching at V_{PWR} = 14 V (SRr/ SRf)	0.9	1.0	1.1		(18)
t_{DLY}	Turn-on and Turn-off Delay Times at V_{PWR} = 14 V • Low Frequency Range • Medium Frequency Range • High Frequency Range	 20 20 10	 70 70 30	 120 120 50	µs	(18)
Δt_{DLY}	Turn-on and Turn-off Delay Times Matching at V_{PWR}= 14 V • Low Frequency Range • Medium Frequency Range • High Frequency Range	 -20 -20 -10	 0.0 0.0 0.0	 20 20 10	µs	(18)
$t_{OUTPUT\ SD}$	Shutdown Delay Time in case of Fault	0.5	2.5	4.5	µs	
Reference PWM clock						
f_{CLK}	Clock Input Frequency Range	25.6	–	102.4	kHz	

Notes

18. With nominal resistive load: 2.5 Ω and 5.0 Ω respectively for 7.0 mΩ and 17 mΩ channel.

6.1.3 Output protections

The power outputs are protected against fault conditions in Normal and Fail mode in case of:

- overload conditions
- harness short-circuit
- overcurrent protection against ultra-low resistive short-circuit conditions due to a smart overcurrent profile and severe short-circuit protection
- overtemperature protection including overtemperature warning
- under and overvoltage protections
- charge pump monitoring
- reverse polarity protection

In case a fault condition is detected, the corresponding output is commanded off immediately after the deglitch time $t_{FAULT\ SD}$. The turn off in case of a fault shutdown (OCHI1, OCHI2, OCHI3, OCLO, OTS, UV, CPF, OLOFF) is provided by the FTO feature (fast turn off). The FTO:

- does not use edge shaping
- is provided with high slew rate to minimize the output turn-off time $t_{OUTPUT\ SD}$, in regards to the detected fault
- uses a latch which keeps the FTO active during an undervoltage condition (0 ≤ V_{PWR} ≤ $V_{PWR\ UVF}$)

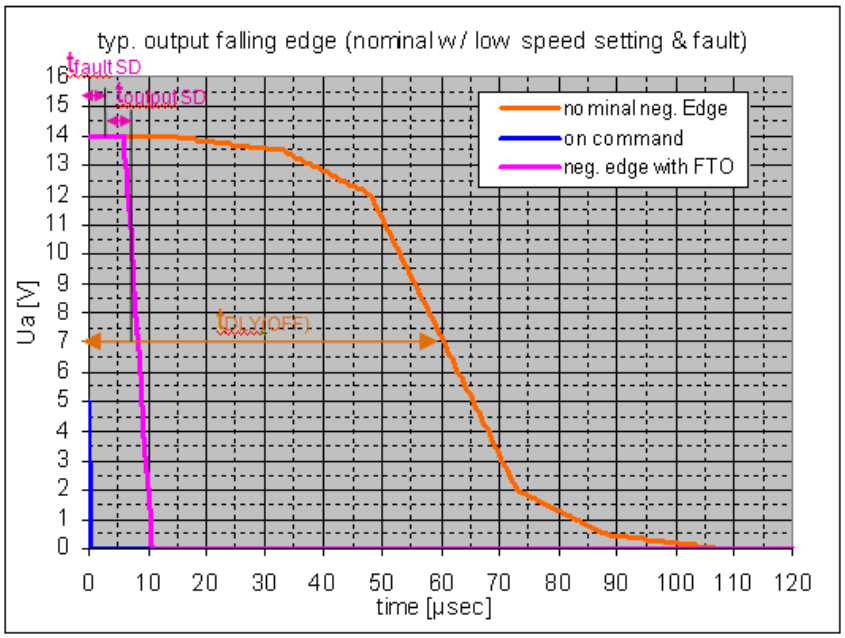


Figure 12. Power output switching in nominal operation and in case of fault

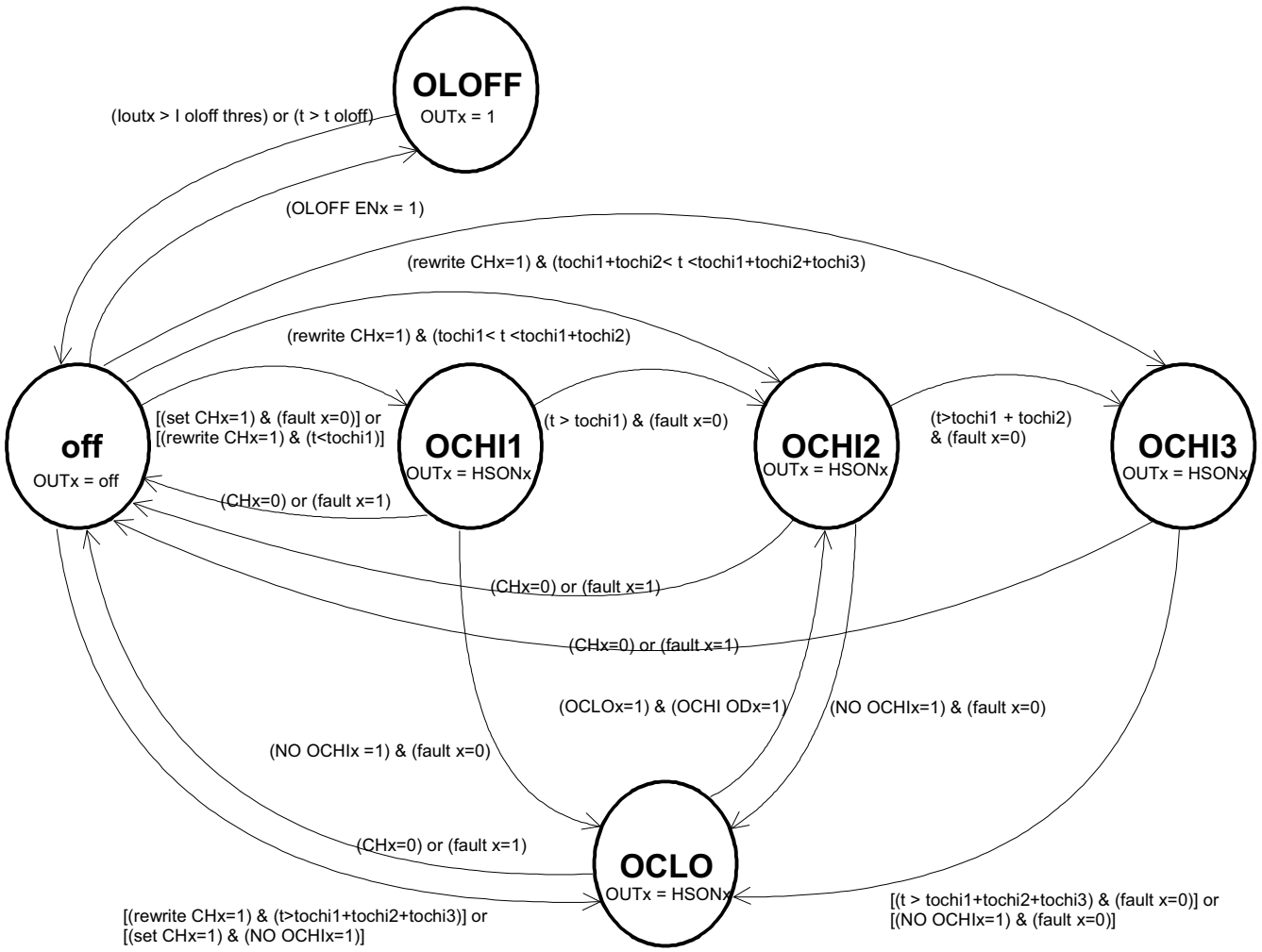
Normal mode

In case of a fault condition during Normal mode:

- the status is reported in the quick status register #1 and the corresponding channel status register #2:#6

To restart the output:

- the channel must be restarted by writing the corresponding ON bit in the channel control register #2:#6 or output control register #8



Definitions of key logic signals

(fault x):= (UV) or (OCHI1x) or (OCHI2x) or (OCHI3x) or (OCLOx) or (OTx) or (SSCx)
(set CHx=1):= [(ONx=0) then (ONx=1)] or [(iINx=0) then (iINx=1)]
(rewrite CHx=1):= (rewrite ONx=1) after (fault x=1)
SSCx:= severe short circuit detection

tochi2 is depending on NO_HID settings and output current during OCHI2 state

Figure 13. Output control diagram in normal mode

Fail mode

In an overcurrent (OCHI2, OCHI3, OCLO) or undervoltage is detected, the restart is controlled by the autorestart feature.

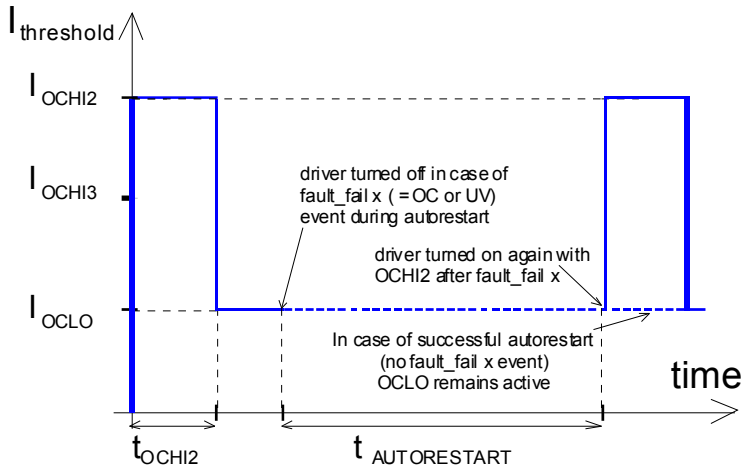


Figure 14. Autorestart in fail mode

During overtemperature (OTSx), severe short-circuit (SSCx), or OCHI1 overcurrent, the corresponding output enters the latch off state until the next wake-up cycle or mode change.

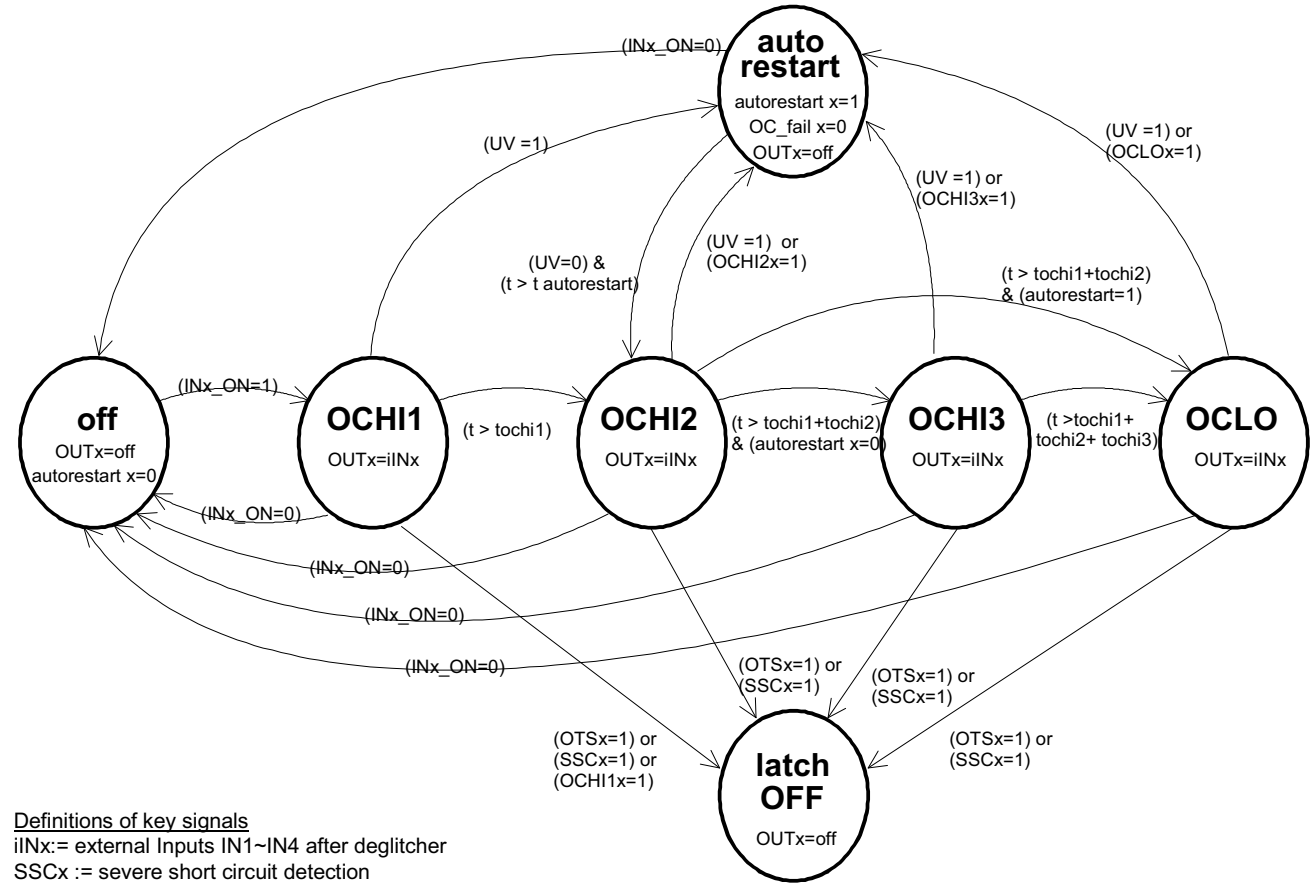


Figure 15. Output control diagram in fail mode

6.1.3.1 Overcurrent protections

Each output channel is protected against overload conditions by use of a multilevel overcurrent shutdown.

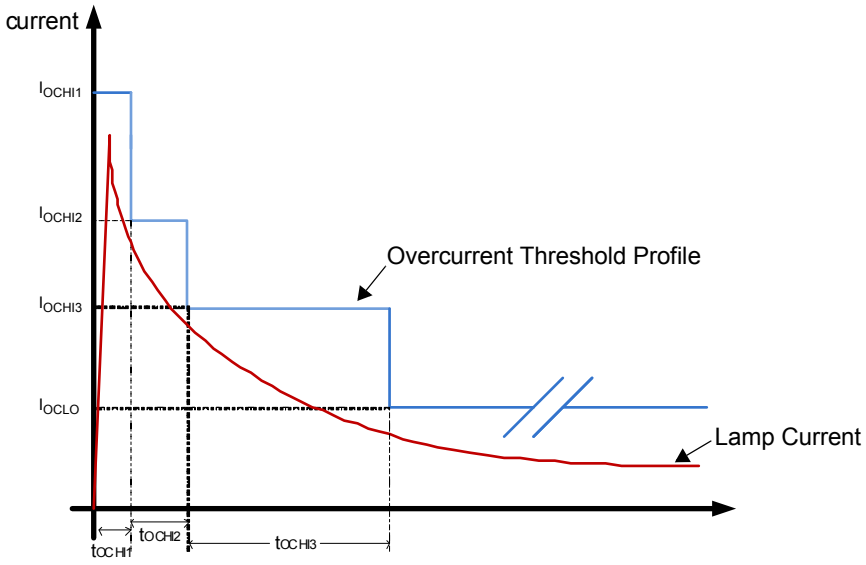


Figure 16. Transient overcurrent profile

The current thresholds and the threshold window times are fixed for each type of power channel. When the output is in PWM mode, the clock for the OCHI time counters (t_{OCHI1}:t_{OCHI3}) is gated (logic AND) with the referring output control signal:

- the clock for the t_{OCHI} counter is activated when the output = [1] respectively CHx = 1
- the clock for the t_{OCHI} counter is stopped when the output = [0] respectively CHx = 0

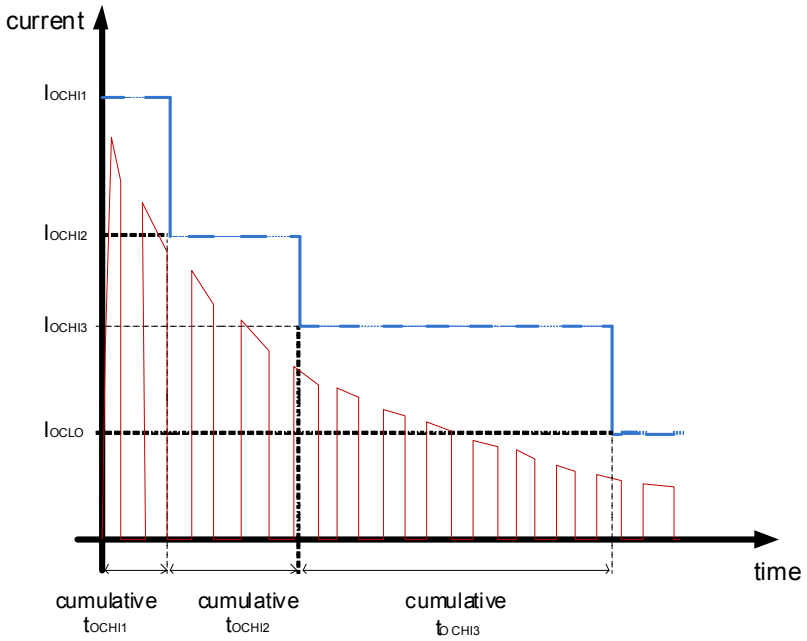


Figure 17. Transient overcurrent profile in PWM mode

This strategy counts the OCHI time only when the bulb is actually heated up. The window counting is stopped in case of UV, CPF and OTS. A severe short-circuit protection (SSC) is implemented to limit the power dissipation in Normal and Fail modes, in case of severe short-circuit event. This feature is active only for a very short period of time, during OFF-to-ON transition. The load impedance is monitored during the output turn-on.

Normal mode

The enabling of the high current window (OCHI1:OCHI3) is dependent on CHx signal. When no control input pin is enabled, the control of the overcurrent window depends on the ON bits inside channel control registers #2:#7 or the output control register #8. When the corresponding CHx signal is:

- toggled (turn OFF and then ON), the OCHI window counter resets and the full OCHI windows is applied

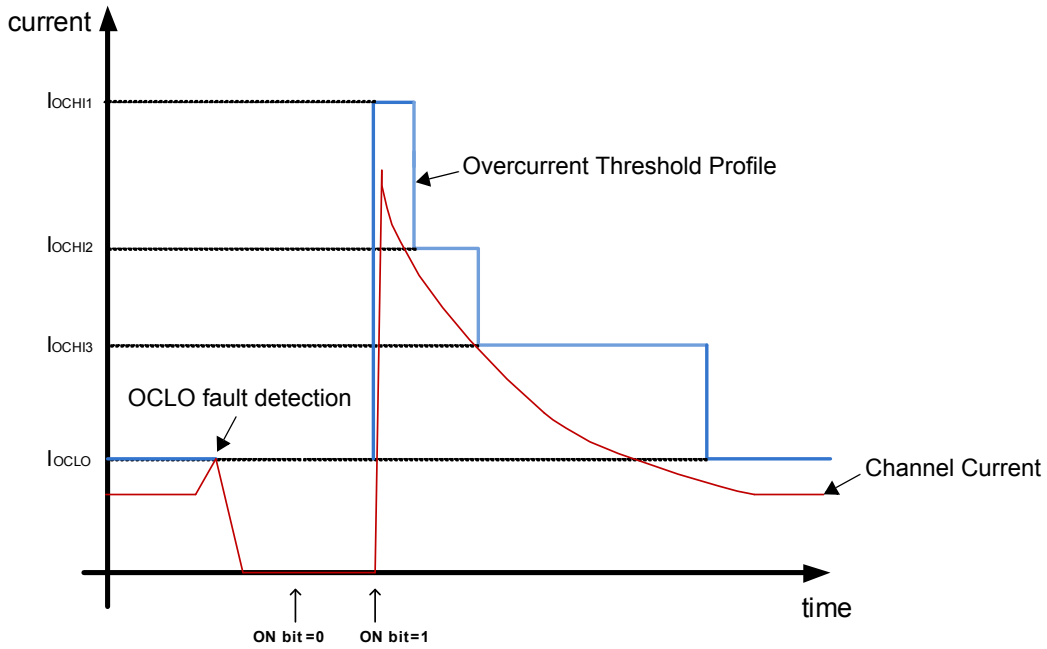


Figure 18. Resetable overcurrent profile

- rewritten (logic [1]), the OCHI window time is proceeding without reset of the OCHI counter

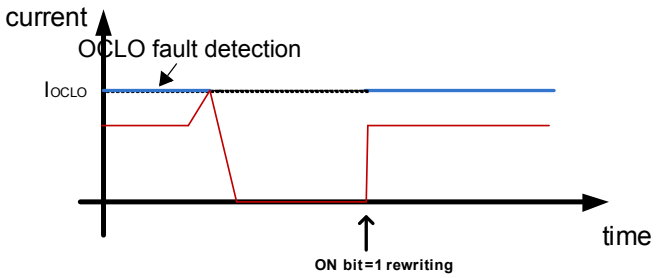


Figure 19. Overcurrent level fixed to OCLO

Fail mode

The enabling of the high current window (OCHI1:OCHI3) is dependent on INx_ON toggle signal. The enabling of output (OUT1:5) is dependent on CHx signal.

6.1.3.1.1 Overcurrent control programming

A set of overcurrent control programming functions are implemented to provide a flexible and robust system behavior:

HID ballast profile (NO_HID)

A smart overcurrent window control strategy is implemented to turn on an HID ballast, even in the case of a long power on reset time. When the output is in 100% PWM mode (including PWM clock failure in Normal mode and iINx = 1 in Fail mode), the clock for the OCHI2 time counter is divided by 8, when no load current is demanded from the output driver:

- the clock for the t_{OCHI2} counter is divided by 8 when the open load signal is high (logic[1]), to accommodate the HID ballast while in power on reset mode
- the clock for the t_{OCHI2} counter is connected directly to the window time counter when the open load signal is low (logic[0]), to accommodate the HID demanding load current from the output

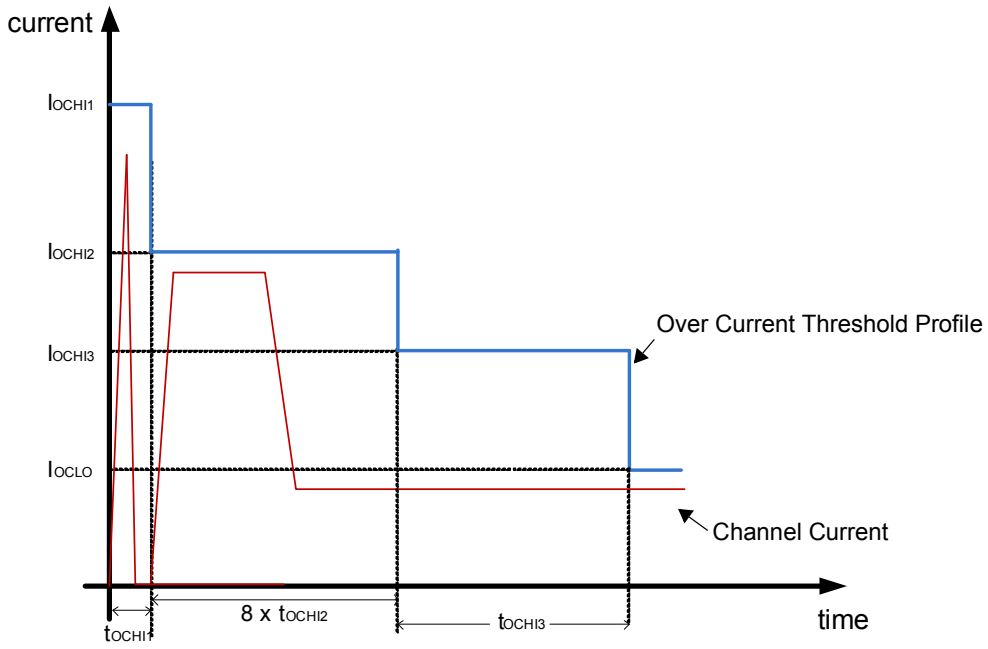


Figure 20. HID ballast overcurrent profile

This feature extends the OCHI2 time, depending on the status of the HID ballast, and ensures to bypass even a long power on reset time of HID ballast. Nominal t_{OCHI2} duration is up to 64 ms (instead of 8.0 ms). This feature is automatically active at the beginning of smart overcurrent window, except for OCHI On Demand as described by the following. The functionality is controlled by the NO_HID1 and NO_HID0 bits inside the initialization #2 register. When the NO_HID1 and NO_HID0 bits are respectively:

- [0 0]: smart HID feature is available for all channels (default status and during Fail mode)
- [0 1]: smart HID feature is available for channel 3 only
- [1 0]: smart HID feature is available for channels 3 and 4 only
- [1 1]: smart HID feature is not available for any channel

OCHI on demand (OCHI OD)

In some instances, a lamp might be de-powered when its supply is interrupted by the opening of a switch (as in a door), or by disconnecting the load (as in a trailer harness). In these cases, the driver should be tolerant of the inrush current occurring when the load is reconnected. The OCHI On Demand feature allows such control individually for each channel through the OCHI ODx bits inside the Initialization #2 register. When the OCHI ODx bit is:

- low (logic[0]), the channel operates in its Normal, Default mode. After end of OCHI window timeout the output is protected with an OCLO threshold
- high (logic[1], the channel operates in the OCHI On Demand mode and uses the OCHI2 and OCHI3 windows and times after an OCLO event

To reset the OCHI ODx bit (logic[0]) and change the response of the channel, first change the bit in the Initialization #2 register and then turn the channel off. The OCHI ODx bit is also reset after an overcurrent event at the corresponding output. The fault detection status is reported in the quick status register #1 and the corresponding channel status registers #2:#6, as presented in Figure 21.

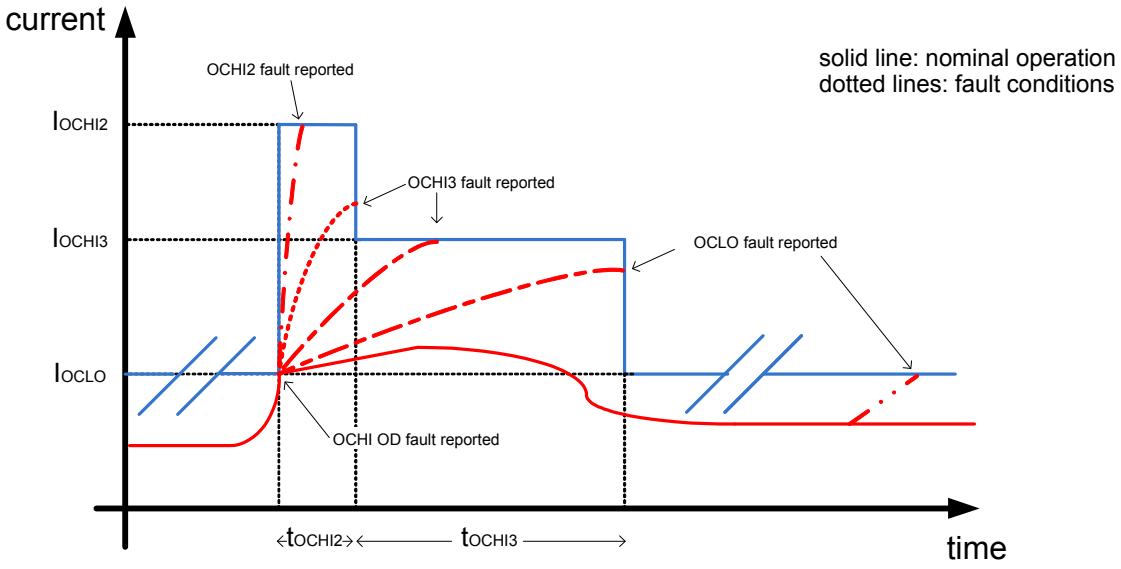


Figure 21. OCHI on demand profile

OCLO threshold setting

The static overcurrent threshold can be programmed individually for each output in two levels to adapt low duty cycle dimming and a variety of loads. The CSNS recopy factor and OCLO threshold depend on OCLO and ACM settings. The OCLO setting is controlled by the OCLOx bits inside the overcurrent control register #10-1. When the OCLOx bit is

- low (logic[0]), the output is protected with the higher OCLO threshold (default status and during Fail mode)
- high (logic[1]), the lower OCLO threshold is applied

Short OCHI

The length of the OCHI windows can be shortened by a factor of 2, to accelerate the availability of the CSNS diagnosis and to reduce the potential stress inside the switch during an overload condition. The setting is controlled individually for each output by the SHORT OCHIx bits inside the overload control register #10-2. When the SHORT OCHIx bit is:

- low (logic[0]), the default OCHI window times are applied (default status and during Fail mode)
- high (logic[1]), the short OCHI window times are applied (50% of the regular OCHI window time)

No OCHI

The switch on process of an output can be done without an OCHI window, to accelerate the availability of the CSNS diagnosis. The setting is controlled individually for each channel by the NO OCHIx bits inside the overcurrent control register #10-2. When the NO OCHIx bit is:

- low (logic[0]), the regular OCHI window is applied (default status and during Fail mode)
- high (logic[1]), the turn on of the output is provided without OCHI windows

The NO OCHI bit is applied in real time. The OCHI window is left immediately when the NO OCHI is high (logic[1]). The overcurrent threshold is set to OCLO when:

- the NO OCHIx bit is set to logic [1] while CHx is ON or
- CHx turns ON if NO OCHIx is already set

Thermal OCHI

To minimize the electro-thermal stress inside the device in case of a short-circuit, the OCHI1 level can be automatically adjusted in regards to the control die temperature. The functionality is controlled for all channels by the OCHI THERMAL bit inside the initialization 2.

When the OCHI THERMAL bit is:

- low (logic[0]), the output is protected with default OCHI1 level
- high (logic[1]), the output is protected with the OCHI1 level reduced by $R_{THERMAL\ OCHI}$ = 15% (typ) when the control die temperature is above $T_{THERMAL\ OCHI}$ = 63 °C (typ.)

Transient OCHI

To minimize the electro-thermal stress inside the device in case of a short-circuit, the OCHIx levels can be dynamically evaluated during the OFF-to-ON output transition. The functionality is controlled for all channels by the OCHI TRANSIENT bit inside the initialization 2 register.

When the OCHI TRANSIENT bit is:

- low (logic[0]), the output is protected with default OCHIx levels
- high (logic[1]), the output is protected with an OCHIx levels depending on the output voltage (V_{OUT}):
  - OCHIx level reduced by $R_{TRANSIENT\ OCHI}$ = 50% typ for $0 \leq V_{OUT} < V_{OUT\ DETECT}$ ($V_{PWR/2}$ typ)
  - Default OCHIx level for $V_{OUT\ DETECT} \leq V_{OUT}$

If the resistive load is less than V_{PWR}/I_{OCHI1}, the overcurrent threshold is exceeded before output reaches $V_{PWR/2}$, and the output current reaches I_{OCHI1}. The output is then switched off at much lower and safer currents. When the load has significant series inductance, the output current transition falls behind voltage with L_{LOAD}/R_{LOAD} constant time. The intermediate overcurrent threshold could not reach and the output current continues to rise up to OCHIx levels.

6.1.3.1.2 Electrical characterization

Table 10. Electrical characteristics

Characteristics noted under conditions 7.0 V ≤ V_{PWR} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Power outputs OUT1:OUT5						
I_{OCHI1}	High Overcurrent Level 1 for 7.0 mΩ Power Channel • T_J = -40 °C and 25 °C • T_J = 150 °C	 100 96	 111 106	 126.5 126.5	A	
I_{OCHI2}	High Overcurrent Level 2 for 7.0 mΩ Power Channel • T_J = -40 °C and 25 °C • T_J = 150 °C	 61.2 60	 70 69	 77.5 77.5	A	
I_{OCHI3}	High Overcurrent Level 3 for 7.0 mΩ Power Channel	34	39	43.5	A	
I_{OCLO}	Low Overcurrent for 7.0 mΩ Power Channel • High Level • Low Level	 17.6 8.8	 21.9 10.8	 26.4 13.2	A	
$I_{OCLO\ ACM}$	Low Overcurrent for 7.0 mΩ Power Channel in ACM Mode • High Level • Low Level	 8.8 4.4	 10.8 5.5	 13.2 6.6	A	
I_{OCHI1}	High Overcurrent Level 1 for 17 mΩ Power Channel • T_J = -40 °C and 25 °C • T_J = 150 °C	 42 40	 48 46	 54.4 54.4	A	
I_{OCHI2}	High Overcurrent Level 2 for 17 mΩ Power Channel	24.5	28.2	32.2	A	
I_{OCHI3}	High Overcurrent Level 3 for 17 mΩ Power Channel	14.8	17.3	19.5	A	
I_{OCLO}	Low Overcurrent for 17 mΩ Power Channel • High Level • Low Level	 8.8 4.4	 10.8 5.3	 13.2 6.6	A	
$I_{OCLO\ ACM}$	Low Overcurrent for 17 mΩ Power Channel in ACM Mode • High Level • Low Level	 4.4 2.2	 5.3 2.6	 6.6 3.3	A	
$R_{TRANSIENT\ OCHI}$	High Overcurrent Ratio 1	0.45	0.5	0.55		
$R_{THERMAL\ OCHI}$	High Overcurrent Ratio 2	0.835	0.85	0.865		
$T_{THERMAL\ OCHI}$	Temperature Threshold for IOCHI1 Level Adjustment	50	63	70	°C	

Table 10. Electrical characteristics (continued)

Characteristics noted under conditions 7.0 V ≤ V_{PWR} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Power outputs OUT1:OUT5 (continued)						
t_{OCHI1}	High Overcurrent Time 1 • Default Value • Short OCHI option	 1.5 0.75	 2.0 1.0	 2.5 1.25	ms	
t_{OCHI2}	High Overcurrent Time 2 • Default Value • Short OCHI option	 6.0 3.0	 8.0 4.0	 10 5.0	ms	
t_{OCHI3}	High Overcurrent Time 3 • Default Value • Short OCHI option	 48 24	 64 32	 80 40	ms	
$R_{SC\ MIN}$	Minimum Severe Short-circuit Detection • 7.0 mΩ Power Channel • 17 mΩ Power Channel	 5.0 10	 – –	 – –	mΩ	
$t_{FAULT\ SD}$	Fault Deglitch Time • OCLO and OCHI OD • OCHI1:3 and SSC	 1.0 1.0	 2.0 2.0	 3.0 3.0	µs	(19)
$t_{AUTO\ RESTART}$	Fault Autorestart Time in Fail Mode	48	64	80	ms	
$t_{BLANKING}$	Fault Blanking Time after Wake-up	–	50	100	µs	

Notes

19. Guaranteed by test mode.

6.1.3.2 Overtemperature protection

A dedicated temperature sensor is located on each power transistor, to protect the transistors and provide SPI status monitoring. The protection is based on a two stage strategy. When the temperature at the sensor exceeds the:

- selectable overtemperature warning threshold (T_{OTW1}, T_{OTW2}), the output stays on and the event is reported in the SPI
- overtemperature threshold (T_{OTS}), the output is switched off immediately after the deglitch time $t_{FAULT\ SD}$ and the event is reported in the SPI after the deglitch time $t_{FAULT\ SD}$

6.1.3.2.1 Overtemperature warning (OTW)

In case of an overtemperature warning:

- the output remains in current state
- the status is reported in the quick status register #1 and the corresponding channel status register #2:#6

The OTW threshold can be selected by the OTW SEL bit inside the initialization 2 register #1. When the bit is:

- low (logic[0]), the high overtemperature threshold is enabled (default status)
- high (logic[1]), the low overtemperature threshold is enabled

To delatch the OTW bit (OTWx):

- the temperature has to drop below the corresponding overtemperature warning threshold
- a read command of the corresponding channel status register #2:#6 must be performed

6.1.3.2.2 Overtemperature shutdown (OTS)

During an overtemperature shutdown:

- the corresponding output is disabled immediately after the deglitch time $t_{FAULT\ SD}$
- the status is reported after $t_{FAULT\ SD}$ in the quick status register #1 and the corresponding channel status register #2:#6

To restart the output after an overtemperature shutdown event in Normal mode:

- the overtemperature condition must be removed, and the channel must be restarted by a write command of the ON bit in the corresponding channel control register #2:#6, or in the output control register #8

To delatch the diagnosis:

- the overtemperature condition must be removed
- a read command of the corresponding channel status register #2:#6 must be performed

To restart the output after an overtemperature shutdown event in Fail mode:

- a mode transition is needed. Refer to Mode transitions

6.1.3.2.3 Electrical characterization

Table 11. Electrical characteristics

Characteristics noted under conditions 7.0 V ≤ V_{PWR} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Power outputs OUT1:OUT5						
T_{OW}	Overtemperature Warning • T_{OW1} level • T_{OW2} level	 100 120	 115 135	 130 150	°C	(20)
T_{OTS}	Overtemperature Shutdown	155	170	185	°C	(20)
$t_{FAULT\ SD}$	Fault Deglitch Time • OTS	2.0	5.0	10	µs	

Notes

20. Guaranteed by testmode.

6.1.3.3 Undervoltage and overvoltage protections

6.1.3.3.1 Undervoltage

During an undervoltage condition (V_{PWRPOR} ≤ V_{PWR} ≤ $V_{PWR\ UVF}$), all outputs (OUT1:OUT5) are switched off immediately after deglitch time $t_{FAULT\ SD}$. The undervoltage condition is reported after the deglitch time $t_{FAULT\ SD}$:

- in the device status flag (DSF) in the registers #1:#7
- in the undervoltage flag (UVF) inside the device status register #7

Normal mode

The reactivation of the outputs is controlled by the microcontroller. To restart, the output the undervoltage condition must be removed and:

- a write command of the ON Bit must be performed in the corresponding channel control register #2:#6 or in the output control register #8

To delatch the diagnosis:

- the undervoltage condition must be removed
- a read command of the device status register #7 must be performed

Fail mode

When the device is in Fail mode, the restart of the outputs is controlled by the autorestart feature.

6.1.3.3.2 Overvoltage

The device is protected against overvoltage on V_{PWR}.

- During the jump start condition, the device may be operated, but with respect to the device limits
- During the load dump condition ($V_{PWR\ LD\ MAX}$ = 40 V) the device does not conduct energy to the loads

The overvoltage condition ($V_{PWR} \geq V_{PWR\ OVF}$) is reported in the:

- device status flag (DSF) in the registers #1:#7
- overvoltage flag (OVF) inside the device status register #7

To delatch the diagnosis:

- the overvoltage condition must be removed
- a read command of the device status register #7 must be performed

During an overvoltage ($V_{PWR} \geq V_{PWR\ HIGH}$), the device is not “short-circuit” proof.

6.1.3.3.3 Electrical characterization

Table 12. Electrical characteristics

Characteristics noted under conditions 7.0 V ≤ V_{PWR} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Supply VPWR						
$V_{PWR\ UVF}$	Supply Undervoltage	5.0	5.25	5.5	V	
$V_{PWR\ UVF\ HYS}$	Supply Undervoltage Hysteresis	200	350	500	mV	
$V_{PWR\ OVF}$	Supply Overvoltage	28	30	32	V	
$V_{PWR\ OVF\ HYS}$	Supply Overvoltage Hysteresis	0.5	1.0	1.5	V	
$V_{PWR\ LD\ MAX}$	Supply Load Dump Voltage (2.0 min at 25 °C)	40	–	–	V	
$V_{PWR\ HIGH}$	Maximum Supply Voltage for Short-circuit Protection	32	–	–	V	
$t_{FAULT\ SD}$	Fault Deglitch Time • UV and OV	2.0	3.5	5.5	µs	

6.1.3.4 Charge pump protection

The charge pump voltage is monitored in order to protect the smart switches in case of:

- power up
- failure of external capacitor
- failure of charge pump circuitry

During power up, when the charge pump voltage has not yet settled to its nominal output voltage range, the outputs can not be turned on. Any turn on command during this phase is executed immediately after settling of the charge pump. When the charge pump voltage is not within its nominal output voltage range:

- the power outputs are disabled immediately after the deglitch time $t_{FAULT\ SD}$
- the failure status is reported after $t_{FAULT\ SD}$ in the device status flag DSF in the registers #1:#7 and the CPF in the quick status register #1
- Any turn on command during this phase is executed including the OCHI windows immediately after the charge pump output voltage has reached its valid range

To delatch the diagnosis:

- the charge pump failure condition must be removed
- a read command of the quick status register #1 is necessary

6.1.3.4.1 Electrical characterization

Table 13. Electrical characteristics

Characteristics noted under conditions 7.0 V ≤ V_{PWR} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Charge pump CP						
C_{CP}	Charge Pump Capacitor Range (Ceramic type X7R)	47	–	220	nF	
$V_{CP\ MAX}$	Maximum Charge Pump Voltage	–	–	16	V	
$t_{FAULT\ SD}$	Fault Deglitch Time • CPF	–	4.0	6.0	µs	

6.1.3.5 Reverse supply protection

The device is protected against reverse polarity of the V_{PWR} line. In reverse polarity condition:

- the output transistors OUT1:5 are turned ON in order to prevent the device from thermal overload
- the OUT6 pin is pulled down to GND. An external current limit resistor shall be added in series with OUT6 pin
- no output protection is available in this condition

6.1.4 Output clamps

6.1.4.1 Negative output clamp

In case of an inductive load (L), the energy is dissipated after the turn-off inside the N-channel MOSFET. When t_{CL} (=Io x L/V_{CL}) > 1.0 ms, the turn-off waveform can be simplified with a rectangle as shown in Figure 22.

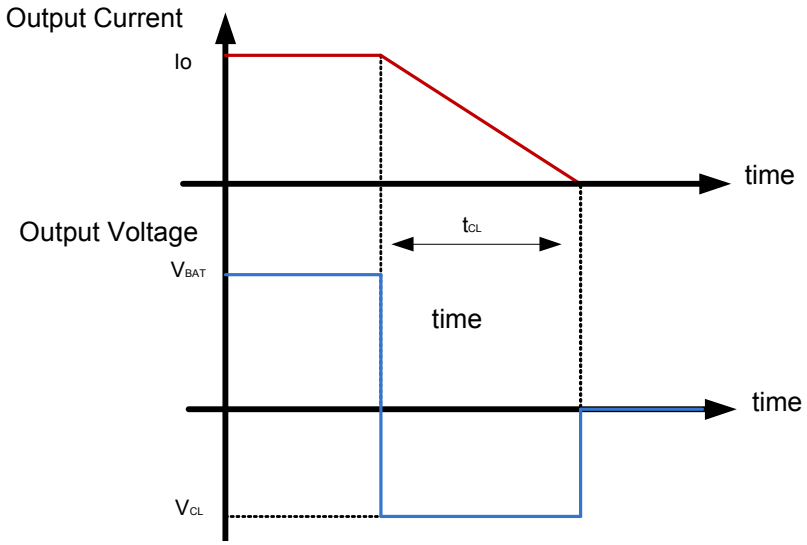


Figure 22. Simplified negative output clamp waveform

The energy dissipated in the N-Channel MOSFET is: E_{CL} = 1/2 x L x Io² x (1+ V_{PWR}/|V_{CL}|). In the case of t_{CL} < 1.0 ms, contact the factory for guidance.

6.1.4.2 Supply clamp

The device is protected against dynamic overvoltage on the V_{PWR} line by means of an active gate clamp, which activates the output transistors in order to limit the supply voltage ($V_{DCCLAMP}$). In case of an overload on an output the corresponding switch is turned off, which leads to high voltage at V_{PWR} with an inductive V_{PWR} line. The maximum V_{PWR} voltage is limited at $V_{DCCLAMP}$ by active clamp circuitry through the load.

6.1.4.3 Electrical characterization

Table 14. Electrical characteristics

Characteristics noted under conditions 7.0 V ≤ V_{PWR} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Supply VPWR						
$V_{DCCLAMP}$	Supply Clamp Voltage	41	–	50	V	
Power outputs OUT1:OUT5						
V_{CL}	Negative Power Channel Clamp Voltage • 7.0 mΩ • 17 mΩ	 -20.5 -21	 – –	 -17.5 -18	V	

6.1.5 Digital Diagnostics

The device offers several modes for load status detection in on state and off state through the SPI.

6.1.5.1 Open load detections

6.1.5.1.1 Open load in on state

Open load detection during ON state is provided for each power output (OUT1:OUT5), based on the current monitoring circuit. The detection is activated automatically when the output is in on state. The detection threshold is dependent on:

- the OLLED EN bits inside the OLLED control register #13-2

The detection result is reported in:

- the corresponding QSFx bit in the quick status register #1
- the global open load flag OLF (registers #1:#7)
- the OLON bit of the corresponding channel status registers #2:#6

To delatch the diagnosis:

- the open load condition must be removed
- a read command of the corresponding channel status register #2:#6 must be performed

When an open load has been detected, the output remains in on state. The deglitch time of the open load in on state can be controlled individually for each output to be compliant with different load types. The setting is dependent on the OLON DGL bits inside the open load control register #13-1:

- low (logic[0]) the deglitch time is $t_{OLON\ DGL}$ = 64 µs typ (bulb mode)
- high (logic[1]) the deglitch time is $t_{OLON\ DGL}$ = 2.0 ms typ (converter mode)

The deglitching filter is reset whenever output falls low and is only active when the output is high.

6.1.5.1.2 Open load in on state for LED

For detection of small load currents (e.g. LED) in on state of the switch a special low current detection mode is implemented by using the OLLED EN bit. The detection principle is based on a digital decision during regular switch off of the output. Thereby a current source (I_{OLLED}) is switched on and the falling edge of the output voltage is evaluated by a comparator at V_{PWR}- 0.75 V (typ).

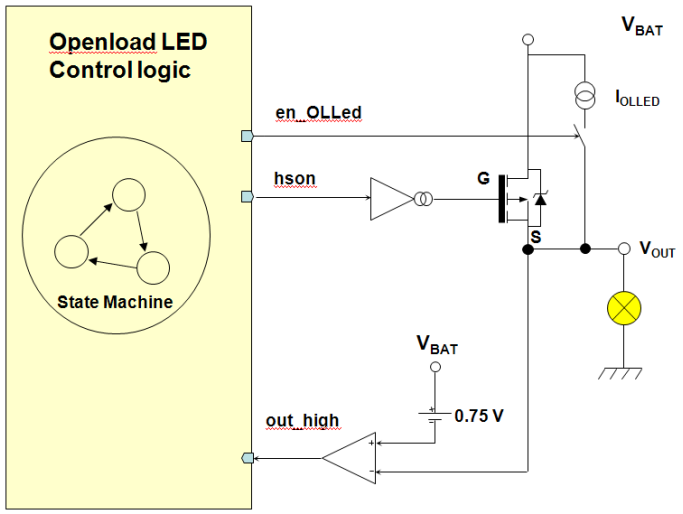


Figure 23. Open load in on state diagram for LED

The OLLED fault is reported when the output voltage is above V_{PWR} - 0.75 V after 2.0 ms off-time or at each turn-on command in case of off-time < 2.0 ms. The detection mode is enabled individually for each channel with the OLLED EN bits inside the LED control register #13-2. When the corresponding OLLED EN bit is:

- low (logic[0]), the standard open load in on state (OLON) is enabled
- high (logic[1]), the OLLED detection is enabled

The detection result is reported in:

- the corresponding QSFx bit in the quick status register #1
- the global open load flag OLF (register #1:#7)
- the OLON bit of the corresponding channel status register #2:#6

When an open load has been detected, the output remains in the on state. When output is in PWM operation:

- the detection is performed at the end of the on time of each PWM cycle
- the detection is active during the off time of the PWM signal, up to 2.0 ms max.

The current source (I_{OLLED}) is disabled after “no OLLED” detection or after 2.0 ms.

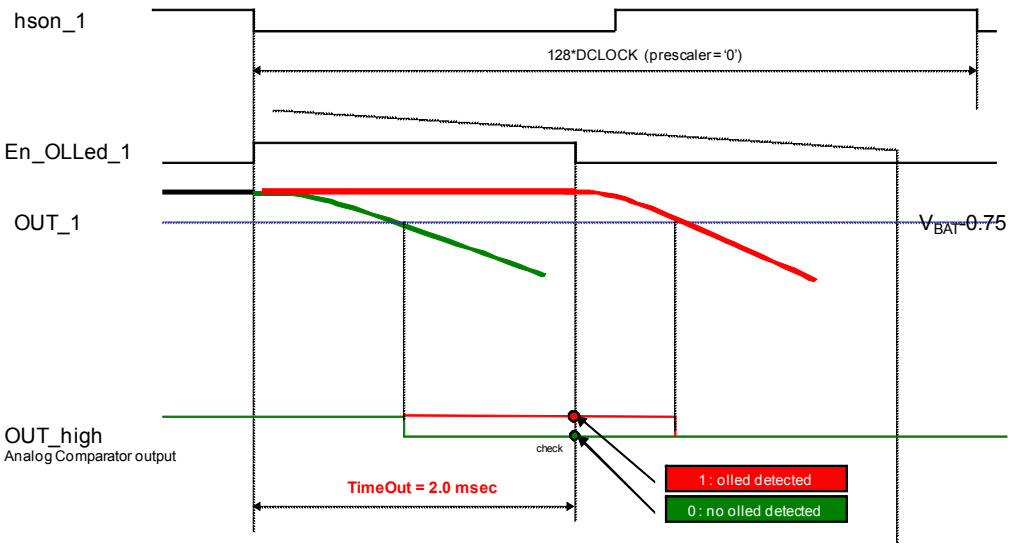


Figure 24. Open load in on state for LED in PWM operation (off time > 2.0 ms)

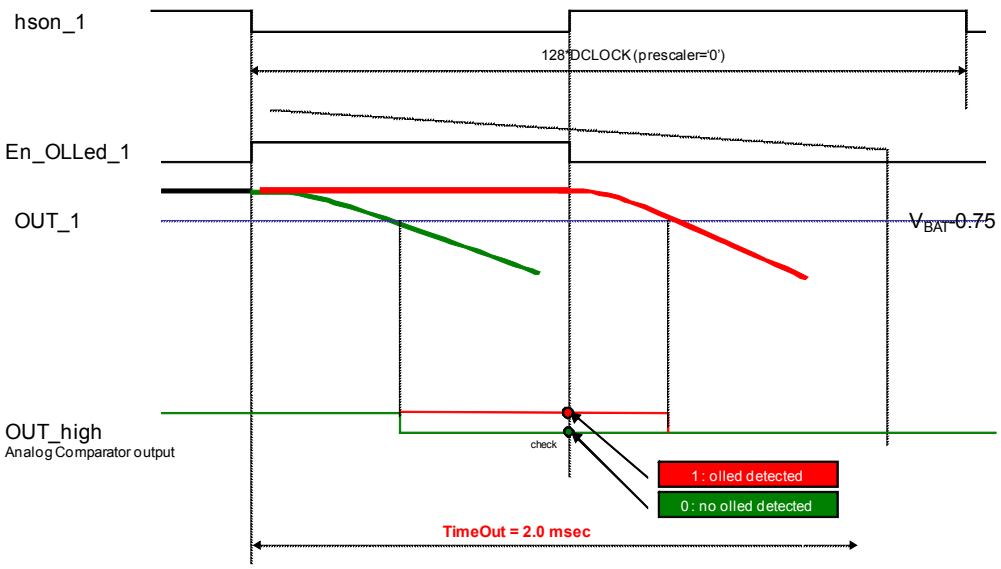


Figure 25. Open load in on state for LED in PWM operation (off time < 2.0 ms)

When output is in fully ON operation (100% PWM):

- the detection on all outputs is triggered by setting the OLLED TRIG bit inside the LED control register #13-2
- at the end of detection time, the current source (I_{OLLED}) is disabled 100 µsec (typ.) after the output reactivation

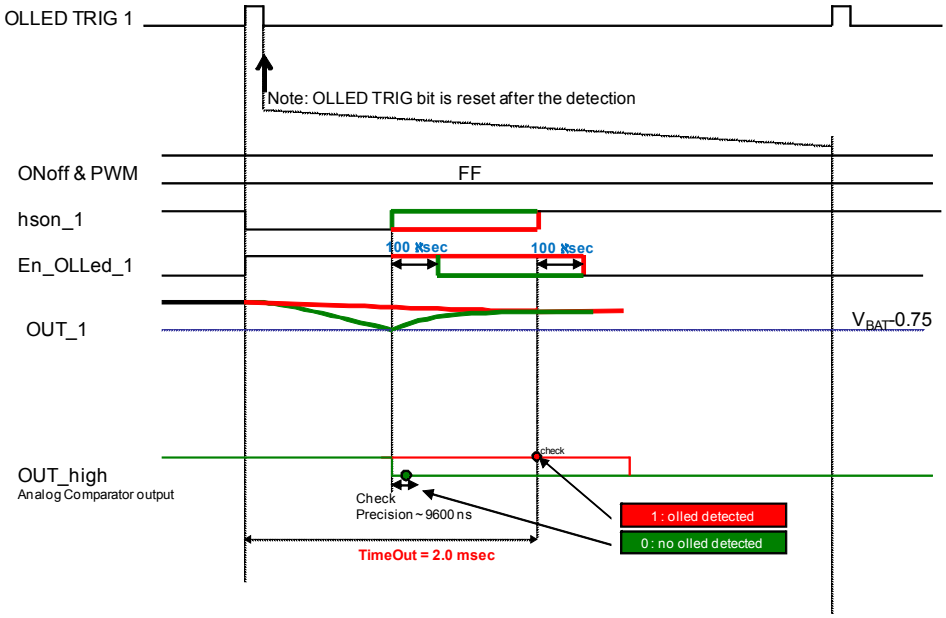


Figure 26. Open load in on state for LED in fully on operation

The OLLED TRIG bit is reset after the detection. To delatch the diagnosis:

- a read command of the corresponding channel status register #2:#6 must be performed

A false “open” result could be reported in the OLON bit:

- for high duty cycles, the PWM off-time becomes too short
- for capacitive load, the output voltage slope becomes too slow

6.1.5.1.3 Open load in off state

An open load in off state detection is provided individually for each power output (OUT1:OUT5). The detection is enabled individually for each channel by the OLOFF EN bits inside the open load control register #13-1. When the corresponding OLOFF EN is:

- low (logic[0]), the diagnosis mode is disabled (default status)
- high (logic[1]), the diagnosis mode is started for t_{OLOFF}. It is not possible to restart any OLOFF or disable the diagnosis mode during active OLOFF state

This detection can be activated independently for each power output (OUT1:OUT5). When it is activated, it is always activated synchronously for all selected outputs (with positive edge of CSB). When the detection is started, the corresponding output channel is turned on with a fixed overcurrent threshold of I_{OLOFF} threshold. When this overcurrent threshold is:

- reached within the detection timeout t_{OLOFF}, the output is turned off and the OLOFF EN bit is reset. No OCLOx and no OLOFFx is reported
- not reached within the detection timeout t_{OLOFF}, the output is turned off after t_{OLOFF} and the OLOFF EN bit is reset. The OLOFFx is reported

The overcurrent behavior as commanded by the overcurrent control settings (NO OCHIx, OCHI ODx, SHORTOCHIx, OCLOx, and ACM ENx) is not be affected by applying the OLOFF ENx bit. The same is true for the output current feedback and the current sense synchronization. The detection result is reported in:

- the corresponding QSFx bit in the quick status register #1
- the global open load flag OLF (register #1:#7)
- the OLOFF bit of the corresponding channel status register #2:#6

To delatch the diagnosis, a read command of the corresponding channel status register #2:#6 must be performed. In case of any fault during t_{OLOFF} (OTS, UV, CPF,), the open load in off state detection is disabled and the output(s) is (are) turned off after the deglitch time $t_{FAULT\ SD}$. The corresponding fault is reported in the SPI SO registers.

6.1.5.1.4 Electrical characterization

Table 15. Electrical characteristics

Characteristics noted under conditions 7.0 V ≤ V_{PWR} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Power outputs OUT1:OUT5						
I_{OL}	Open Load Current Threshold in ON State • 7.0 mΩ Power Channel at T_J = -40 °C • 7.0 mΩ Power Channel at T_J = 25 °C and 125 °C • 17 mΩ Power Channel at T_J = -40 °C • 17 mΩ Power Channel at T_J = 25 °C and 125 °C	 50 100 30 50	 200 200 100 100	 350 300 160 150	mA	
$\delta_{PWM\ OLON}$	Output PWM Duty Cycle Range for Open Load Detection in ON state • Low Frequency Range (25 to 100 Hz) • Medium Frequency Range (100 to 200 Hz) • High Frequency Range (200 to 400 Hz)	 18 18 17	 – – –	 – – –	LSB	
I_{OLLED}	Open Load Current Threshold in ON state/OLLED mode	2.0	4.0	5.0	mA	
$t_{OLLED100}$	Maximum Open Load Detection Time/OLLED mode with 100% duty cycle	1.5	2.0	2.6	ms	
t_{OLOFF}	Open Load Detection Time in OFF State	0.9	1.2	1.5	ms	
$t_{FAULT\ SD}$	Fault Deglitch Time • OLOFF • OLON with OLON DGL = 0 • OLON with OLON DGL = 1	 2.0 48 1.5	 3.3 64 2.0	 5.0 80 2.5	 µs ms ms	
I_{OLOFF}	Open Load Current Threshold in OFF state • 7.0 mΩ power channel • 17 mΩ power channel	 0.77 0.385	 1.1 0.55	 1.43 0.715	A	

6.1.5.2 Output shorted to v_{pwr} in off state

A short to V_{PWR} detection during OFF state is provided individually for each power output OUT1:OUT5, based on an output voltage comparator referenced to $V_{PWR/2}$ ($V_{OUT\ DETECT}$) and an external pull-down circuitry. The detection result is reported in the OUTx bits of the I/O status register #8 in real time. In case of UVF, the OUTx bits are undefined.

6.1.5.2.1 Electrical characterization

Table 16. Electrical characteristics

Characteristics noted under conditions 7.0 V ≤ V_{PWR} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Power outputs OUT1:OUT5						
$V_{OUTDETECT}$	Output Voltage Comparator Threshold	0.42	0.5	0.58	V_{PWR}	

6.1.5.3 SPI fault reporting

Protection and monitoring of the outputs during normal mode is provided by digital switch diagnosis via the SPI. The selection of the SO data word is controlled by the SOA0:SOA3 bits inside the initialization 1 register #0. The device provides two different reading modes, depending on the SOA MODE bit. When the SOA MODE bit is:

- low (logic[0]), the programmed SO address is used for a single read command. After the reading, the SO address returns to quick status register #1 (default state)
- high (logic[1]), the programmed SO address is used for the next and all further read commands until a new programming

The “quick status register” #1 provides one glance failure overview. As long as no failure flag is set (logic[1]), no control action by the microcontroller is necessary.

Register	SO address					SO data											
	#	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
quick address	1	0	0	0	1	FM	DSF	OVLF	OLF	CPF	RCF	CLKF	QSF5	QSF4	QSF3	QSF2	QSF1

- FM: Fail mode indication. This bit is also present in all other SO data words, and indicates the fail mode by a logic[1]. When the device is in Normal mode, the bit is logic[0]
- global device status flags (D10:D8): These flags are also present in the channel status registers #2:#6, the device status register #7, and are cleared when all fault bits are cleared by reading the registers #2:#7
- DSF = device status flag (RCF, or UVF, or OVF, or CPF, or CLKF, or TMF). UVF and TMF are also reported in the device status register #7
- OVLF = over load flag (wired OR of all OC and OTS signals)
- OLF = open load flag
- CPF: charge pump flag
- RCF: registers clear flag: this flag is set (logic[1]) when all SI and SO registers are reset
- CLKF: clock fail flag. Refer to Logic I/O plausibility check
- QSF1:QSF5: channel quick status flags (QSFx = OC0x, or OC1x, or OC2x, or OTWx, or OTSx, or OLONx, or OLOFFx)

The SOA address #0 is also mapped to register #1 (D15:D12 bits report logic [0001]). When a fault condition is indicated by one of the quick status bits (QSF1:QSF5, OVLF, OLF), the detailed status can be evaluated by reading of the corresponding channel status registers #2:#6.

Register	SO address					SO data											
	#	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CH1 status	2	0	0	1	0	FM	DSF	OVLF	OLF	res	OTS1	OTW1	OC21	OC11	OC01	OLON1	OLOFF1
CH2 status	3	0	0	1	1	FM	DSF	OVLF	OLF	res	OTS2	OTW2	OC22	OC12	OC02	OLON2	OLOFF2
CH3 status	4	0	1	0	0	FM	DSF	OVLF	OLF	res	OTS3	OTW3	OC23	OC13	OC03	OLON3	OLOFF3

Register	SO address					SO data										
	#	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CH4 status	5	0	1	0	1	FM	DSF	OVLF	OLF	res	OTS4	OTW4	OC24	OC14	OC04	OLON4	OLOFF4
CH5 status	6	0	1	1	0	FM	DSF	OVLF	OLF	res	OTS5	OTW5	OC25	OC15	OC05	OLON5	OLOFF5

- OTSx: overtemperature shutdown flag
- OTWx: overtemperature warning flag
- OC0x:OC2x: overcurrent status flags
- OLONx: open load in on state flag
- OLOFFx: open load in off state flag

The most recent OC fault is reported by the OC0x:OC2x bits, if a new OC occurs before an old OC on the same output that was read.

#2~#6	*OC2x*	*OC1x*	*OC0x*	*over current status*
	0	*0*	*0*	*no overcurrent*
	0	*0*	*1*	*OCHI1*
	0	*1*	*0*	*OCHI2*
	0	*1*	*1*	*OCHI3*
	1	*0*	*0*	*OCLO*
	1	*0*	*1*	*OCHIOD*
	1	*1*	*0*	*SSC*
	1	*1*	*1*	*not used*

When a fault condition is indicated by one of the global status bits (FM, DSF), the detailed status can be evaluated by reading of the device status registers #7:

Register	SO address					SO data										
	#	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
device status	7	0	1	1	1	FM	DSF	OVLF	OLF	res	res	res	TMF	OVF	UVF	SPIF	iLMP

- TMF: testmode activation flag. Testmode is used for manufacturing testing only. If this bit is set to logic [1], the MCU shall reset the device
- OVF: overvoltage flag
- UVF: undervoltage flag
- SPIF: SPI fail flag
- iLIMP (real time reporting after the t_{IN_DGL}, not latched)

The I/O status register #8 can be used for system test, fail mode test and the power down procedure:

Register	SO address					SO data										
	#	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
I/O status	8	1	0	0	0	FM	res	TOGGLE	iIN4	iIN3	iIN2	iIN1	OUT5	OUT4	OUT3	OUT2	OUT1

The register provides the status of the control inputs, the toggle signal, and the power outputs state in real time (not latched).

- TOGGLE = status of the 4 input toggle signals (IN1_ON, or IN2_ON, or IN3_ON, or IN4_ON), reported in real time
- iINx = status of iINx signal (real time reporting after the t_{IN_DGL}, not latched)
- OUTx = status of output pins OUTx (the detection threshold is $V_{PWR/2}$) when undervoltage condition does not occur

The device can be clearly identified by the device ID register #9 when the supply voltage is within its nominal range:

Register	SO address					SO data											
	#	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
device ID	9	1	0	0	1	X	X	X	X4	DEVID 7	DEVID 6	DEVID 5	DEVID 4	DEVID 3	DEVID 2	DEVID 1	DEVID 0

The register delivers DEVIDx bits = 40hex for the 07XS6517. During undervoltage condition (UVF = 1), DEVIDx bits report 00hex.

6.1.6 Analog diagnostics

The analog feedback circuit (CSNS) is implemented to provide load and device diagnostics during Normal mode. During Fail and Sleep modes, the analog feedback is not available. The routing of the integrated multiplexer is controlled by MUX0:MUX2 bits inside the initialization 1 register #0.

6.1.6.1 Output current monitoring

The current sense monitor provides a current proportional to the current of the selected output (OUT1:OUT5). CSNS output delivers 1.0 mA full scale range current source reporting channel 1:5 current feedback (I_{FSR}).

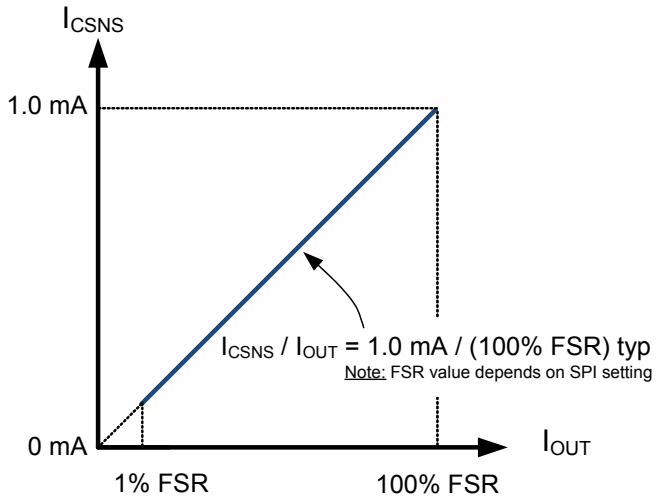


Figure 27. Output current sensing

The feedback is suppressed during OCHI window ($t \leq t_{OCHI1} + t_{OCHI2} + t_{OCHI3}$) and only enabled during low overcurrent shutdown threshold (OCLO). During PWM operation, the current feedback circuit (CSNS) delivers current only during the on time of the output switch. Current sense settling time, $t_{CSNS(SET)}$, varies with current amplitude. Current sense valid time, $t_{CSNS(VAL)}$, depends on the PWM frequency (see Electrical characterization).

An advanced current sense mode (ACM) is implemented in order to diagnose LED loads in Normal mode and to improve current sense accuracy for low current loads. In the ACM mode, the offset sign of current sense amplifier is toggled on every CSNS SYNCB rising edge. The error amplifier offset contribution to the CSNS error can be fully eliminated from the measurement result by averaging each two sequential current sense measurements. The ACM mode is enabled with the ACM ENx bits inside the ACM control register #10-1. When the ACM ENx bit is:

- low (logic[0]), ACM disabled (default status and during Fail mode)
- high (logic[1]), ACM enabled

In ACM mode:

- the precision of the current recopy feature (CSNS) is improved, especially at low output currents by averaging CSNS reporting on sequential PWM periods
- the current sense full scale range (FSR) is reduced by a factor of two
- the overcurrent protection threshold OCLO is reduced by a factor of two

Figure 28 describes the timings between the selected channel current and the analog feedback current. Current sense validation time pertains to stabilization time needed after turn on. Current sense settling time pertains to the stabilization time needed after the load current changes while the output is continuously on or when another output signal is selected.

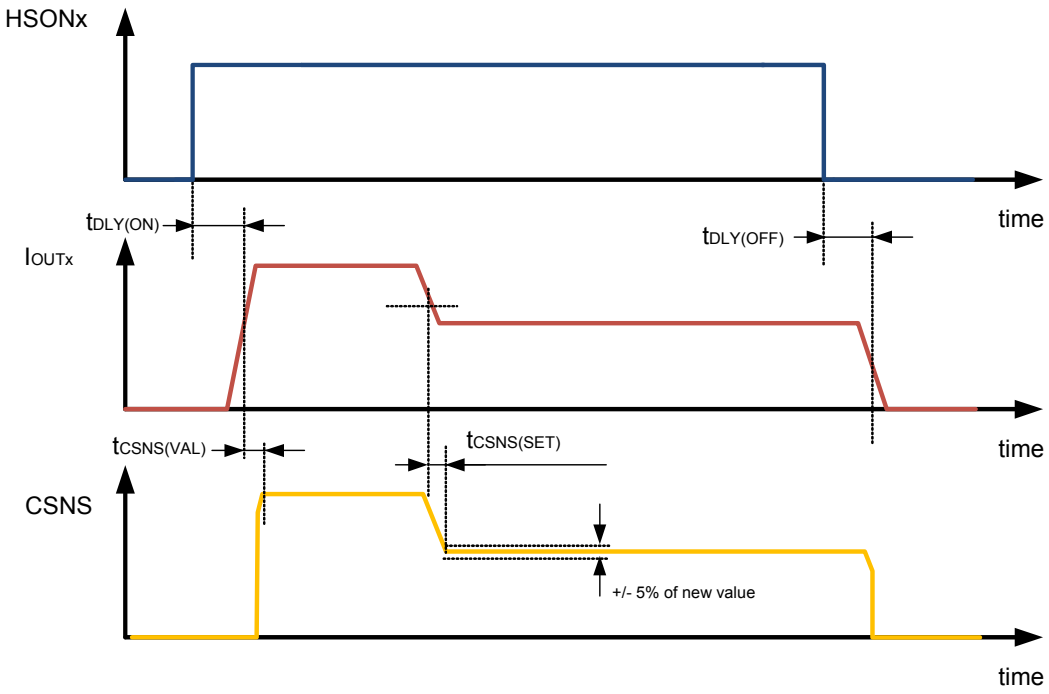


Figure 28. Current sensing response time

Internal circuitry limits the voltage of the CSNS pin when its sense resistor is absent. This feature prevents damage to other circuitry sharing that electrical node, such as a microcontroller pin, for example. Several 12XSF may be connected to one shared CSNS resistor.

6.1.6.2 Supply voltage monitoring

The V_{PWR} monitor provides a voltage proportional to the supply tab. The CSNS voltage is proportional to the V_{PWR} voltage as shown in Figure 29.

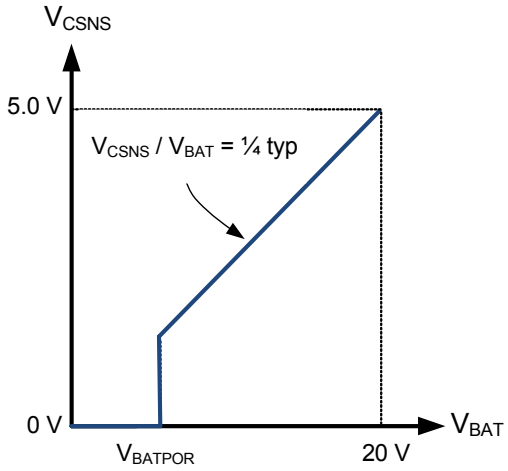


Figure 29. Supply voltage reporting

6.1.6.3 Temperature monitoring

The average temperature of the control die is monitored by an analog temperature sensor. The CSNS pin can report the voltage of this sensor.

The chip temperature monitor output voltage is independent of the resistor connected to the CSNS pin, provided the resistor is within the min/max range of 5.0 kΩ to 50 kΩ. Temperature feedback range, T_{FB}, -40 °C to 150 °C.

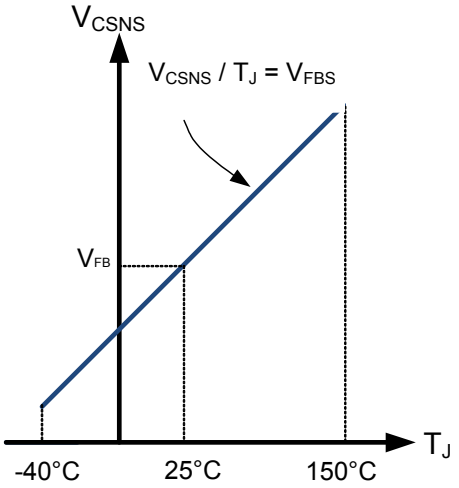


Figure 30. Temperature reporting

6.1.6.4 Analog diagnostic synchronization

A current sense synchronization pin is provided to simplify the synchronous sampling of the CSNS signal. The CSNS SYNCB pin is an open drain requiring an external 5.0 kΩ (min.) pull-up resistor to V_{CC}. The CSNS SYNC signal is:

- available during Normal mode only
- behavior depends on the type of signal selected by the MUX2:MUX0 bits in the initialization 1 register #0. This signal is either a current proportional to an output current or a voltage proportional to temperature or the supply voltage

Current sense signal

When a current sense signal is selected:

- the pin delivers a recopy of the output control signal during on phase of the PWM defined by the SYNC EN0, SYNC EN1 bits inside the initialization 1 register #0

SYNC EN1	SYNC EN0	Setting	Behavior
0	0	OFF	CSNS SYNC is inactive (high)
0	1	VALID	CSNS SYNC is active (low) when CSNS is valid. During switching the output of MUXMUX, the CSNS SYNC is inactive (high)
1	0	TRIG0	As in setting VALID, but after a change of the MUX, the CSNS SYNC is inactive (high) until the next PWM cycle is started
1	1	TRIG1/2	Pulses (active low) from the middle of the CSNS pulse to its end are generated. Switching phases (output and MUX) and the time from the MUX switching to the next middle of the CSNS pulse are blanked (high)

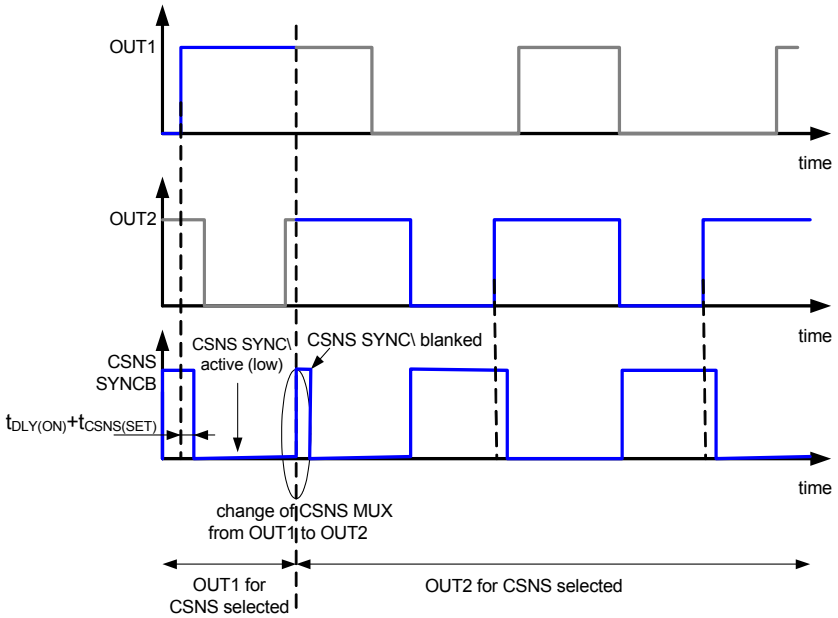


Figure 31. CSNS SYNCB valid setting

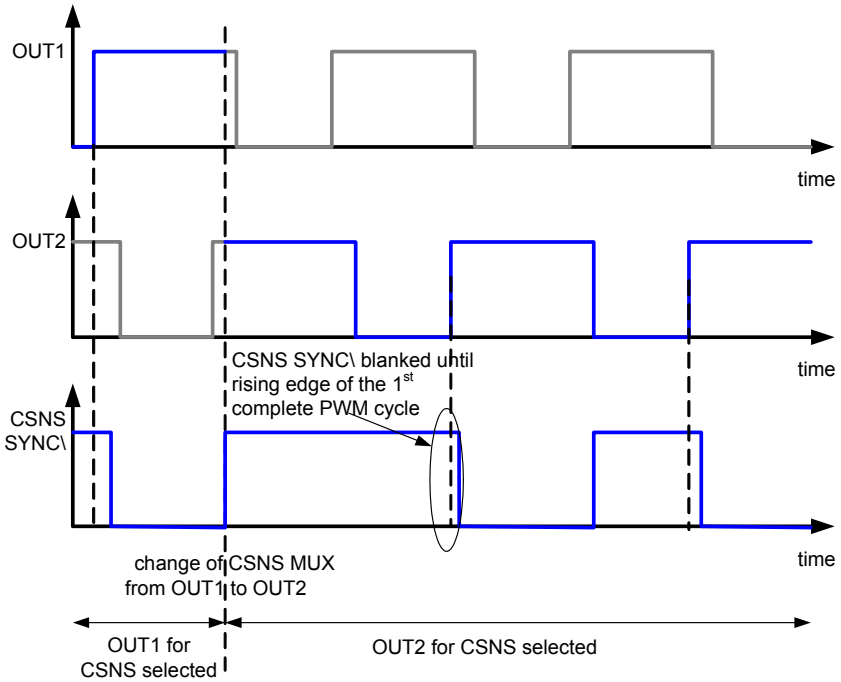


Figure 32. CSNS SYNCB TRIG0 setting

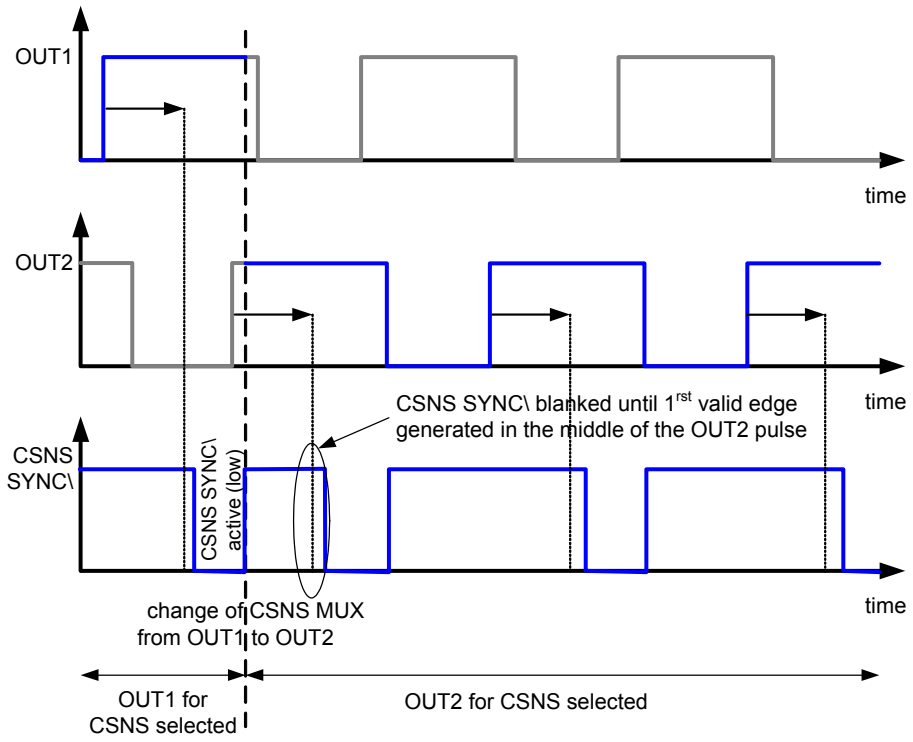


Figure 33. CSNS SYNCB TRIG1/2 setting

- the CSNS SYNCB pulse is suppressed during OCHI and during OFF phase of the PWM
- the CSNS SYNCB is blanked during settling time of the CSNS multiplexer and ACM switching by a fixed time of $t_{DLY(ON)}$ + $t_{CSNS(SET)}$
- when a PWM clock fail is detected, the CSNS SYNCB delivers a signal with 50% duty cycle at a fixed period of 6.5 ms
- when the output is programmed with 100% PWM, the CSNS SYNCB delivers a logic[0] a high pulse with the length of 100 µs (typ.) during the PWM counter overflow for TRIG0 and TRIG1/2 settings, as shown in Figure 34

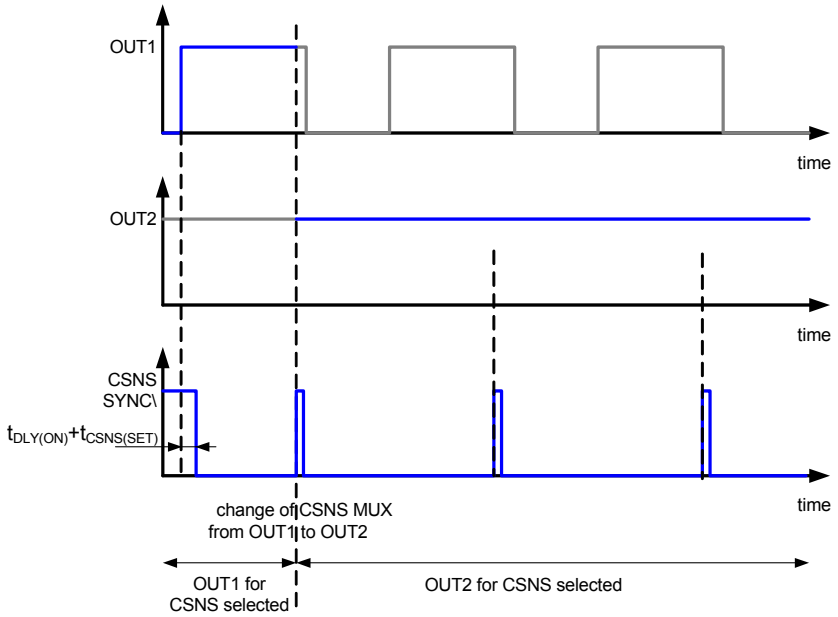


Figure 34. CSNS SYNCB when the output is programmed with 100%

- In case of output fault, the CSNS SYNCB signal for current sensing does not deliver a trigger signal until the output is enabled again

Temperature signal or V_{PWR} monitor signal

When a voltage signal (average control die temperature or supply voltage) is selected:

- the CSNS SYNCB delivers a signal with 50% duty cycle and the period of the lowest prescaler setting (f_{CLK}/1024)
- and a PWM clock fail is detected, the CSNS SYNCB delivers a signal with 50% duty cycle at a fixed period of 6.5 ms ($t_{SYNC\ DEFAULT}$)

6.1.6.5 Electrical characterization

Table 17. Electrical characteristics

Characteristics noted under conditions 7.0 V ≤ V_{PWR} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Current sense CSNS						
R_{CSNS}	Current Sense Resistor Range	5.0	–	50	kΩ	
$I_{CSNS\ LEAK}$	Current Sense Leakage Current when CSNS is disabled	-1.0	–	+1.0	µA	
V_{CS}	Current Sense Clamp Voltage	6.0	–	8.0	V	
I_{FSR}	Current Sense Full Scale Range for 7.0 mΩ Power Channel • High OCLO and ACM = 0 • Low OCLO and ACM = 0 • High OCLO and ACM = 1 • Low OCLO and ACM = 1	 – – – –	 22 11 11 5.5	 – – – –	A	
ACC I_{CSNS}	Current Sense Accuracy for 9.0 V ≤ V_{PWR} ≤ 18 V for 7.0 mΩ Power Channel • I_{OUT} = 80% FSR • I_{OUT} = 25% FSR • I_{OUT} = 10% FSR • I_{OUT} = 5.0% FSR	 -11 -14 -20 -29	 – – – –	 +11 +14 +20 +29	%	
ACC $I_{CSNS\ 1\ CAL}$	Current Sense Accuracy for 9.0 V ≤ V_{PWR} ≤ 18 V with one calibration point at 25 °C for 50% FSR and V_{PWR} = 14 V for 7.0 mΩ Power Channel • I_{OUT} = 80% FSR • I_{OUT} = 25% FSR • I_{OUT} = 10% FSR • I_{OUT} = 5.0% FSR	 -7.0 -7.0 -20 -29	 – – – –	 +7.0 +7.0 +20 +29	%	(25) (23)
ACC $I_{CSNS\ 2\ CAL}$	Current Sense Accuracy for 9.0 V ≤ V_{PWR} ≤ 18 V with two calibration points at 25 °C for 2.0% and 50% FSR and V_{PWR} = 14 V for 7.0 mΩ Power Channel • I_{OUT} = 80% FSR • I_{OUT} = 25% FSR • I_{OUT} = 10% FSR • I_{OUT} = 5.0% FSR	 -6.0 -6.0 -8.0 -12	 – – – –	 +6.0 +6.0 +8.0 +12	%	(25) (23)
$I_{CSNSMIN}$	Minimum Current Sense Reporting for 7.0 mΩ • 9.0 V < V_{PWR} < 18 V	–	–	1.0	%	(21) (24)
I_{FSR}	Current Sense Full Scale Range for 17 mΩ Power Channel • High OCLO and ACM = 0 • Low OCLO and ACM = 0 • High OCLO and ACM = 1 • Low OCLO and ACM = 1	 – – – –	 11 5.5 5.5 2.75	 – – – –	A	

Table 17. Electrical characteristics (continued)

Characteristics noted under conditions 7.0 V ≤ V_{PWR} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Current sense CSNS (continued)						
ACC I_{CSNS}	Current Sense Accuracy for 9.0 V ≤ V_{PWR} ≤ 18 V for 17 mΩ Power Channel • I_{OUT} = 80% FSR • I_{OUT} = 25% FSR • I_{OUT} = 10% FSR • I_{OUT} = 5.0% FSR	 -11 -14 -20 -29	 – – – –	 +11 +14 +20 +29	%	(21)
ACC $I_{CSNS\ 1\ CAL}$	Current Sense Accuracy for 9.0 V ≤ V_{PWR} ≤ 18 V with one calibration point at 25 °C for 2% or 50% FSR and V_{PWR} = 14 V for 17 mΩ Power Channel • I_{OUT} = 80% FSR • I_{OUT} = 25% FSR • I_{OUT} = 10% FSR • I_{OUT} = 5.0% FSR	 -7.0 -7.0 -20 -29	 – – – –	 +7.0 +7.0 +20 +29	%	(21) (23)
ACC $I_{CSNS\ 2\ CAL}$	Current Sense Accuracy for 9.0 V ≤ V_{PWR} ≤ 18 V with two calibration points at 25 °C for 2.0% and 50% FSR and V_{PWR} = 14 V for 17 mΩ Power Channel • I_{OUT} = 80% FSR • I_{OUT} = 25% FSR • I_{OUT} = 10% FSR • I_{OUT} = 5.0% FSR	 -6.0 -6.0 -8.0 -12	 – – – –	 +6.0 +6.0 +8.0 +12	%	(21) (23)
$I_{CSNSMIN}$	Minimum Current Sense Reporting for 17 mΩ • 9.0 V ≤ V_{PWR} ≤ 18 V	–	–	1.0	%	(21) (24)
V_{PWR}	Supply Voltage Feedback Range	V_{PWRMAX}	–	20	V	
ACC V_{PWR}	Supply Feedback Precision • Default • 1 calibration point at 25 °C and V_{PWR}= 12 V, for 7.0 V ≤ V_{PWR} ≤ 20 V • 1 calibration point at 25 °C and V_{PWR}= 12 V, for 6.0 V ≤ V_{PWR} < 7.0 V	 -7.0 -1.5 -2.2	 – – –	 +7.0 +1.5 +2.2	%	(23)
T_{FB}	Temperature Feedback Range	-40	–	150	°C	(22)
V_{FB}	Temperature Feedback Voltage at 25 °C	–	2.31	–	V	
COEF V_{FB}	Temperature Feedback Thermal Coefficient	–	7.72	–	mV/°C	(23)
ACC T_{FB}	Temperature Feedback Voltage Precision • Default • 1 calibration point at 25 °C and V_{PWR} = 7.0 V	 -15 -5.0	 – –	 +15 +5.0	°C	(23)
$t_{CSNS(SET)}$	Current Sense Settling Time • Current Sensing Feedback for I_{OUT} from 75% FSR to 50% FSR • Current Sensing Feedback for I_{OUT} from 10% FSR to 1.0% FSR Temperature and Supply Voltage Feedbacks	 – – –	 – – –	 40 260 10	µs	(22)
$t_{CSNS(VAL)}$	Current Sense Valid Time Current Sensing Feedback • Low/Medium Frequency • High Frequency Temperature and Supply Voltage Feedback	 – – –	 – – –	 100 50 10	µs	(25)
$t_{SYNC\ DEFAULT}$	Current Sense Synchronization Period for PWM Clock Failure	4.8	6.5	8.2	ms	

Table 17. Electrical characteristics (continued)

Characteristics noted under conditions 7.0 V ≤ V_{PWR} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Current sense synchronization CSNS SYNCB						
$R_{CSNS\ SYNC}$	Pull-up Current Sense Synchronization Resistor Range	5.0	–	–	kΩ	
V_{OL}	Current Sense Synchronization Logic Output Low State Level at 1.0 mA	–	–	0.4	V	
$I_{OUT\ MAX}$	Current Sense Synchronization Leakage Current in Tri-state (CSNS SYNC from 0 to 5.5 V)	-1.0	–	+1.0	µA	

Notes

21. Precision either OCLO and ACM setting.
22. Parameter is derived mainly from simulations.
23. Parameter is guaranteed by design characterization. Measurements are taken from a statistically relevant sample size across process variations.
24. Error of ±100% without calibration for all modes and ±50% with 1 calibration point done at 25 °C in ACM mode (+/-70% in non-ACM).
25. Tested at 5.0% of final value @ V_{PWR} = 14 V, current step from 0 A to 2.8 A (or 5.6 A). Parameter guaranteed by design at 1% of final value.

6.2 Power supply functional block description and application information

6.2.1 Introduction

The device is functional when wake = [1] with supply voltages from 5.5 to 40 V (V_{PWR}), but is fully specification compliant only between 7.0 and 18 V. The VPWR pin supplies power to the internal regulator, analog, and logic circuit blocks. The VCC pin (5.0 V typ.) supplies the output register of the Serial Peripheral Interface (SPI) and the OUT6 driver. Consequently, the SPI registers cannot be read without presence of V_{CC}. The employed IC architecture guarantees a low quiescent current in Sleep mode (wake = [0]).

6.2.2 Wake state reporting

The CLK input/output pin is also used to report the wake state of the device to the microcontroller as long as RSTB is logic [0].

When the device is in:

- “wake state” and RSTB is inactive, the CLK pin reports a high signal (logic[1])
- “sleep mode” or the device is wake by the RSTB pin, the CLK is an input pin

6.2.2.1 Electrical characterization

Table 18. Electrical characteristics

Characteristics noted under conditions 7.0 V ≤ V_{PWR} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Clock input/output CLK						
V_{OH}	Logic Output High State Level (CLK) at 1.0 mA	VCC - 0.6	–	–	V	

6.2.3 Supply voltages disconnection

6.2.3.1 Loss of V_{PWR}

In case of V_{PWR} disconnection ($V_{PWR} \leq V_{PWR\ POR}$) the device behavior depends on V_{CC} voltage value:

- $V_{CC} \leq V_{CC\ POR}$: the device enters the power off mode. All outputs are shut off immediately. All registers and faults are cleared
- $V_{CC} > V_{CC\ POR}$: all registers and faults are maintained. OUT1:5 are shut off immediately. The ON/OFF state of OUT6 depends on the current SPI configuration. SPI reporting is available when V_{CC} remains within its operating voltage range (4.5 to 5.5 V)

The wake-up event is not reported to the CLK pin. The clamping structures (supply clamp, negative output clamp) are available to protect the device. No current is conducted from V_{CC} to V_{PWR}. An external current path shall be available to drain the energy from an inductive load, in case a supply disconnection occurs when an output is ON.

6.2.3.2 Loss of V_{CC}

In case of a V_{CC} disconnection, the device behavior depends on V_{PWR} voltage:

- $V_{PWR} \leq V_{PWR\ POR}$: the device enters the power off mode. All outputs are shut off immediately. All registers and faults are cleared
- $V_{PWR} > V_{PWR\ POR}$: the SPI is not available. Therefore, the device enters WD timeout

The clamping structures (supply clamp, negative output clamp) are available to protect the device. No current is conducted from V_{PWR} to V_{CC}.

6.2.3.3 Loss of device GND

During loss of ground, the device cannot drive the loads, therefore the OUT1:OUT5 outputs are switched off and the OUT6 voltage is pulled up. The device shall not be damaged by this failure condition. For protection of the digital inputs series resistors (1.0 kΩ typ) can be provided externally in order to limit the current to I_{CL}.

6.2.3.4 Electrical characterization

Table 19. Electrical characteristics

Characteristics noted under conditions 7.0 V ≤ V_{PWR} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Supply VPWR						
$V_{PWR\ POR}$	Supply Power On Reset	2.0	3.0	4.0	V	
VCC						
$V_{CC\ POR}$	VCC Power On Reset	2.0	3.0	4.0	V	
Ground GND						
$V_{GND\ SHIFT}$	Maximum Ground Shift between GND Pin and Load Grounds	-1.5	–	+1.5	V	

6.3 Communication interface and device control functional block description and application information

6.3.1 Introduction

In Normal mode, the power output channels are controlled by the embedded PWM module, which is configured by the SPI register settings. For bidirectional SPI communication, V_{CC} has to be in the authorized range. Failure diagnostics and configuration are also performed through the SPI port. The reported failure types are: open load, short-circuit to supply, severe short-circuit to ground, overcurrent, overtemperature, clock fail, and under and overvoltage. For direct input control, the device shall be in Fail-safe mode. V_{CC} is not required and this mode can be forced by the LIMP input pin.

6.3.2 Fail mode input (LIMP)

The Fail mode of the component can be activated by LIMP direct input. The Fail mode is activated when the input is logic [1]. In Fail mode, the channel power outputs are controlled by the corresponding inputs. Even though the input thresholds are logic level compatible, the input structure of the pins are able to withstand supply voltage level (max. 40 V) without damage. External current limit resistors (i.e. 1.0 kΩ:10 kΩ) can be used to handle reverse current conditions. The direct inputs have an integrated pull-down resistor. The LIMP input has an integrated pull-down resistor. The status of the LIMP input can be monitored by the LIMP IN bit inside the device status register #7.

6.3.2.1 Electrical characterization

Table 20. Electrical characteristics

Characteristics noted under conditions 4.5 V ≤ V_{PWR} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Fail mode input LIMP						
V_{IH}	Logic Input High State Level	3.5	–	–	V	
V_{IL}	Logic Input Low State Level	–	–	1.5	V	
I_{IN}	Logic Input Leakage Current in Inactive State (LIMP = [0])	-0.5	–	+0.5	µA	
R_{PULL}	Logic Input Pull-down Resistor	25	–	100	kΩ	
C_{IN}	Logic Input Capacitance	–	–	20	pF	(26)
Direct inputs IN1:IN4						
V_{IH}	Logic Input High State Level	3.5	–	–	V	
$V_{IH(WAKE)}$	Logic Input High State Level for wake-up	3.75	–	–	V	
V_{IL}	Logic Input Low State Level	–	–	1.5	V	
I_{IN}	Logic Input Leakage Current in Inactive State (forced to [0])	-0.5	–	+0.5	µA	
R_{PULL}	Logic Input Pull-down Resistor	25	–	100	kΩ	
C_{IN}	Logic Input Capacitance	–	–	20	pF	(26)

Notes

26. Parameter is derived mainly from simulations.

6.3.3 MCU communication interface protections

6.3.3.1 Loss of communication interface

If a SPI communication error occurs, the device is switched into Fail mode. A SPI communication fault is detected if:

- the WD bit is not toggled with each SPI message or
- WD timeout is reached or
- protocol length error (modulo 16 check)

The SI stuck to static levels during CSB period and VCC fail (SPI not functional) are indirectly detected by a WD toggle error. The SPI communication error is reported in:

- SPI failure flag (SPIF) inside the device status register #7 in the next SPI communication

As long as the device is in Fail mode, the SPIF bit retains its state. The SPIF bit is delatched during the transition from fail-to-normal modes.

6.3.3.2 Logic I/O plausibility check

The logic and signal I/O are protected against fatal mistreatment by a signal plausibility check, according following table:

I/O	Signal check strategy
IN1 ~ IN4	frequency above limit (low pass filter)
LIMP	frequency above limit (low pass filter)
RSTB	frequency above limit (low pass filter)
CLK	frequency above limit (low pass filter)

The LIMP and IN1:IN4 have an input symmetrically deglitch time t_{IN_DGL} = 200 µs (typ). If the LIMP input is set to logic [1] for a delay longer than 200 µs typ, the device is switched into Fail mode (internal signal called iLIMP).

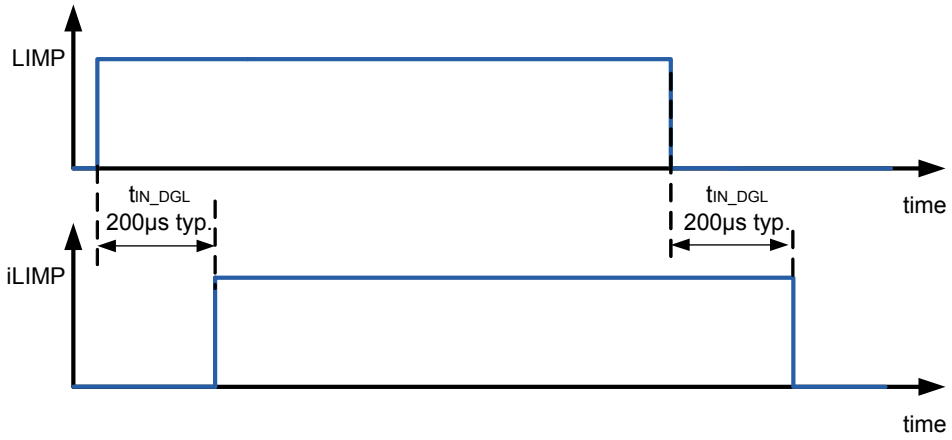


Figure 35. LIMP and iLIMP signal

If the INx input is set to logic [1] for a delay longer than 200 µs (typ.), the corresponding channel is controlled by the direct signal (internal signal called iINx).

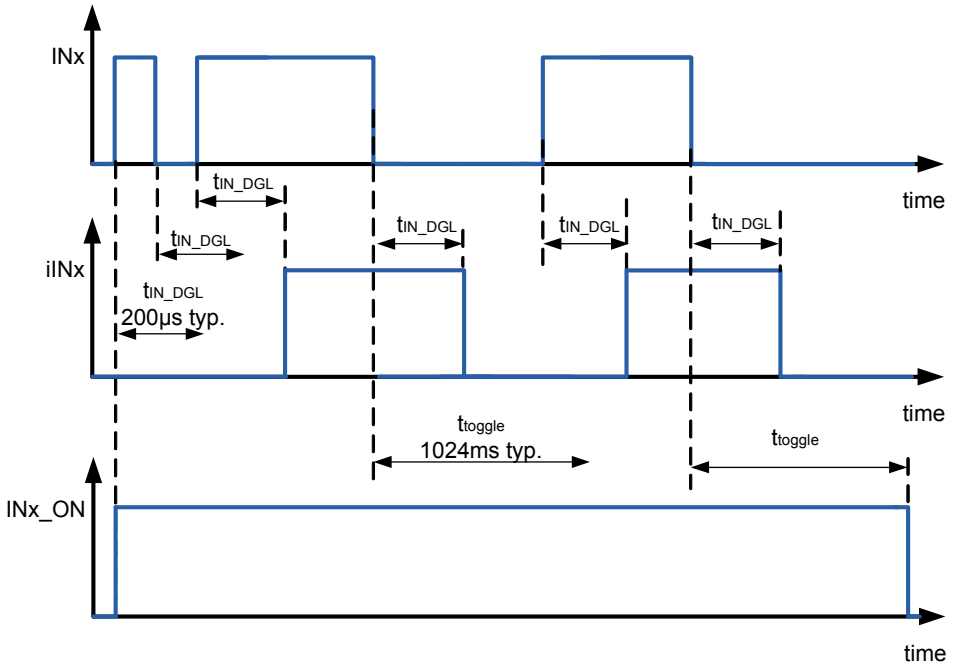


Figure 36. IN, iIN and IN_ON signal

The RSTB has an input deglitch time t_{RST_DGL} = 10 µs (typ.) for the falling edge only. The CLK has an input symmetrically deglitch time t_{CLK_DGL} = 2.0 µs (typ). Due to the input deglitcher (at the CLK input) a very high input frequency leads to a clock fail detection. The CLK fail detection (clock input frequency detection $f_{CLK\ LOW}$) is started immediately with the positive edge of RSTB signal. If the CLK frequency is below $f_{CLK\ LOW}$ limit, the output state depends on the corresponding CHx signal. As soon as the CLK signal is valid, the output duty cycle depends on the corresponding SPI configuration. To delatch the CLK fail diagnosis:

- the clock failure condition must be removed
- a read command of the quick status register #1 must be performed

6.3.3.3 Electrical characterization

Table 21. Electrical characteristics

Characteristics noted under conditions 7.0 V ≤ V_{PWR} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Logic I/O LIMP IN1:IN4 CLK						
t_{WD}	SPI Watchdog Timeout • WD SEL = 0 • WD SEL = 1	 24 96	 32 128	 40 160	ms	
t_{TOGGLE}	Input Toggle Time for IN1:IN4	768	1024	1280	ms	
t_{DGL}	Input Deglitching Time • LIMP and IN1:IN4 • CLK • RST\	 150 1.5 7.5	 200 2.0 10	 250 2.5 12.5	µs	
$f_{CLOCK\ LOW}$	Clock Low Frequency Detection	50	100	200	Hz	

6.3.4 External smart power control (OUT6)

The device provides a control output to drive an external smart power device in Normal mode only. The control is according to the channel 6 settings in the SPI input data register.

- The protection and current feedback of the external SmartMOS device are under the responsibility of the microcontroller
- The output delivers a 5.0 V CMOS logic signal from V_{CC}

The output is protected against overvoltage. An external current limit resistor (i.e. 1.0 kΩ:10 kΩ) shall be used to handle negative output voltage conditions. The output has an integrated pull-down resistor to provide a stable OFF condition in Sleep mode and Fail mode. In case of a ground disconnection, the OUT6 voltage is pulled up. External components are mandatory to define the state of external smart power device and to limit possible reverse OUT6 current (i.e. resistor in series).

6.3.4.1 Electrical characterization

Table 22. Electrical characteristics

Characteristics noted under conditions 7.0 V ≤ V_{PWR} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
External smart power output OUT6						
$t_{OUT6\ RISE}$	OUT6 Rising Edge for 100 pF capacitive load	–	–	5.0	µs	
$R_{OUT6\ DWN}$	OUT6 Pull-down Resistor	5.0	10	20	kΩ	
V_{OH}	Logic Output High State Level (OUT6)	VCC - 0.6	–	–	V	
V_{OL}	Logic Output Low State Level (OUT6)	–	–	0.6	V	

7 Typical applications

7.1 Introduction

The 12XSF is the latest achievement in DC motors and lighting drivers.

7.1.1 Application diagram

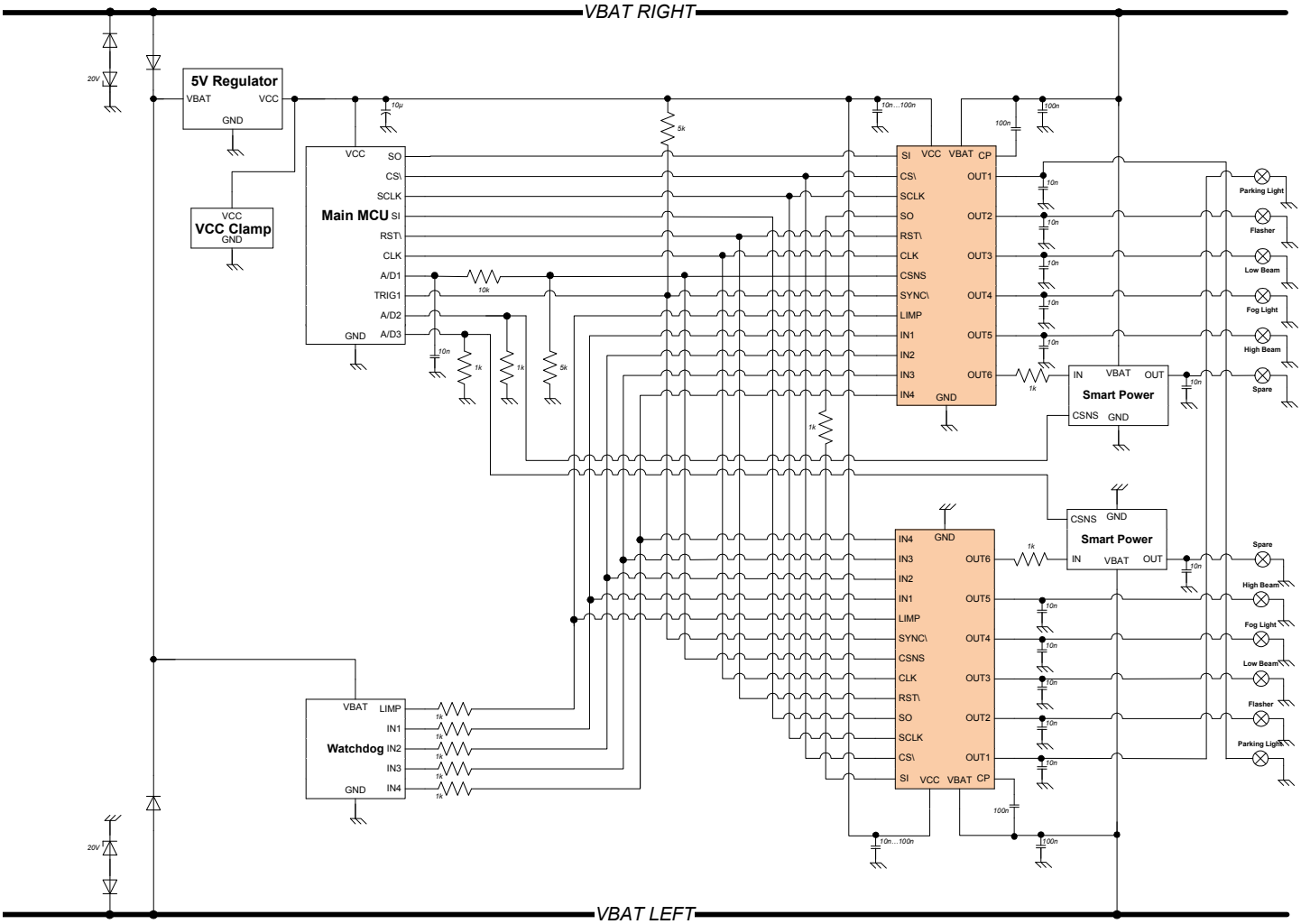


Figure 37. Typical front lighting application

7.1.2 Application instructions

7.1.3 Bill of materials

Table 23. 12XSF Bill of materials [27]

Signal	Location	Mission	Value
V_{PWR}	close to 12XSF eXtreme Switch	improve emission and immunity performances	100 nF (X7R 50 V)
CP	close to 12XSF eXtreme Switch	charge pump tank capacitor	100 nF (X7R 50 V)
V_{CC}	close to 12XSF eXtreme Switch	improve emission and immunity performances	10 to 100 nF (X7R 16 V)
OUT1:OUT4/5	close to output connector	sustain ESG gun and fast transient pulses improve emission and immunity performances	10 to 22 nF (X7R 50 V)
CSNS	close to MCU	output current sensing	5.0 k (±1.0%)
CSNS	close to MCU	low pass filter removing noise	10 kΩ (±1.0%) and 10 nF (X7R 16 V)
CSNS SYNCB	N/A	pull-up resistor for the synchronization of A/D conversion	5.0 k (±1.0%)
IN1:IN4	N/A	sustain high-voltage	1.0 kΩ (±1.0%)
OUT6	N/A	sustain reverse polarity	1.0 kΩ (±1.0%)
To Increase Fast Transient Pulses Robustness			
V_{PWR}	close to connector	sustain pulse #1 in case of LED loads or without loads	20 V zener diode and diode in series per supply line
V_{PWR}	close to 12XSF eXtreme Switch	sustain pulse #2 without loads	additional 10 µF (X7R 50 V)
To Sustain 5.0 V Voltage Regulator Failure Mode			
V_{CC}	close to 5.0 V voltage regulator	prevent high-voltage application on the MCU	5.0 V zener diode and a bipolar transistor

Notes

27. NXP does not assume liability, endorse, or warrant components from external manufacturers that are referenced in circuit drawings or tables. While NXP offers component recommendations in this configuration, it is the customer's responsibility to validate their application.

7.2 EMC and EMI considerations

7.2.1 EMC/EMI tests

This paragraph gives EMC/EMI performances. Further generic design recommendations can be found on the NXP website www.nxp.com.

Table 24. EMC/EMI performances

Test	Signals	Conditions	Standard	Criteria
Conducted Emission	VPWR	outputs off outputs on in PWM	CISPR25	Class 5
	150 Ω Method Global pins: V_{PWR} and OUT1:OUT5 Local pins: V_{CC}, CP, and CSNS		IEC 61967-4	150 Ω Method Global pins: 12-K level for VPWR pin - 11-L for OUT1: 5 pins Local pins: 10-J level
Conducted Immunity	Global pins: V_{PWR} and OUT1:OUT5 Local pins: V_{CC}		IEC 62132-4	Class A related to the outputs state and the analog diagnostics (±20%) 30 dBm for Global pins 12 dBm for Local pins

7.2.2 Fast transient pulse tests

This paragraph gives the device performances.against fast transient disturbances.

Table 25. Fast transient capability on VPWR

Test	Conditions	Standard	Criteria
Pulse 1	outputs loaded with lamps other cases with external transient voltage suppressor	ISO 7637-2 (for automotive)	Class A
Pulse 2a			
Pulse 3a/3b	outputs loaded outputs unloaded		
Pulse 5b (40 V)			

7.3 Robustness considerations

The short-circuit protections embedded in 12XSF are preferred to conventional current limitations, to minimize the thermal overstress within the device in case of an overload condition. The junction temperature elevation is drastically reduced to a value which does not affect the device's reliability. Moreover, the availability of the lighting is guaranteed in fail mode by the unlimited autorestart feature.

The chapter 12 of AEC-Q100 specification published by the Automotive Electronics Council presents turn-on into short-circuit condition. It is not enough, because the short-circuit event can also occur in on-state. The test plan at T_A = 70 °C is presented in Table 26. The tests are performed on 30 parts from three engineering lots (total 90 pieces).

Table 26. 12XSF repetitive short-circuit test results at T_A = 70 °C

Short-circuit case	Supply voltage	Supply line	Load line	7.0 mΩ output cycle without failure	17 mΩ output cycle without failure
Turn-on into short-circuit condition	16 V	0.3 m/2.5 mm²	5.0 m/1.0 mm²	500 k	500 k
			0.3 m/1.0 mm²	500 k	500 k
		5.0 m/2.5 mm²		500 k	500 k
Short-circuit in On-state (28)	14 V	0.3 m/2.5 mm²	5.0 m/1.0 mm²	500 k	500 k
			0.3 m/1.0 mm²	500 k	500 k
		5.0 m/2.5 mm²		500 k	500 k

Table 26. 12XSF repetitive short-circuit test results at T_A = 70 °C

Short-circuit case	Supply voltage	Supply line	Load line	7.0 mΩ output cycle without failure	17 mΩ output cycle without failure
On-state overload 95% of min OCHI1/2/3 levels	16 V	0.3 m/6.0 mm²	0.3 m/6.0 mm²	500 k	500 k

Notes

28. The channel was loaded in the on-state with 100 mA.

7.4 PCB layout recommendations

This new generation of high-side switch products family facilitates ECU design thanks to compatible MCU software and PCB foot print for each device variant. The PCB Copper layer is similar for all devices in the 12XSF family, only the solder Stencil opening is different. Figure 38 shows superposition of SOIC54 (in black) and SOIC32 packages (in blue). To keep pin-to-pin compatibility in the same PCB footprint, pin 1 of the SOIC32 package must be located at pin 3 of the SOIC54 package.

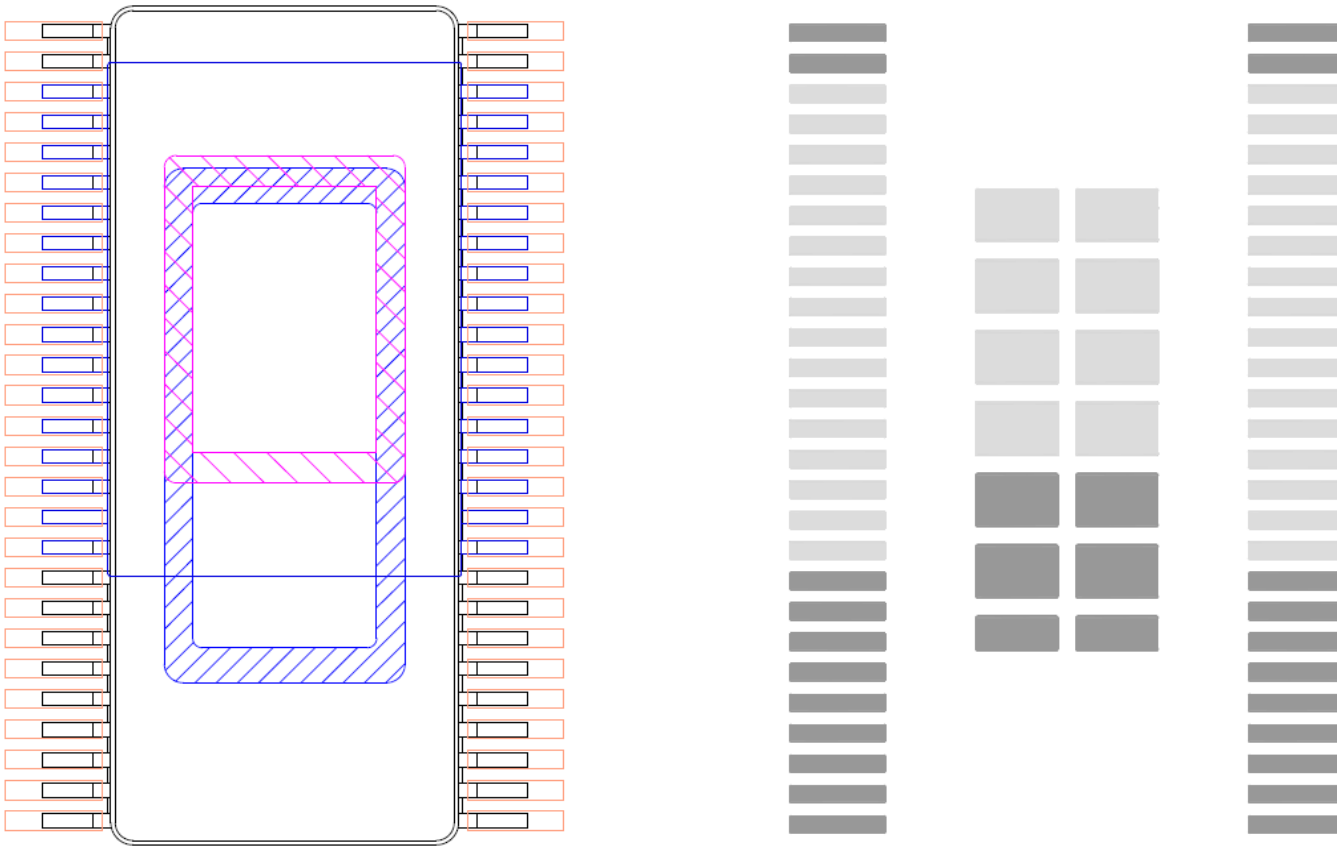


Figure 38. PCB copper layer and solder stencil opening recommendations

7.5 Thermal information

This section provides thermal information.

7.5.1 Thermal transient

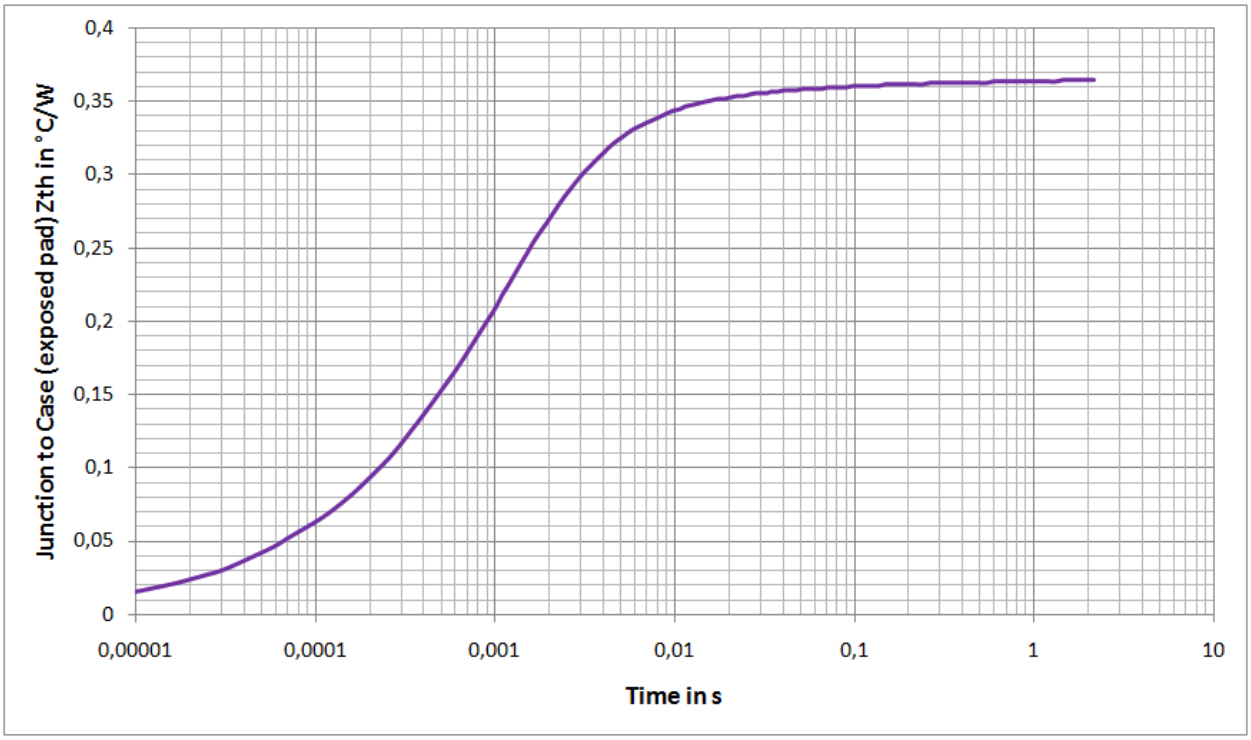


Figure 39. Transient thermal response curve

7.5.2 R/C thermal model

Contact the local Field Application Engineer (email: support@nxp.com).

8 Packaging

8.1 Marking information

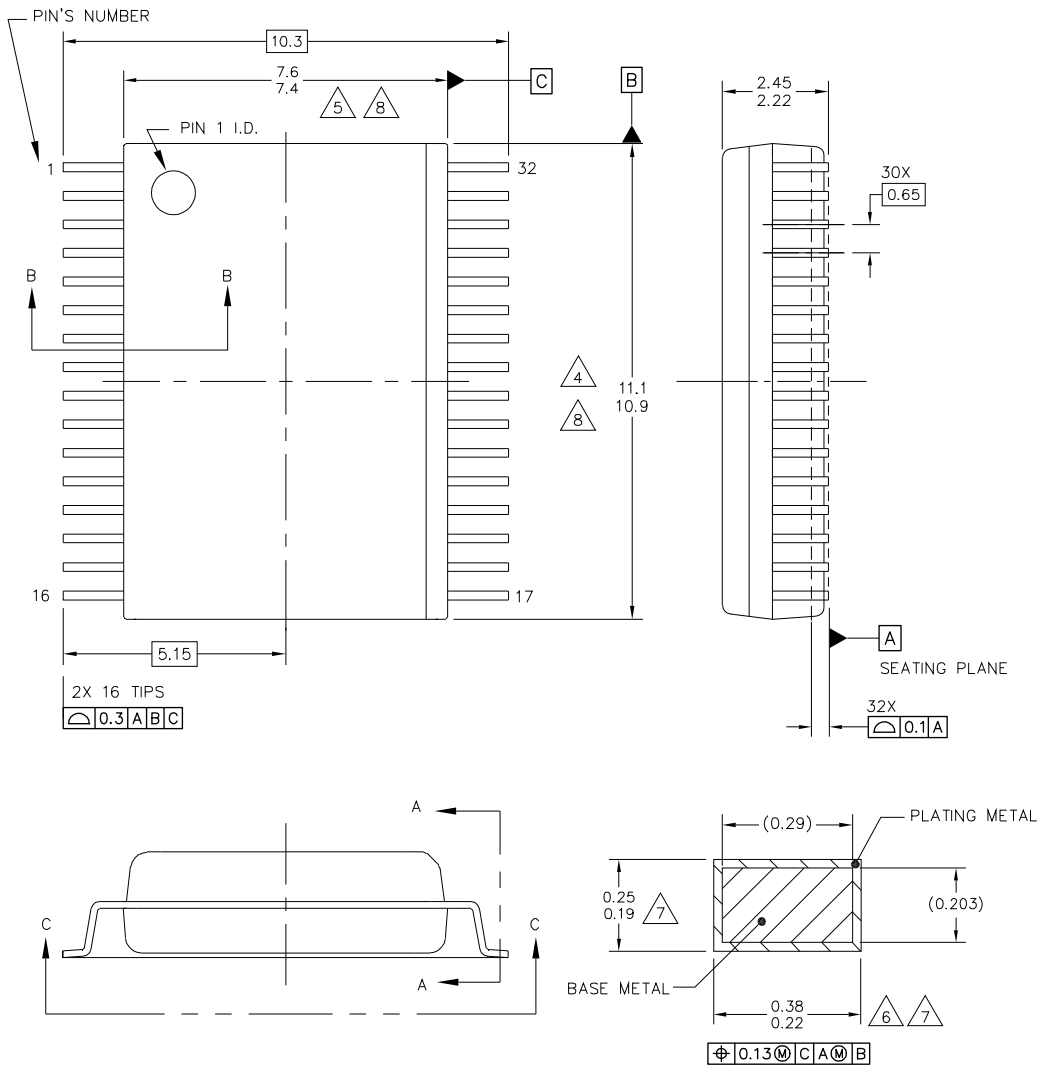
Device markings indicate information on the week and year of manufacturing. The date is coded with the last four characters of the nine character build information code (e.g. “CTKAH1229”). The date is coded as four numerical digits where the first two digits indicate the year and the last two digits indicate the week. For instance, the date code “1229” indicates the 29th week of the year 2012.

8.2 Package mechanical dimensions

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.nxp.com and perform a keyword search for the drawing’s document number.

Table 27. Package outline

Package	Suffix	Package outline drawing number
32-Pin SOICEP	EK	98ASA00368D
54-Pin SOICEP	EK	98ASA00367D



SECTION A–A

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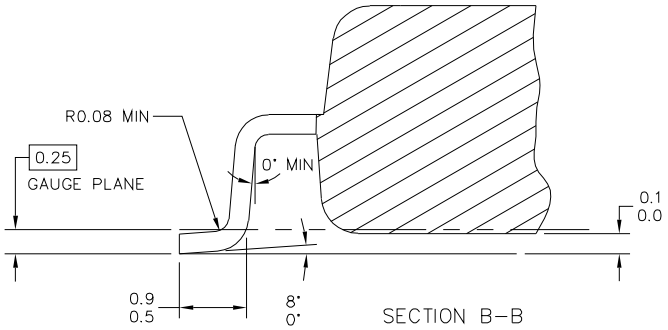
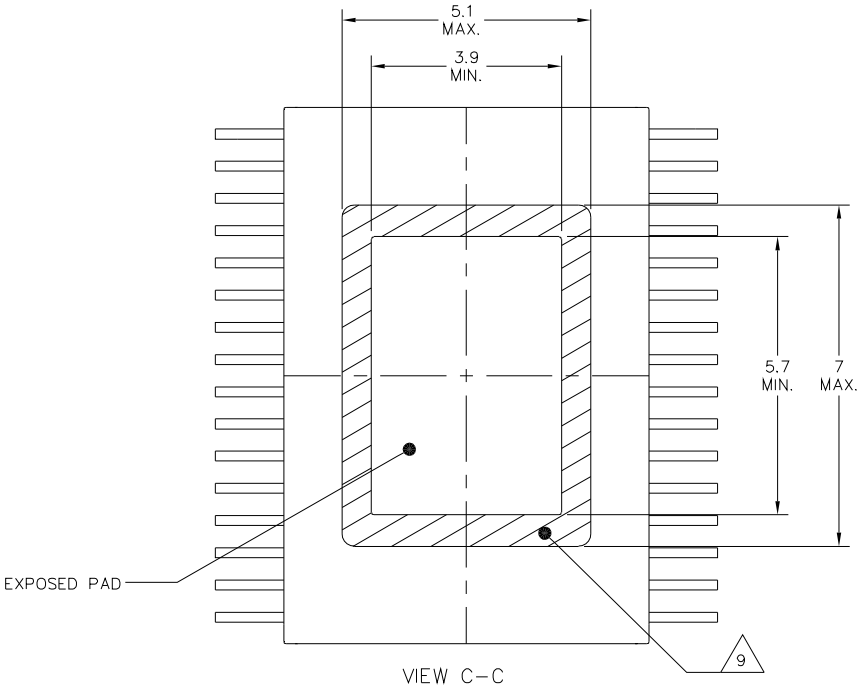
TITLE: SOIC W/B, 32 TERMINAL, 0.65 PITCH, 6.4 X 4.5 EXPOSED PAD	DOCUMENT NO: 98ASA00368D	REV: A
	STANDARD: NON–JEDEC	
	SOT1746–2	07 JAN 2016





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TITLE: SOIC W/B, 32 TERMINAL, 0.65 PITCH, 6.4 X 4.5 EXPOSED PAD	DOCUMENT NO: 98ASA00368D	REV: A
	STANDARD: NON–JEDEC	
	SOT1746–2	07 JAN 2016

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS B AND C TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.

4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.

5. THIS DIMENSION DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.

6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.4 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT LESS THAN 0.07 mm.

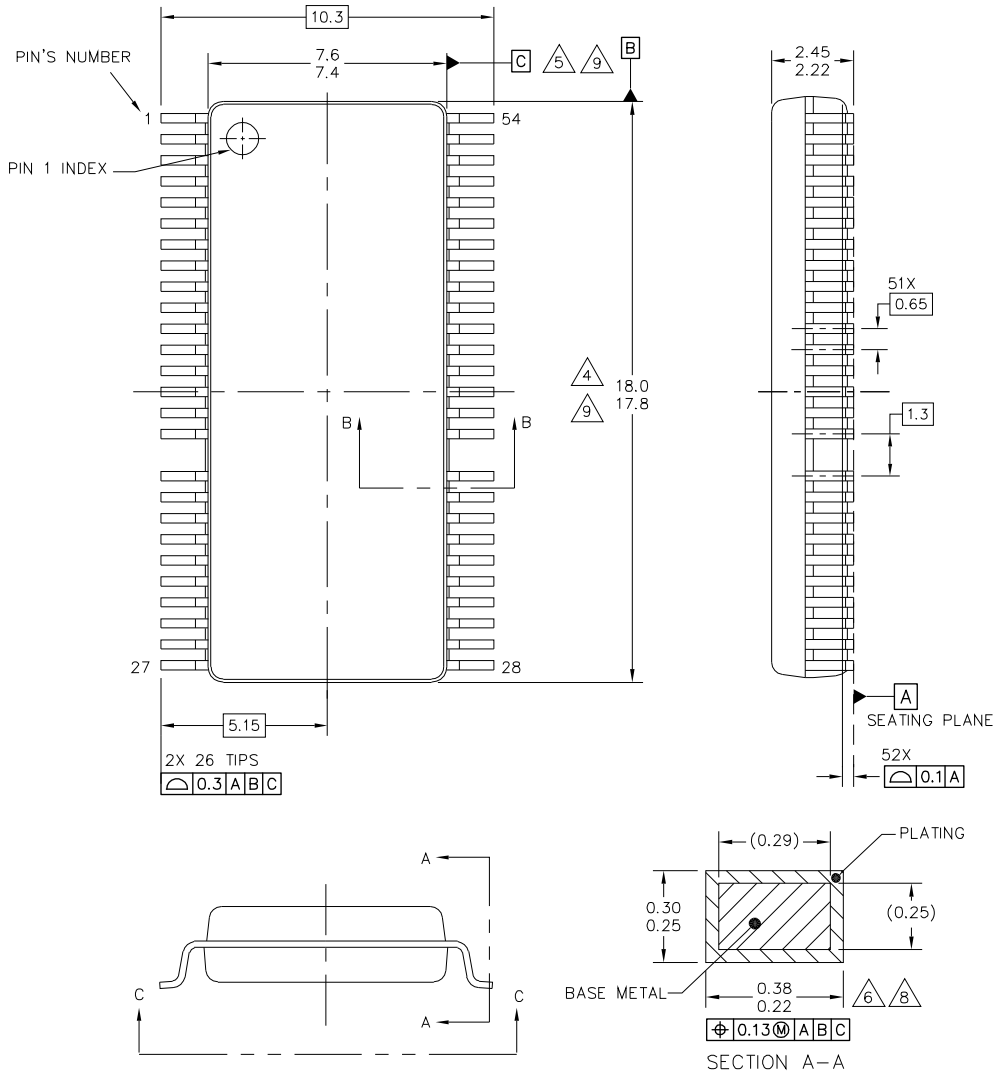
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.3 mm FROM THE LEAD TIP.

8. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER–LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.

9. HATCHED AREA TO BE KEEP–OUT ZONE FOR PCB ROUTING.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE: SOIC W/B, 32 TERMINAL, 0.65 PITCH, 6.4 X 4.5 EXPOSED PAD	DOCUMENT NO: 98ASA00368D REV: A
	STANDARD: NON–JEDEC
	SOT1746–2 07 JAN 2016



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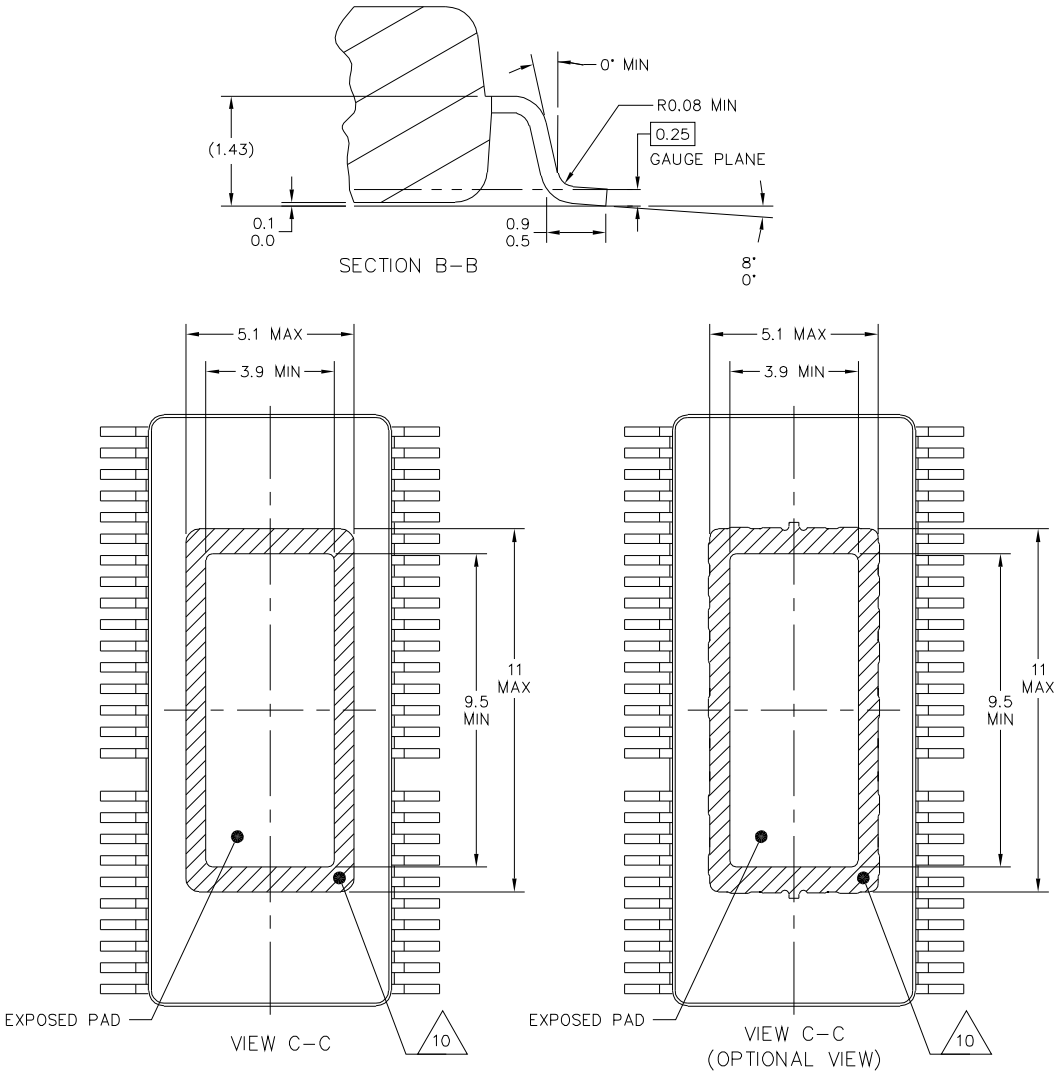
TITLE: SOIC W/B, TOOTH GAP DESIGN, 54 TERMINAL, 0.65 PITCH, 4.5 X 10.3 EXPOSED PAD	DOCUMENT NO: 98ASA00367D	REV: B
	STANDARD: NON–JEDEC	
	SOT1747–2	07 JAN 2016



MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: SOIC W/B, TOOTH GAP DESIGN, 54 TERMINAL, 0.65 PITCH, 4.5 X 10.3 EXPOSED PAD	DOCUMENT NO: 98ASA00367D REV: B
	STANDARD: NON–JEDEC
	SOT1747–2 07 JAN 2016

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS B AND C TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.3 mm FROM THE LEAD TIP.
9. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER–LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
10. HATCHED AREA TO BE KEEP OUT ZONE FOR PCB ROUTING.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE: SOIC W/B, TOOTH GAP DESIGN, 54 TERMINAL, 0.65 PITCH, 4.5 X 10.3 EXPOSED PAD	DOCUMENT NO: 98ASA00367D REV: B
	STANDARD: NON–JEDEC
	SOT1747–2 07 JAN 2016

9 Revision history

Revision	Date	Description of changes
1.0	1/2015	• Initial release
	8/2016	• Updated to NXP document form and style

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