TVS Diodes

Transient Voltage Suppressor Diodes

ESD102-U2-099EL

2-Line Ultra-low Capacitance ESD / Transient Protection Diodes

ESD102-U2-099EL

Data Sheet

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Final

Power Management & Multimarket

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Page or Item	**Subjects (major changes since previous revision)**
Revision 1.1, 2013-05-15	

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1 2-Line Ultra-low Capacitance ESD / Transient Protection Diodes

1.1 Features

- ESD / transient protection of high speed data lines exceeding:
  - **IEC61000-4-2 (ESD): ±20 kV (air / contact)**
  - **IEC61000-4-4 (EFT): ±2.5 kV / 50 A (5/50ns)**
  - **IEC61000-4-5 (Surge): ±3 A (8/20µs)**
- Maximum working voltage: V_{RWM} **= 3.3 V**
- Ultra low capacitance C_L **= 0.4 pF** (typ.) I/O to GND, **0.2 pF** (typ.) I/O to I/O
- Very low clamping voltage: V_{CL} **= 8 V** (typ.) at I_{PP} **= 16 A**
- Very low dynamic resistance: R_{DYN} **= 0.19 Ω** (typ.)
- TSLP-4-10 package with pad pitch 0.4 mm, smallest 2 line package
- Pb-free and halogen free package (RoHS compliant)

1.2 Application Examples

- USB 3.0, 10/100/1000 Ethernet, Firewire
- DVI, HDMI, S-ATA, DisplayPort
- Mobile HDMI Link, MDDI, MIPI, etc.

1.3 Product Description

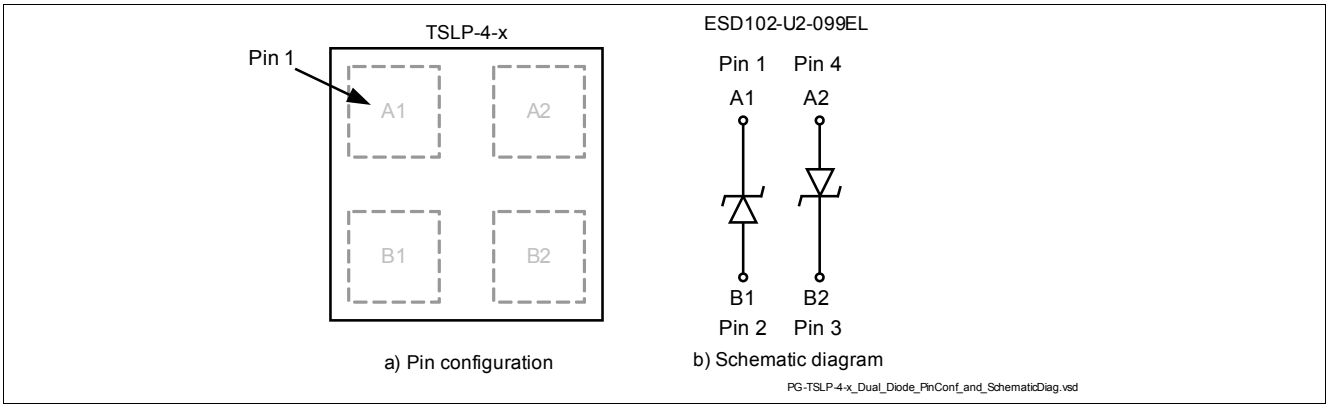

Figure 1 Pin Configuration and Schematic Diagram

Table 1 Ordering Information

Type	Package	Configuration	Marking code
ESD102-U2-099EL	TSLP-4-10	2 Lines anti-parallel, uni-directional	B

2 Characteristics

Table 2 Maximum Rating at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
ESD air / contact discharge[1)]	V_{ESD}	-20	–	20	kV
Peak pulse current (t_p = 8/20 µs)[2)]	I_{PP}	-3	–	3	A
Operating temperature	T_{OP}	-40	–	125	°C
Storage temperature	T_{stg}	-65	–	150	°C

1) V_{ESD} according to IEC61000-4-2

2) I_{PP} according to IEC61000-4-5

2.1 Electrical Characteristics at T_A = 25 °C, unless otherwise specified

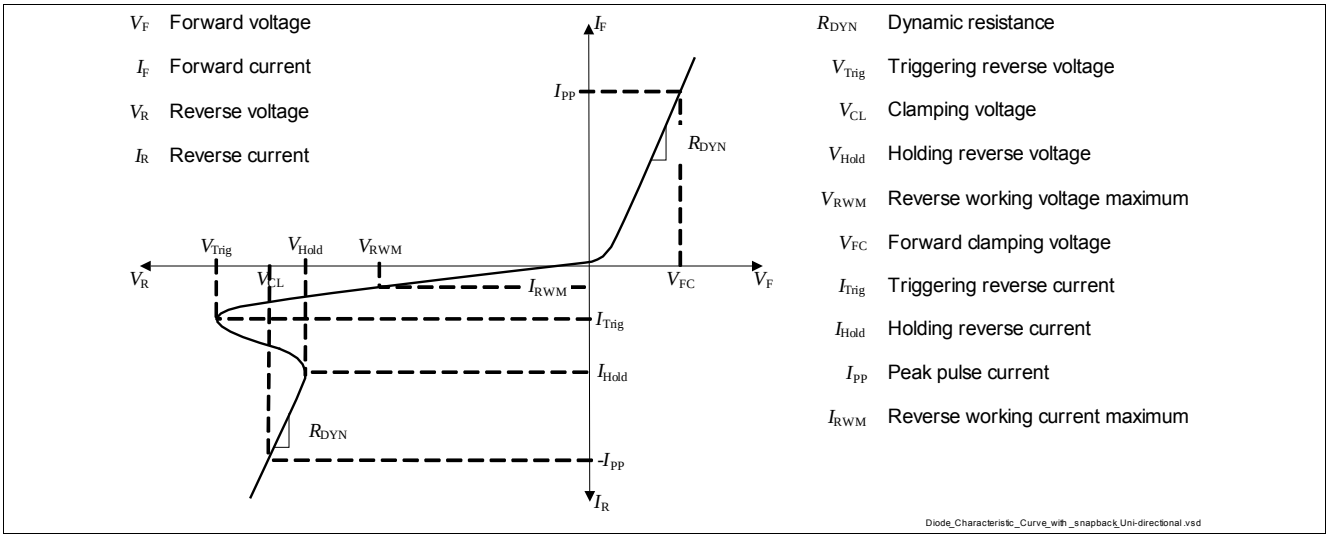

Figure 2 Definitions of electrical characteristics[1]

Table 3 DC Characteristics at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Reverse working voltage	V_{RWM}	–	–	3.3	V	I/O to *GND*
Reverse current	I_R	–	1	50	nA	V_R = 3.3 V, I/O to *GND*

Table 4 RF Characteristics at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line capacitance[1]	C_L	–	0.4	0.65	pF	V_R = 0 V, f = 1 MHz, I/O to GND
		–	0.2	0.35	pF	V_R = 0 V, f = 1 MHz, I/O to I/O
Channel capacitance matching between I/O to GND	$\Delta C_{i/o\text{-}GND}$	–	0.01	–	pF	V_R = 0 V, f = 1 MHz, I/O to GND
Channel capacitance matching between I/O to I/O	$\Delta C_{i/o\text{-}i/o}$	–	0.005	–	pF	V_R = 0 V, f = 1 MHz, I/O to I/O

1) Total capacitance line to ground

Table 5 ESD Characteristics at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clamping voltage[1] [2]	V_{CL}	–	8	–	V	I_{TLP} = 16 A, from I/O to GND
		–	11	–	V	I_{TLP} = 30 A, from I/O to GND
Forward clamping voltage[1] [2]	V_{FC}	–	6	–	V	I_{TLP} = 16 A, from GND to I/O
		–	9	–	V	I_{TLP} = 30 A, from GND to I/O
Dynamic resistance[1] [2]	R_{DYN}	–	0.19	–	Ω	I/O to GND
		–	0.23	–	Ω	GND to I/O

1) Please refer to Application Note AN210. TLP parameter: Z_0 = 50 Ω , t_p = 100ns, t_r = 300ps, averaging window: t_1 = 30 ns to t_2 = 60 ns, extraction of dynamic resistance using least squares fit of TLP characteristic between I_{TLP1} = 10 A and I_{TLP2} = 40 A.

3 Typical Characteristics at T_A = 25 °C, unless otherwise specified

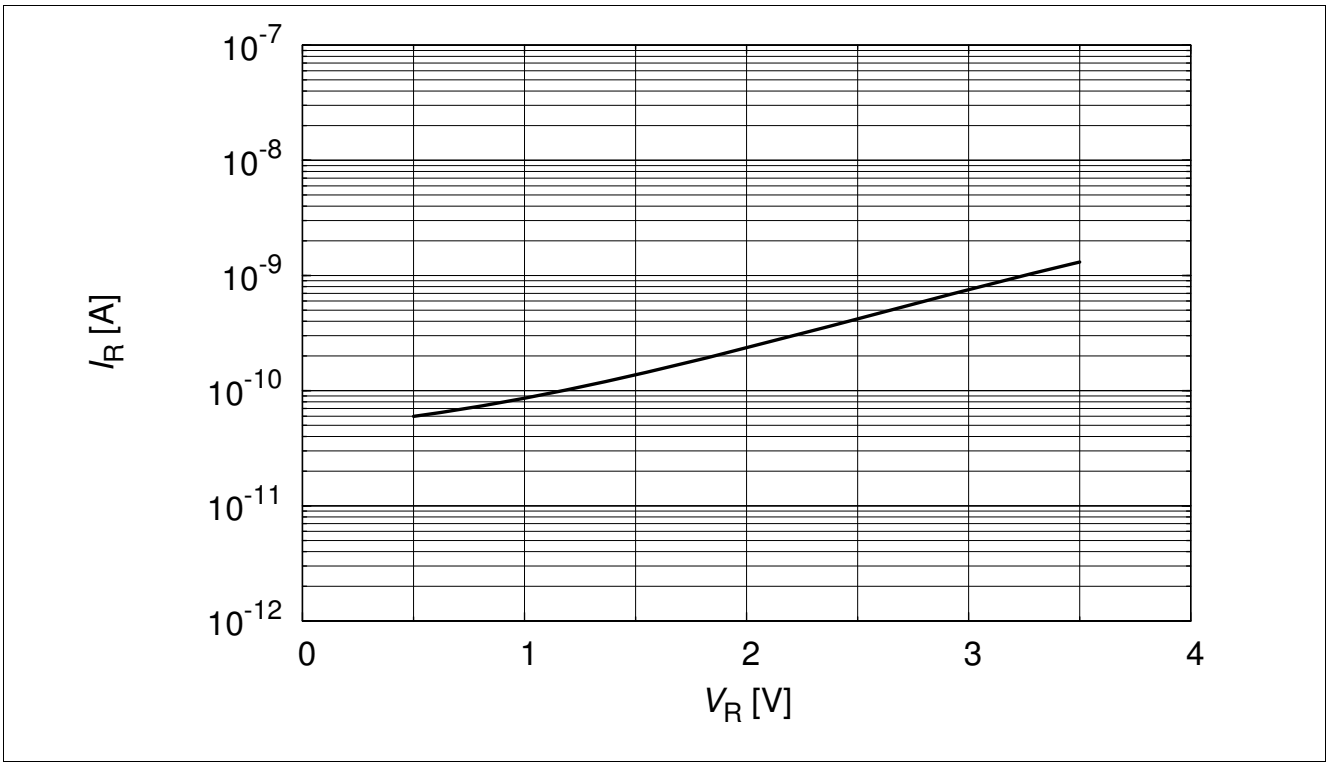

Figure 3 Reverse current, $I_R = (V_R)$

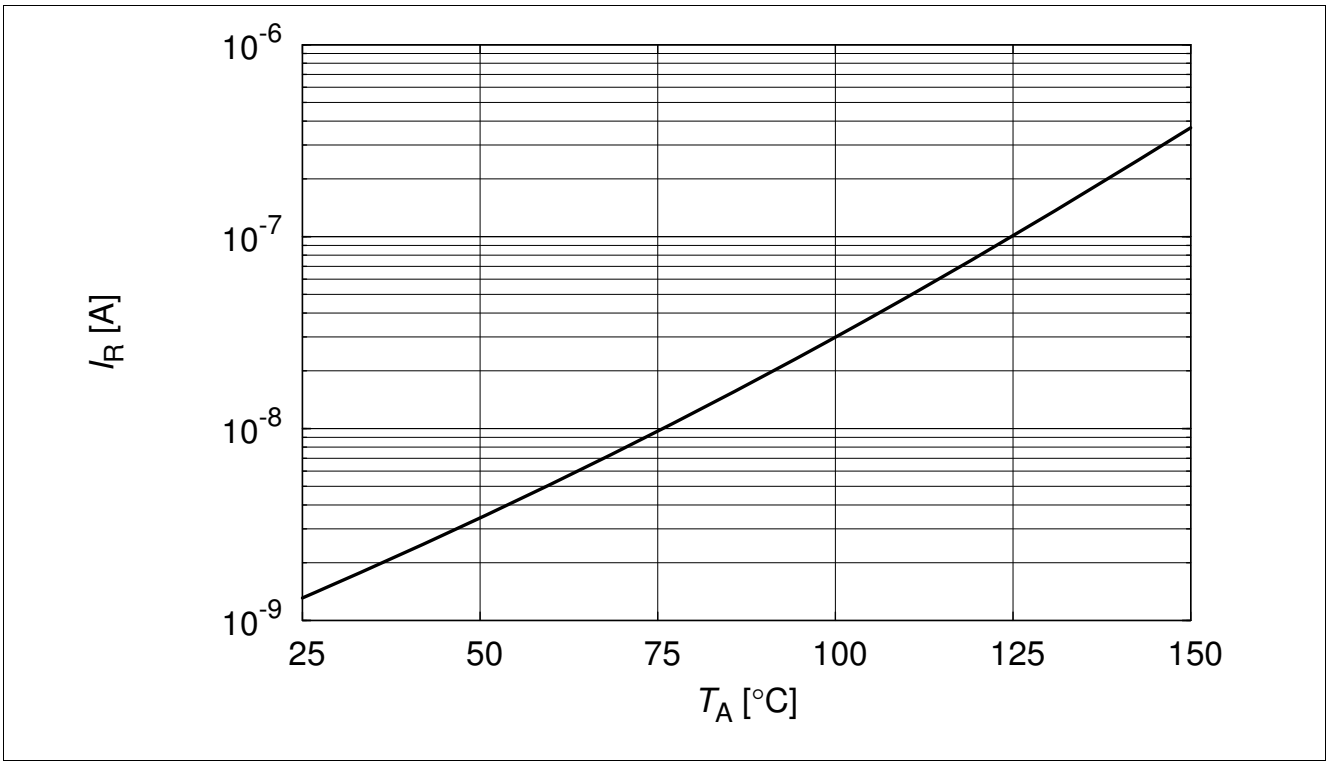

Figure 4 Reverse current: $I_R = f(T_A)$, V_R = 3.3 V

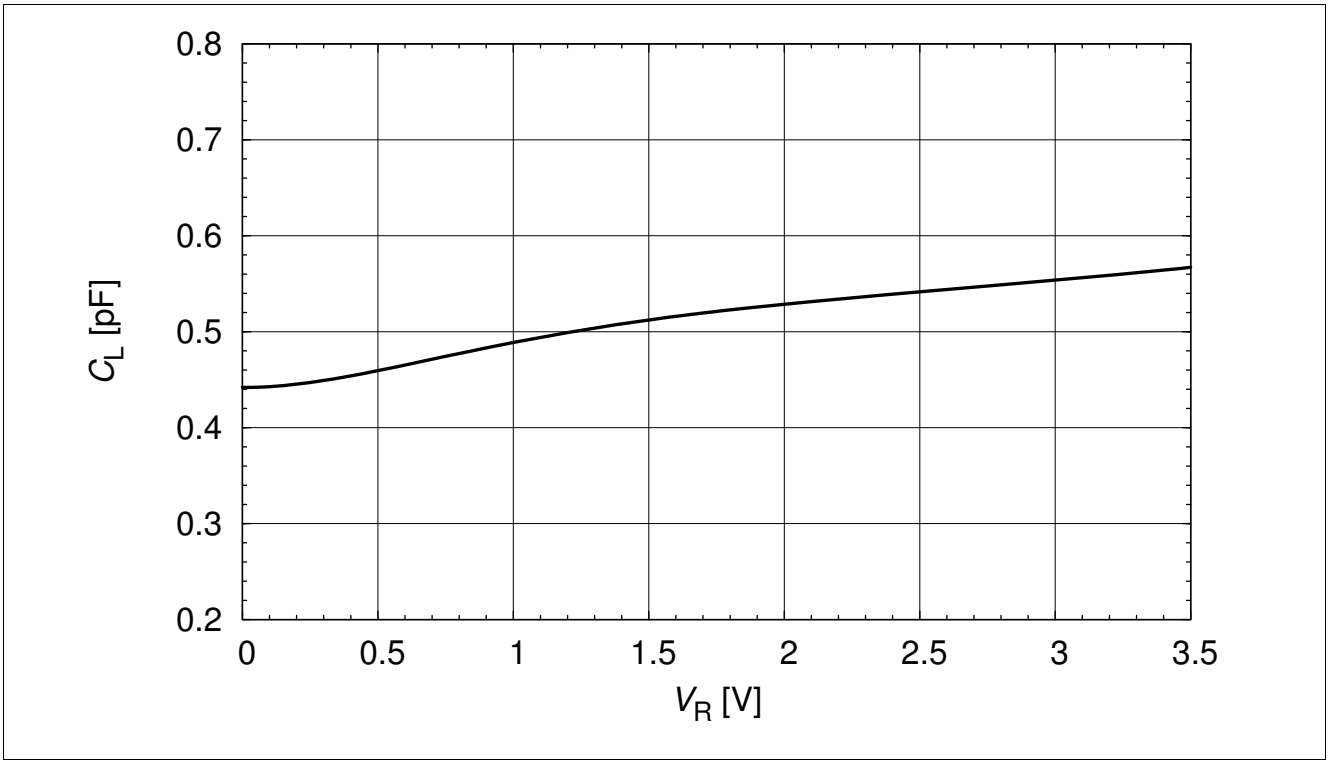

Figure 5 Line capacitance: $C_L = f(V_R)$, f = 1MHz, from I/O to GND

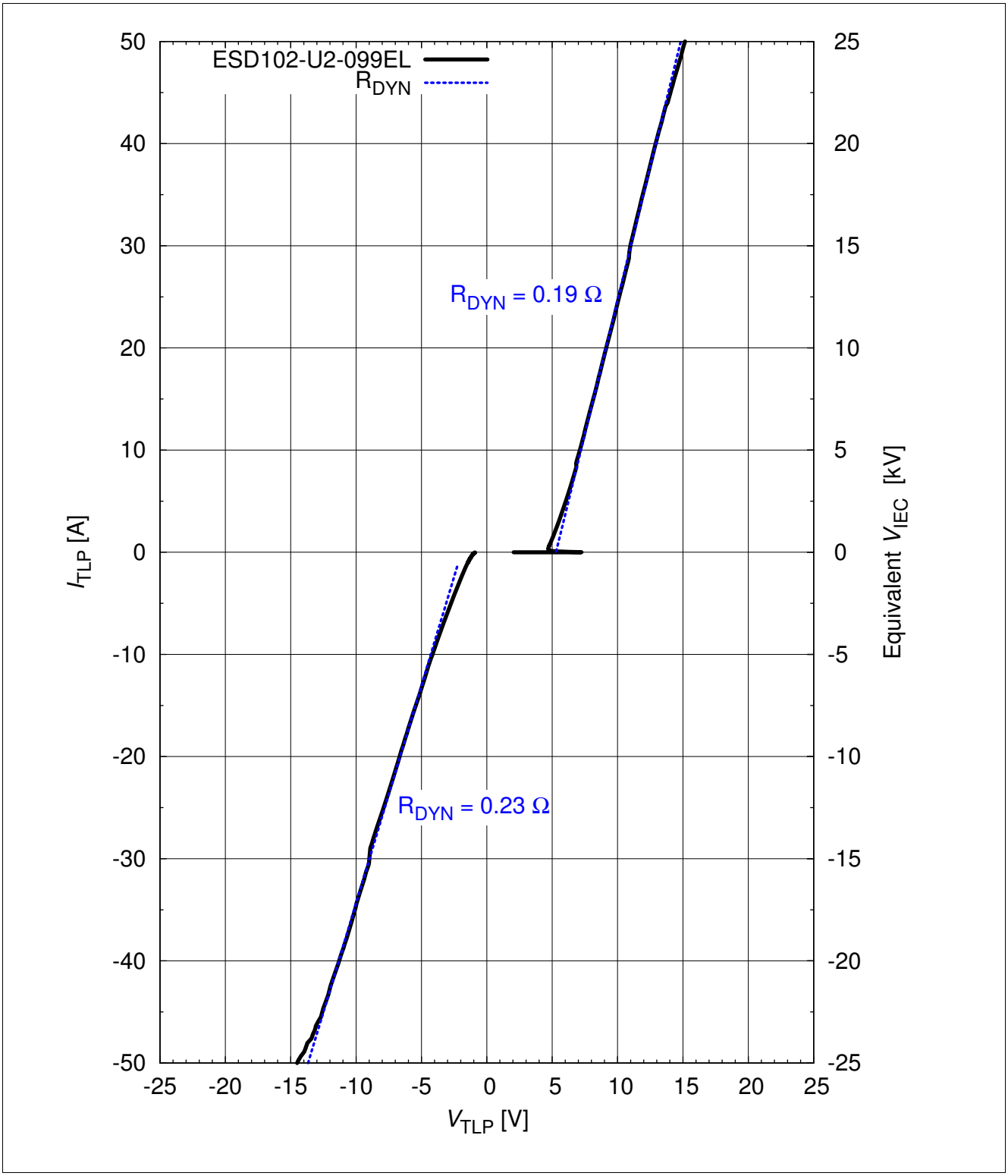

Figure 6 Clamping voltage $V_{TLP} = f(I_{TLP})$[2]

Note: TLP parameter: Z_0 = 50 Ω, t_p = 100 ns, t_r = 300 ps, averaging window: t_1 = 30 ns to t_2 = 60 ns, extraction of dynamic resistance using least squares fit of TLP characteristic between I_{TLP1} = 10 A and I_{TLP2} = 40 A. The equivalent stress level V_{IEC} according IEC 61000-4-2 (R = 330 Ω, C = 150 pF) is calculated at the broad peak of the IEC waveform at t = 30 ns with 2 A / kV

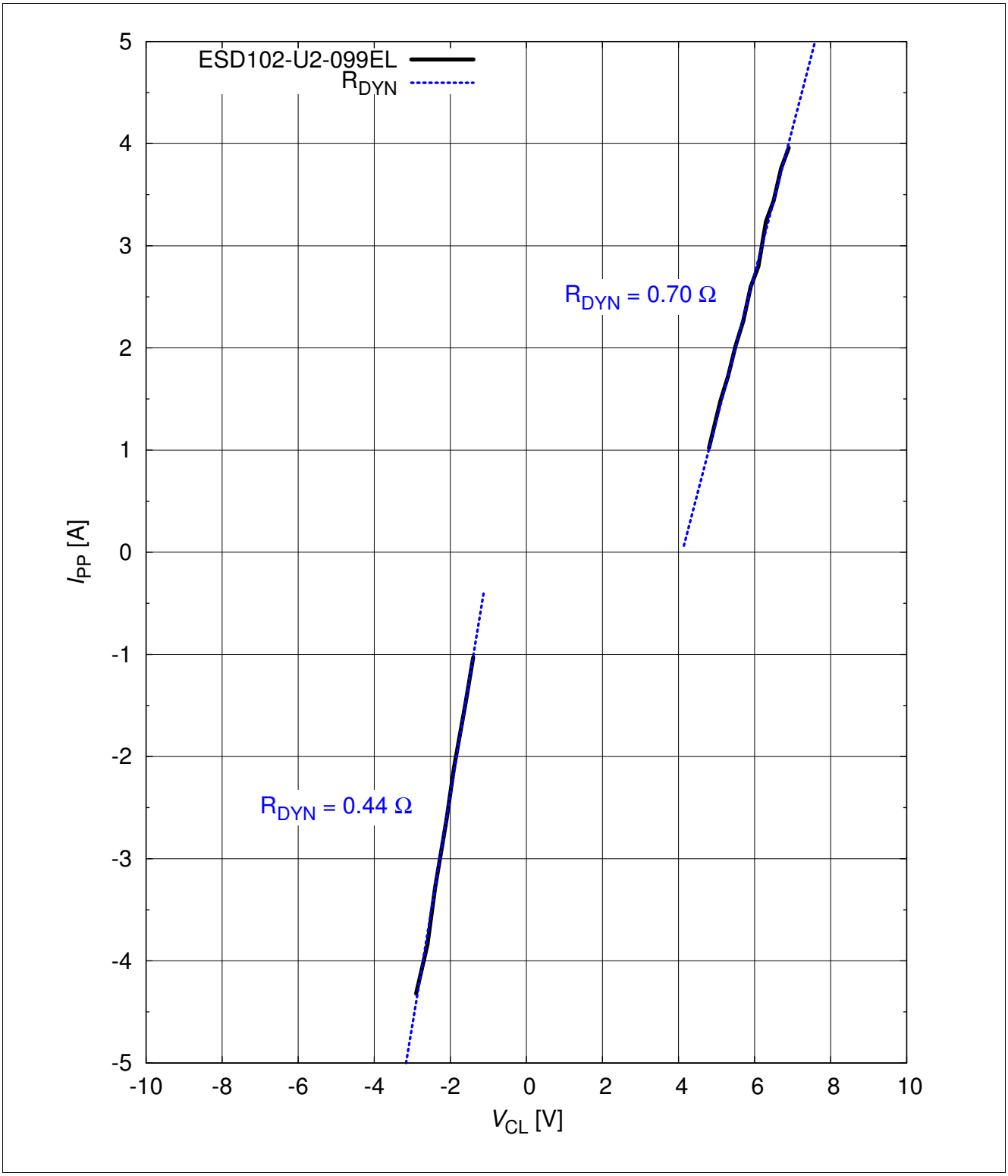

Figure 7 Pulse current (IEC61000-4-5) versus clamping voltage: $I_{PP} = f(V_{CL})$

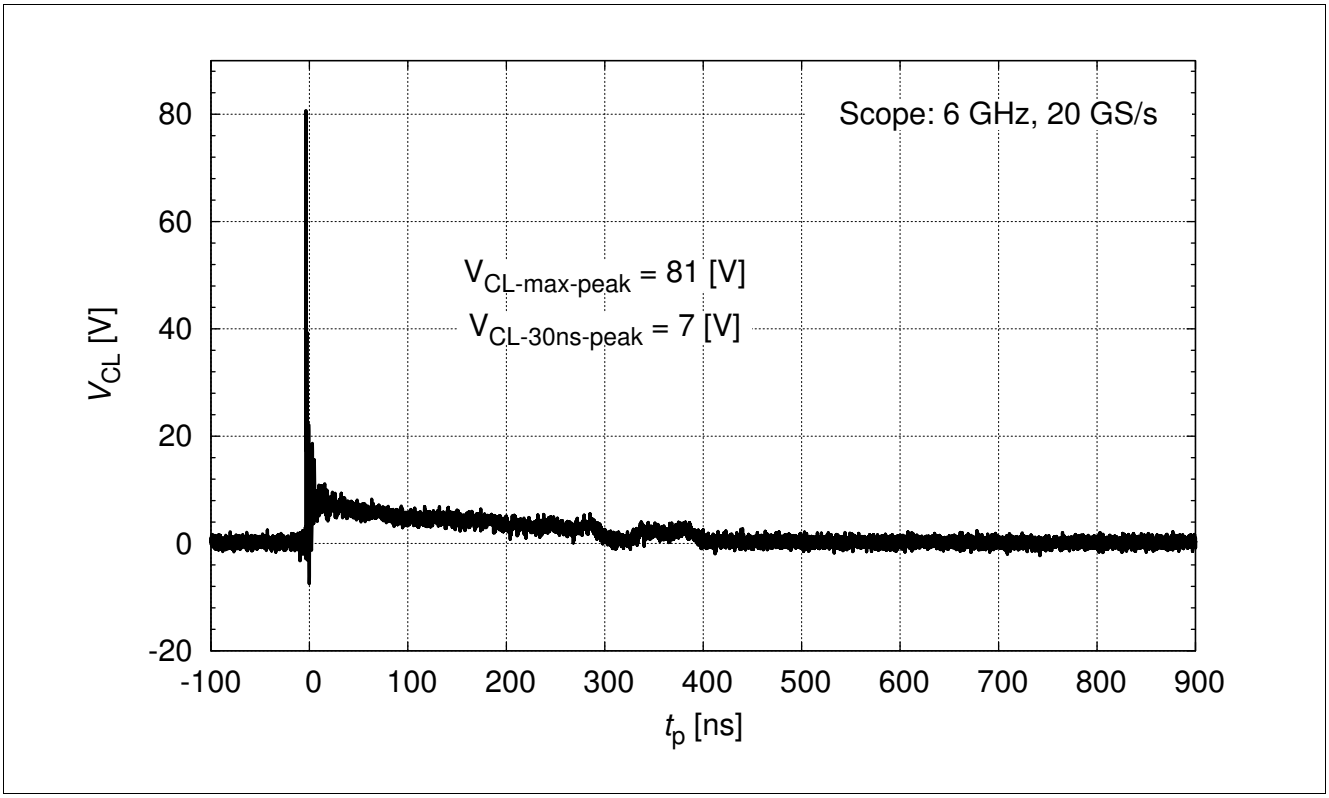

Figure 8 IEC61000-4-2 V_{CL} = *f*(*t*), 8 kV positive pulse from pin 1 to pin 2

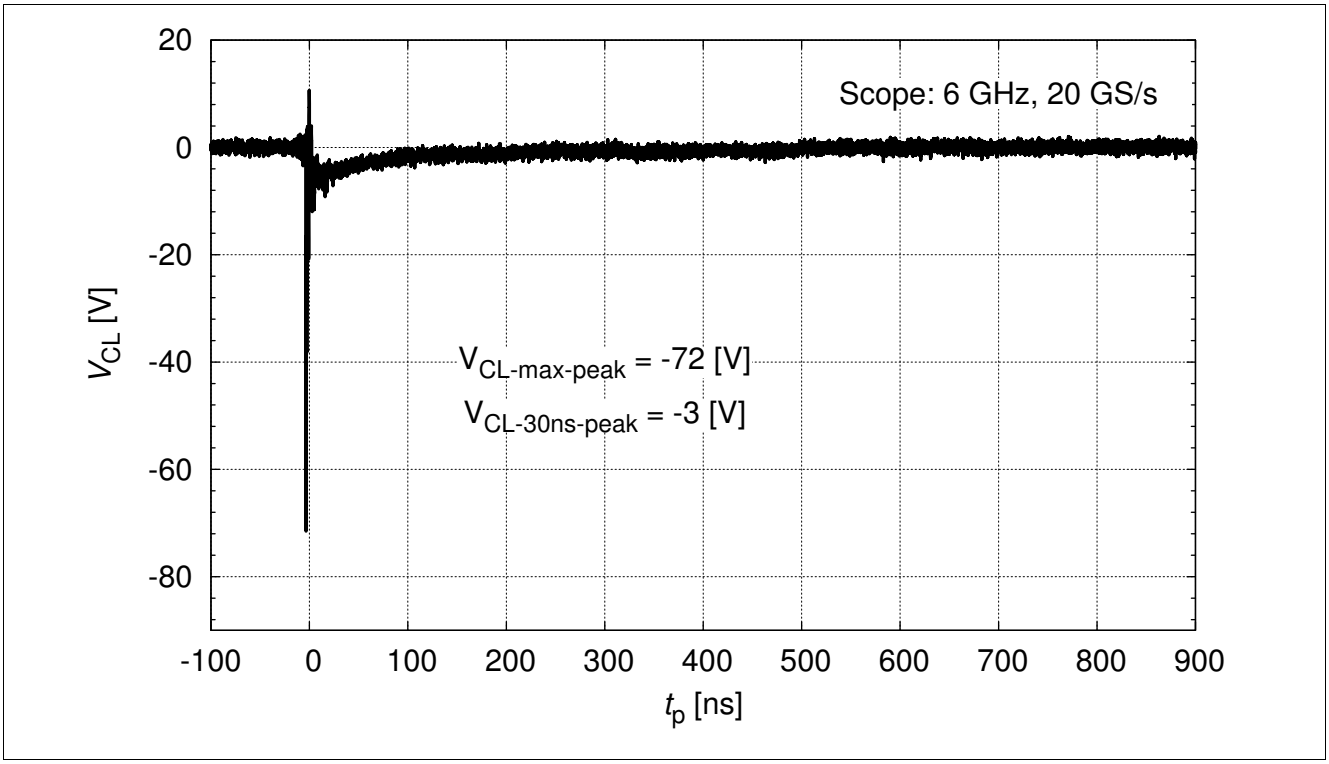

Figure 9 IEC61000-4-2 V_{CL} = *f*(*t*), 8 kV negative pulse from pin 1 to pin 2

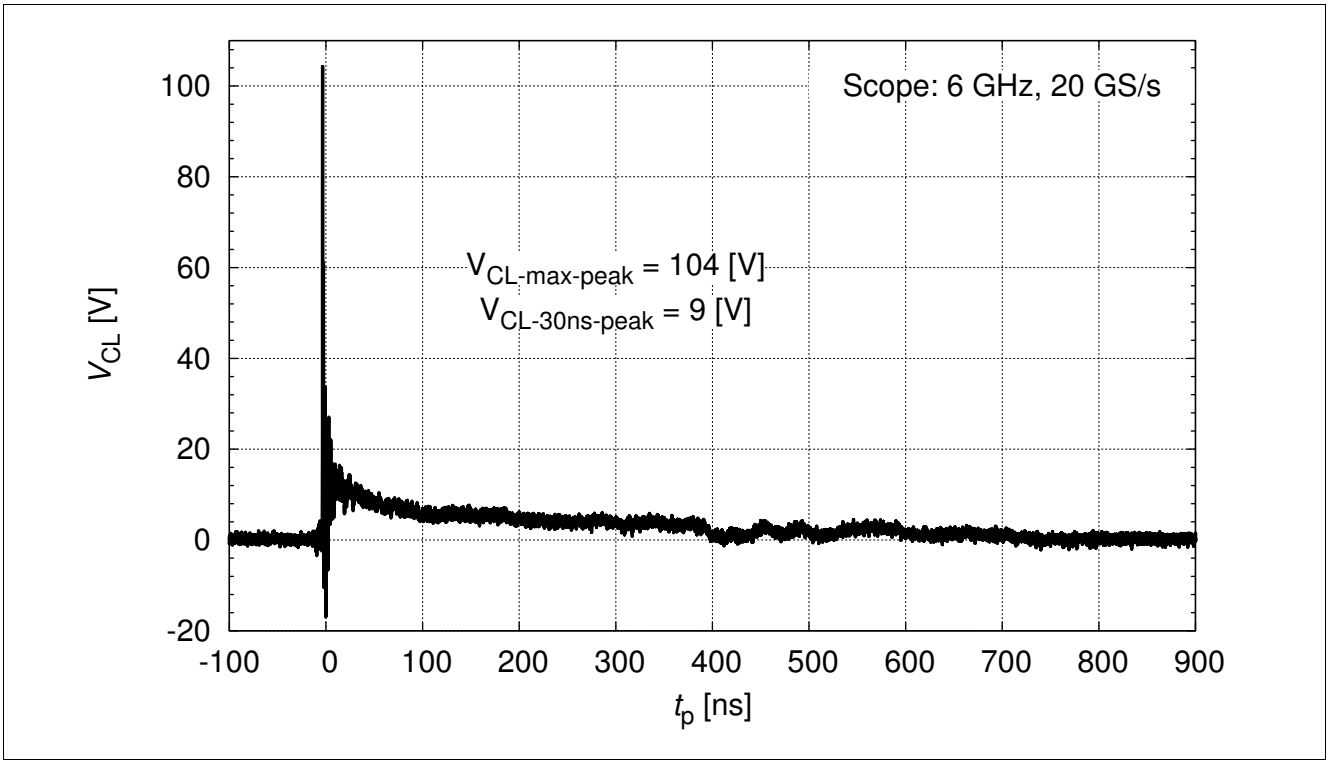

Figure 10 IEC61000-4-2 V_{CL} = $f(t)$, 15 kV positive pulse from pin 1 to pin 2

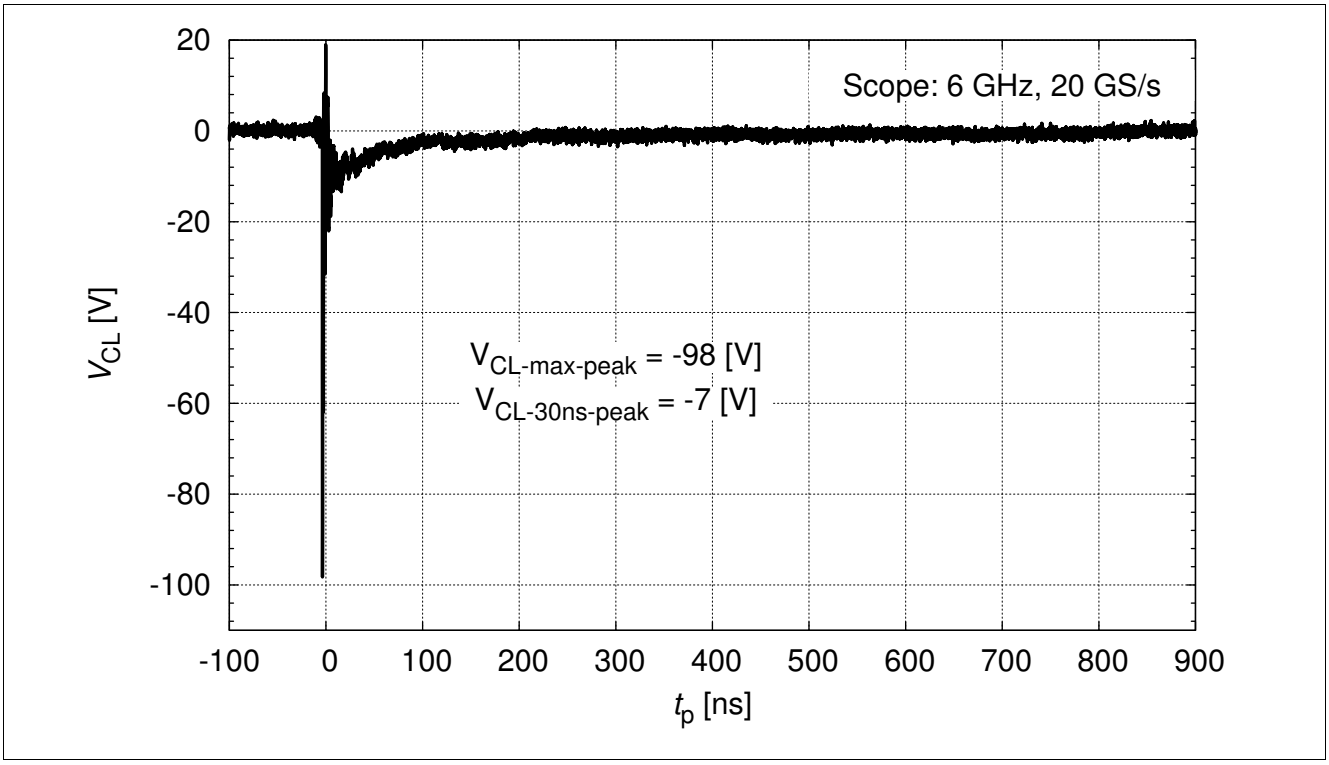

Figure 11 IEC61000-4-2 V_{CL} = $f(t)$, 15 kV negative pulse from pin 1 to pin 2

4 Package Information

4.1 TSLP-4-10 (mm)

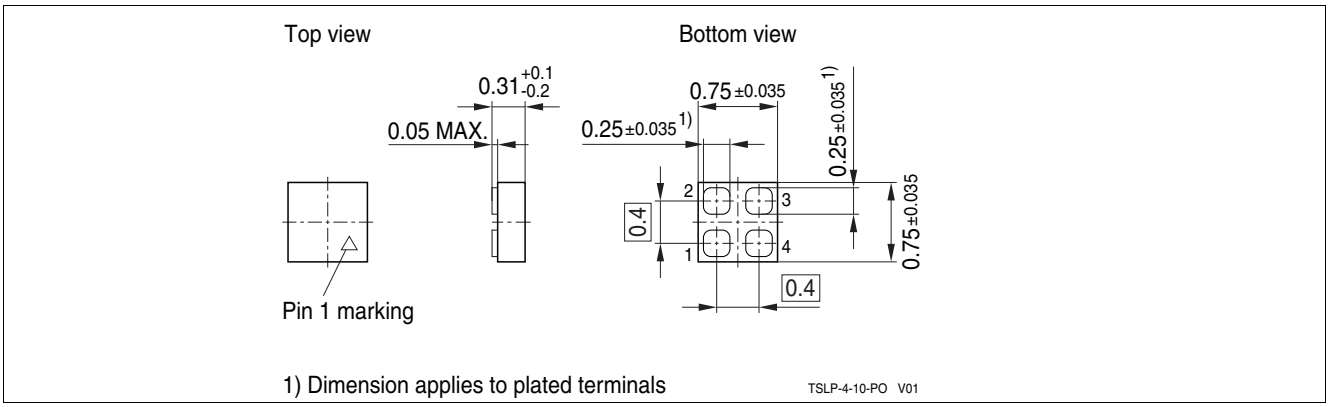

Figure 12 TSLP-4-10: Package outline (dimension in mm)

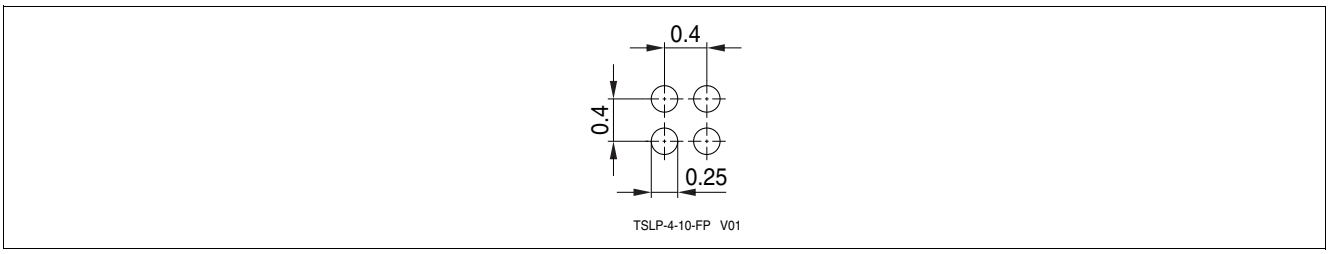

Figure 13 TSLP-4-10: Footprint (dimension in mm)

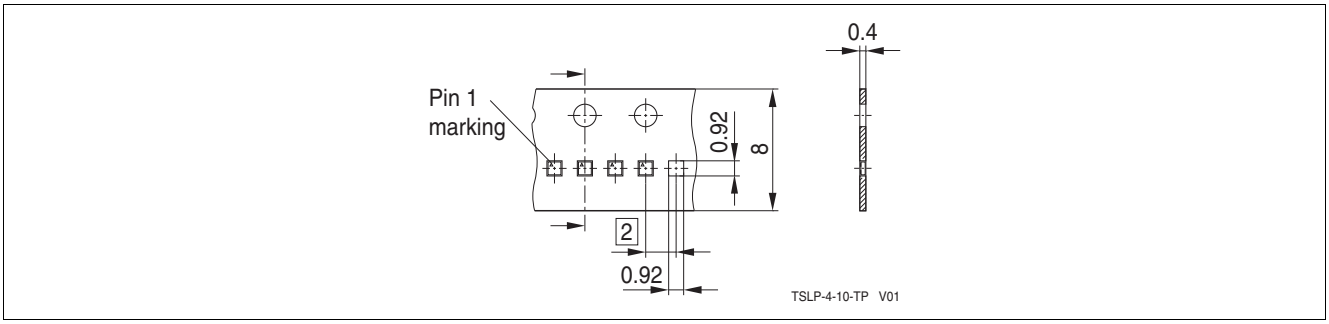

Figure 14 TSLP-4-10: Packing dimension in mm)

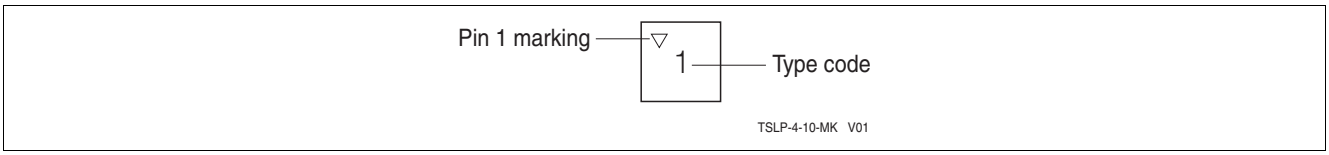

Figure 15 TSLP-4-10: Marking (example)

References

[1] **On-chip ESD protection for integrated circuits**, Albert Z. H. Wang, ISBN:0-7923-7647-1

[2] Infineon Technologie AG - **Application Note AN210**: Effective ESD Protection Design at System Level Using VF-TLP Characterization Methodology

[3] Infineon Technologie AG - **Application Note AN240**: Effective ESD Protection for USB3.0, combined with perfect Signal Intergrity.

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