EPC2050 – Enhancement-Mode Power Transistor
Preliminary Specification Sheet

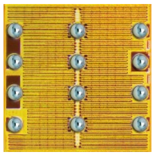
Status: Engineering

Features:

- V_{DS}, 350 V
- Maximum $R_{DS(on)}$, 65 mΩ
- I_D, 6.3 A

Applications:

- Multi-Level AC-DC Conversion
- EV Charging
- Solar Power Inverters
- Motor Drives
- Wireless Power Class-E Amplifiers
- LED Lighting
- Medical Imaging



EPC2050 eGaN® FETs are supplied in passivated die form with solder bumps.

Die Size: 1.95 mm x 1.95 mm

Maximum Ratings			
V_{DS}	Drain-to-Source Voltage (Continuous)	350	V
I_D	Continuous (T_A = 25˚C, $R_{θJA}$= 26 ˚C/W)	6.3	A
	Pulsed (25˚C, T_{PULSE} = 300 µs)	26	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	˚C
T_{STG}	Storage Temperature	-40 to 150	

Static Characteristics (T_J= 25˚C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 120 µA	350			V
I_{DSS}	Drain Source Leakage	V_{DS} = 280 V, V_{GS} = 0 V		2	20	µA
I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 5 V		0.1	1	mA
	Gate-to-Source Reverse Leakage	V_{GS} = -4 V		2	20	µA
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 1.5 mA	0.8	1.4	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D = 6 A		42	65	mΩ
V_{SD}	Source-Drain Forward Voltage	I_S = 0.5 A, V_{GS} = 0 V		2.2		V

All measurements were done with substrate shorted to source.

Thermal Characteristics

		TYP	UNIT
$R_{θJC}$	Thermal Resistance, Junction to Case	1.4	˚C/W
$R_{θJB}$	Thermal Resistance, Junction to Board	9.2	˚C/W
$R_{θJA}$	Thermal Resistance, Junction to Ambient (Note 1)	64	˚C/W

Note 1: $R_{θJA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.
See http://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.

Dynamic Characteristics (T_J= 25˚C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	V_{DS} = 280 V, V_{GS} = 0 V		420	505	pF
C_{RSS}	Reverse Transfer Capacitance			0.3		
C_{OSS}	Output Capacitance			55	83	
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (note 2)	V_{DS} = 0 to 280 V, V_{GS} = 0 V		83		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (note 3)			116		
Q_G	Total Gate Charge	V_{DS} = 280 V, V_{GS} = 5 V, I_D= 6 A		3.4	4.3	nC
Q_{GS}	Gate-to-Source Charge	V_{DS} = 280 V, I_D = 6 A		1.4		
Q_{GD}	Gate-to-Drain Charge			0.4		
$Q_{G(TH)}$	Gate Charge at Threshold			1		
Q_{OSS}	Output Charge	V_{DS} = 280 V, V_{GS} = 0 V		33	50	
Q_{RR}	Source-Drain Recovery Charge			0		

Note 2: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.

Note 3: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DS}.

All measurements were done with substrate shorted to source.

Figure 1: Typical Output Characteristics at 25°C

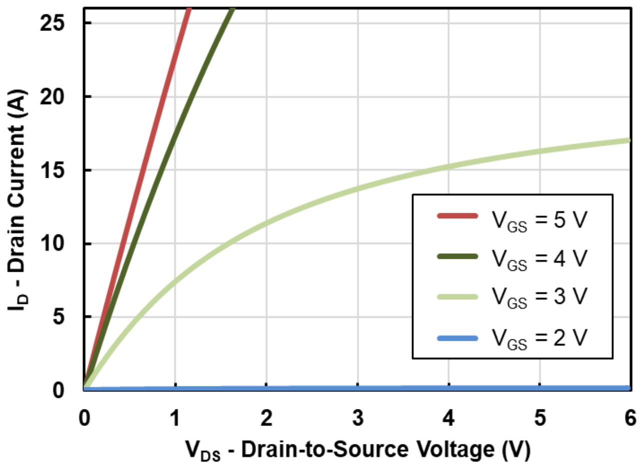


Figure 2: Transfer Characteristics

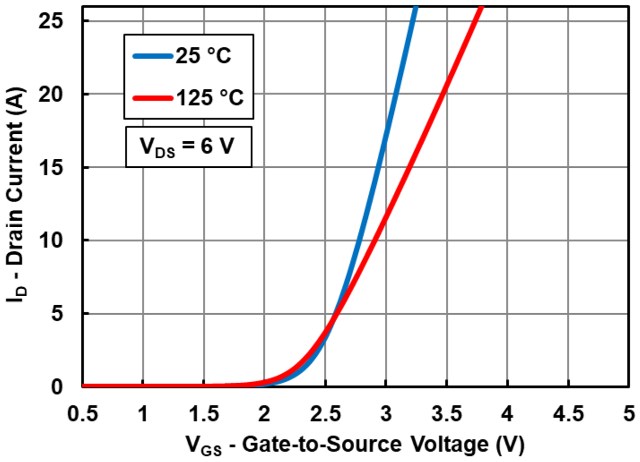


Figure 3: $R_{DS(on)}$ vs V_{GS} for Various Drain Currents

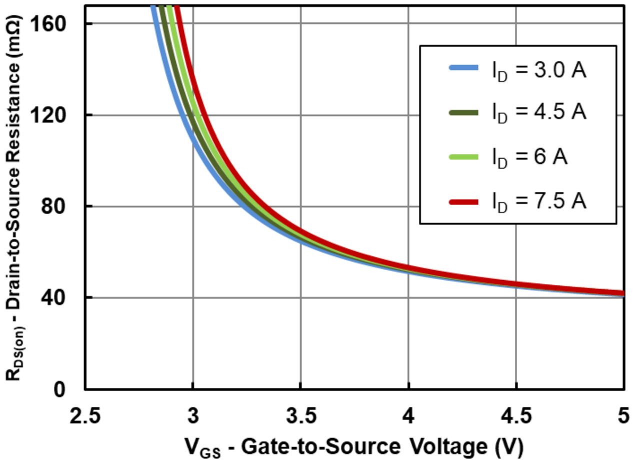


Figure 4: $R_{DS(on)}$ vs V_{GS} for Various Temperatures

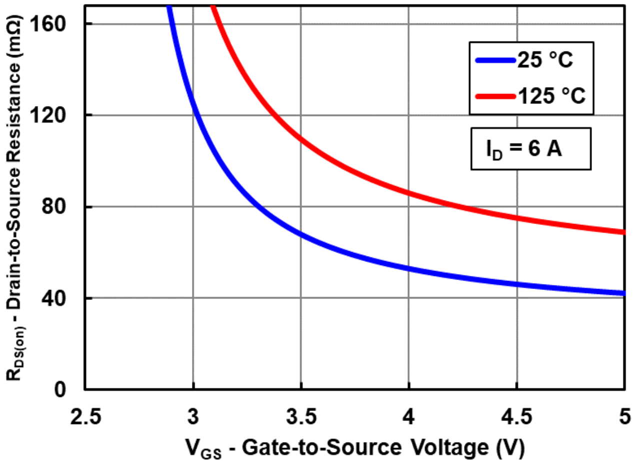


Figure 5a: Capacitance (Linear Scale)

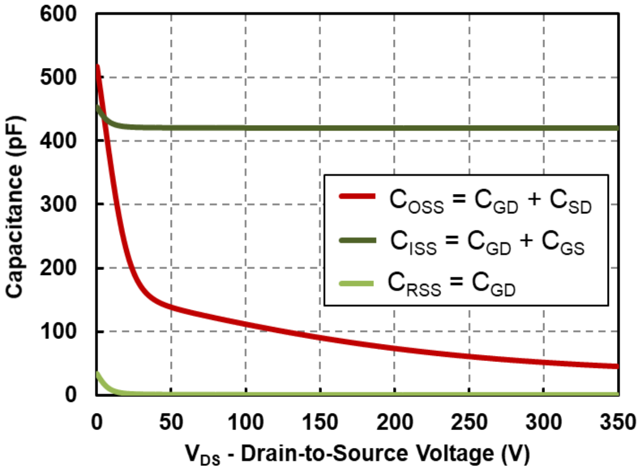


Figure 5b: Capacitance (Log Scale)

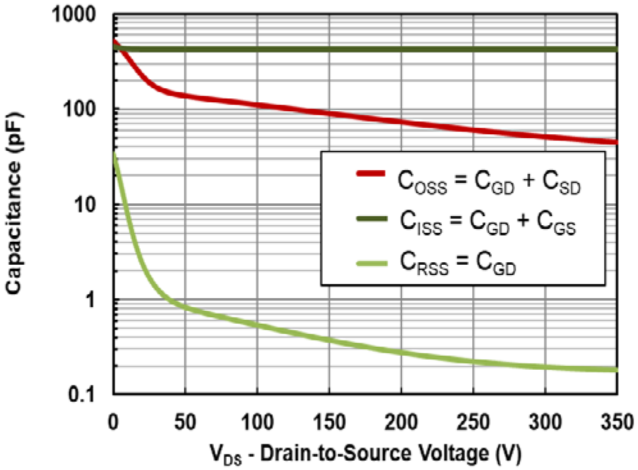


Figure 5c: Output Charge and C_{OSS} Stored Energy

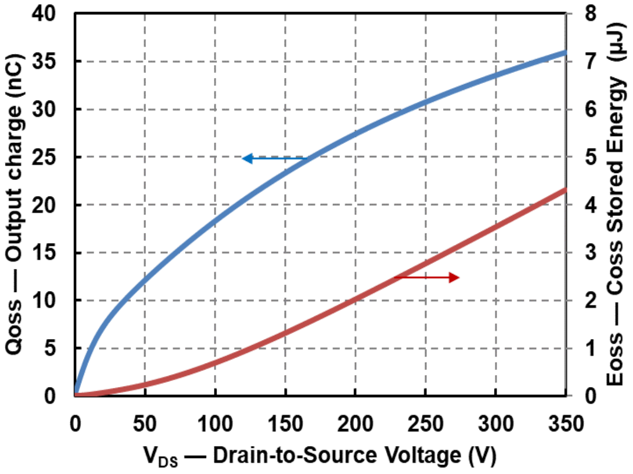


Figure 6: Gate Charge

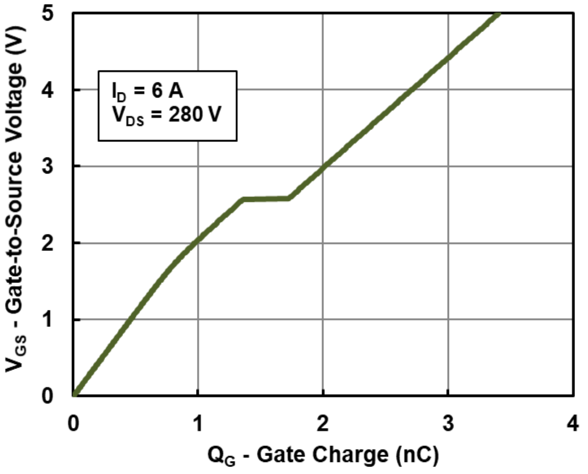


Figure 7: Reverse Drain-Source Characteristics

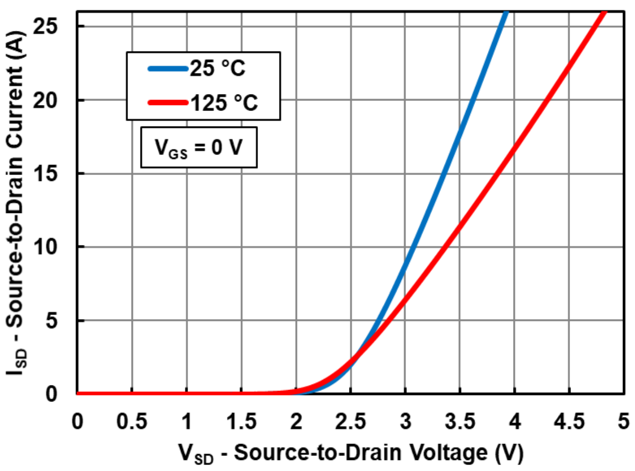


Figure 8: Normalized On-State Resistance vs Temperature

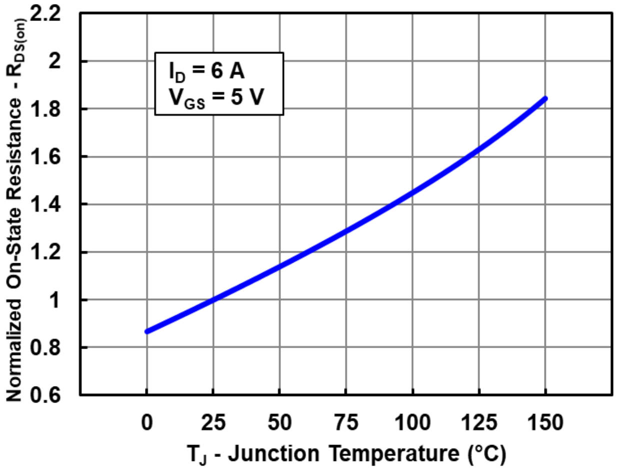


Figure 9: Normalized Threshold Voltage vs Temperature

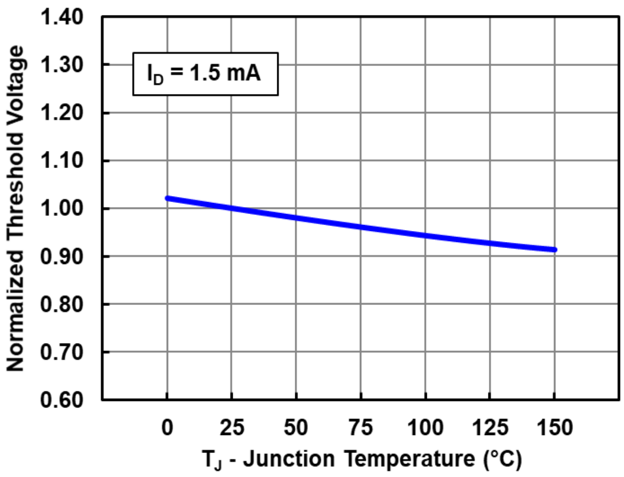


Figure 10: Safe Operating Area

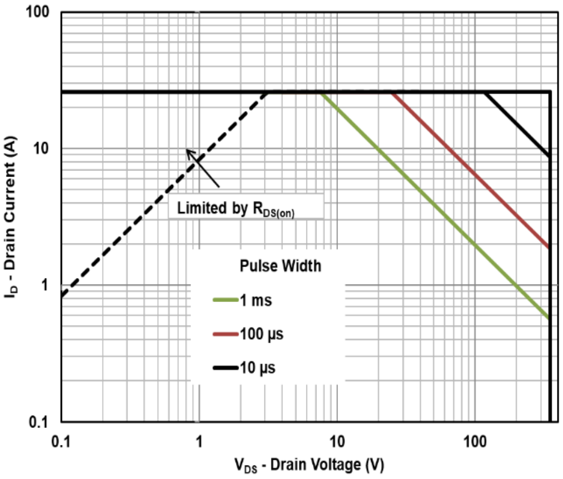
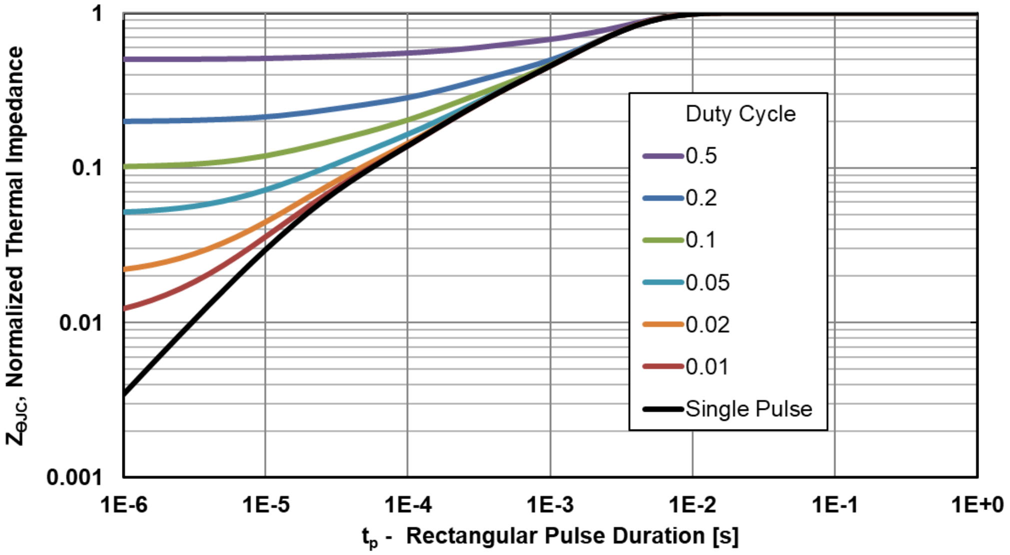
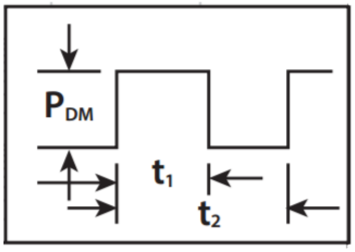


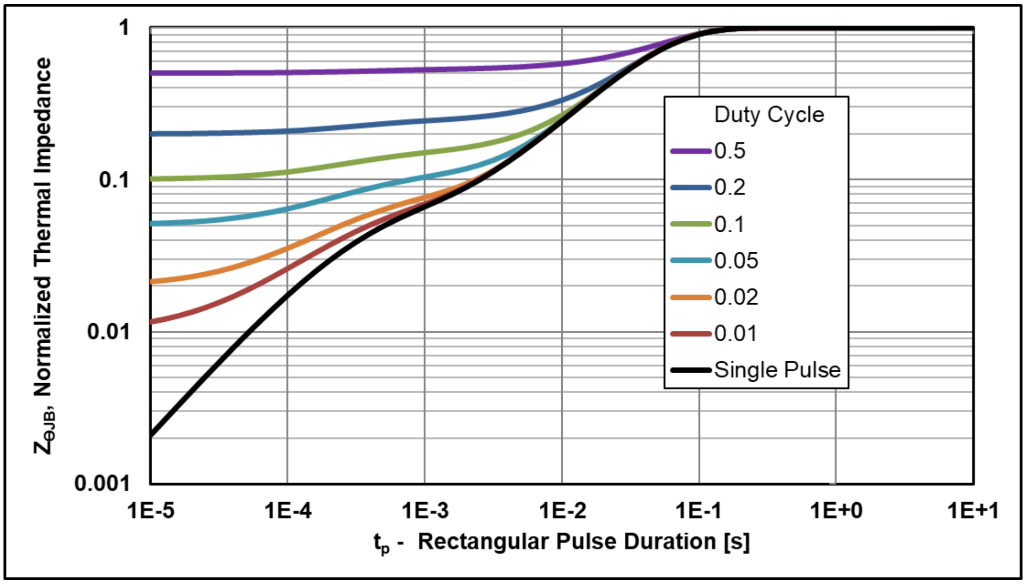
Figure 11a: Transient Thermal Response Curves (Junction-to-Case)

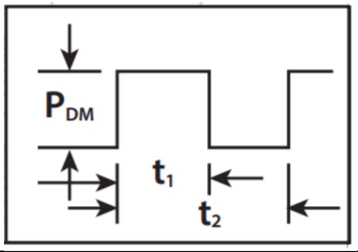




Notes:
Duty Factor: D = t_1/t_2
Peak $T_J = P_{DM} \times Z_{\theta JC} \times R_{\theta JC} + T_C$

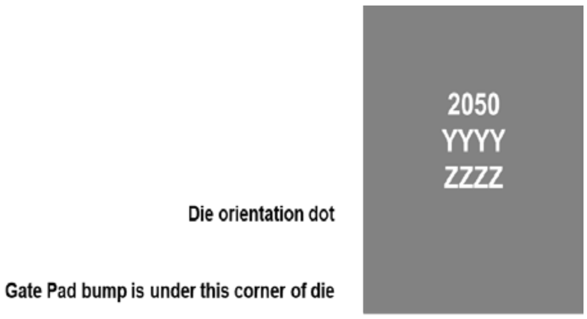
Figure 11b: Transient Thermal Response Curves (Junction-to-Board)





Notes:
Duty Factor: D = t_1/t_2
Peak $T_J = P_{DM} \times Z_{\theta JB} \times R_{\theta JB} + T_B$

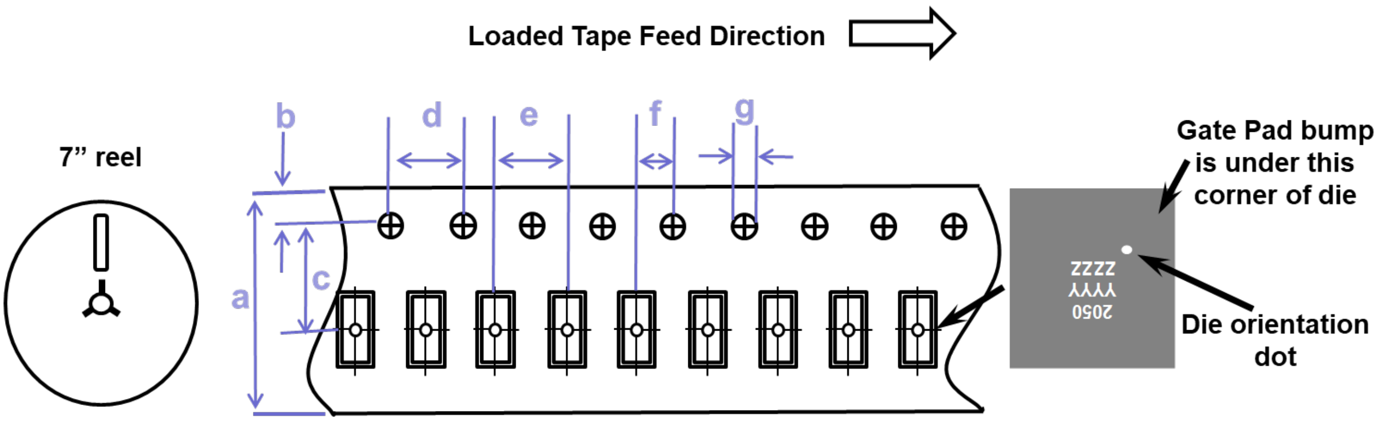
DIE MARKINGS



Part Number	Laser Marking		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2050	2050	YYYY	ZZZZ

TAPE AND REEL DRAWINGS

4mm pitch, 8mm wide tape on 7” reel



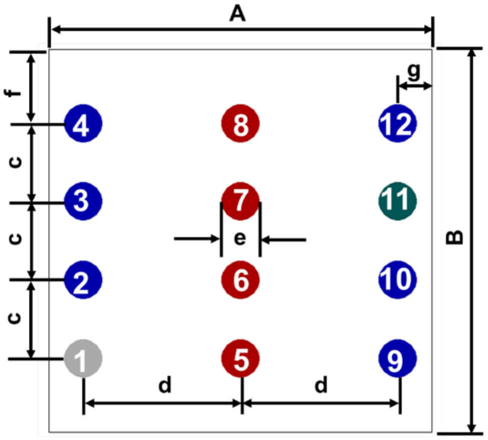
Die is placed into pocket bump side down (face side down)

	EPC2050 (note 1)		
Dimension (mm)	target	min	max
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (note 2)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (note 2)	2.00	1.95	2.05
g	1.50	1.50	1.60

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.
Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

DIE OUTLINE

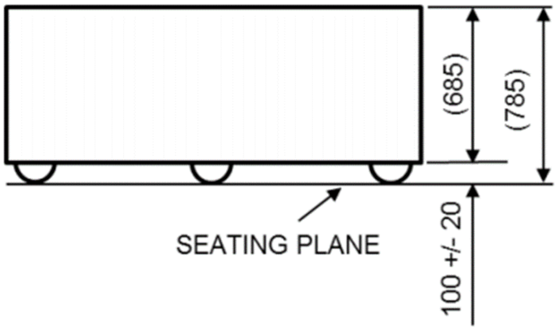
Solder Bump View



DIM	Micrometers		
	MIN	Nominal	MAX
A	1920	1950	1980
B	1920	1950	1980
c	400	400	400
d	800	800	800
e	180	200	220
f	360	375	390
g	160	175	190

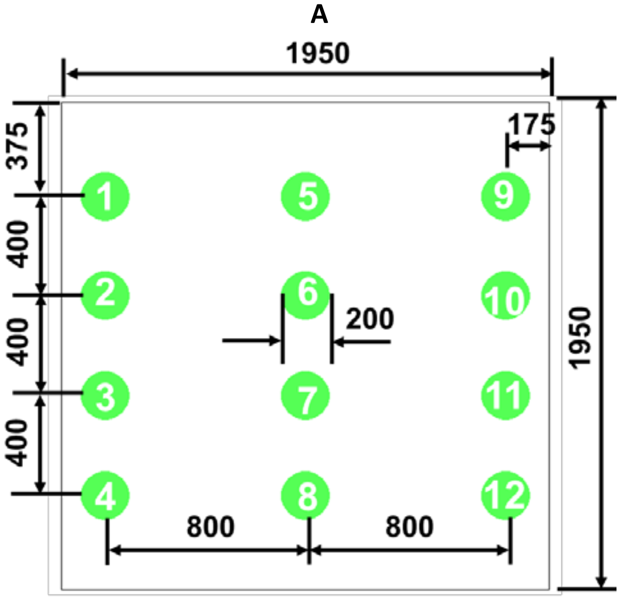
Pad 1 is Gate;
Pads 5, 6, 7, 8 are Drain;
Pads 2, 3, 4, 9, 10, 12 are Source;
Pad 11 is substrate

Side View



RECOMMENDED LAND PATTERN

(measurements in µm)



Pad 1 is Gate;

Pads 5, 6, 7, 8 are Drain;

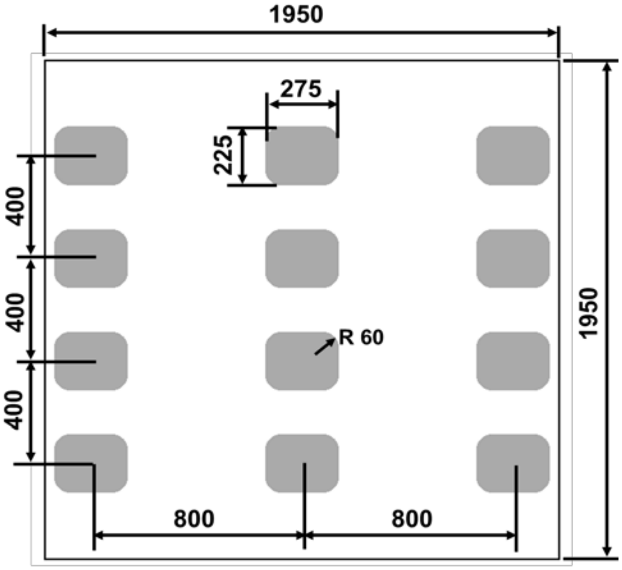
Pads 2, 3, 4, 9, 10, 12 are Source;

Pad 11 is substrate

The land pattern is solder mask defined

RECOMMENDED STENCIL DRAWING

(measurements in µm)



Recommended stencil should be 4mil (100µm) thick, must be laser cut, openings per drawing.

The corner has a radius of R60

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Additional assembly resources available at epc-co.com/epc/DesignSupport/AssemblyBasics.aspx

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