



ON Semiconductor®

## FDB9503L-F085

### P-Channel PowerTrench® MOSFET

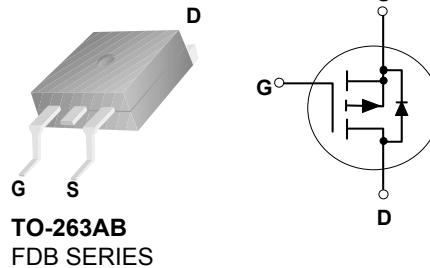
- 40 V, - 110 A, 2.6 mΩ

#### Features

- Typical  $R_{DS(on)}$  = 2.0 mΩ at  $V_{GS} = -10V$ ,  $I_D = -80 A$
- Typical  $Q_{g(tot)}$  = 196 nC at  $V_{GS} = -10V$ ,  $I_D = -80 A$
- UIS Capability
- RoHS Compliant
- Qualified to AEC Q101

#### Applications

- Automotive Engine Control
- PowerTrain Management
- Solenoid and Motor Drivers
- Electrical Power Steering
- Integrated Starter/Alternator
- Distributed Power Architectures and VRM
- Primary Switch for 12V Systems



**MOSFET Maximum Ratings**  $T_J = 25^\circ C$  unless otherwise noted.

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain-to-Source Voltage	-40	V
$V_{GS}$	Gate-to-Source Voltage	$\pm 16$	V
$I_D$	Drain Current - Continuous ( $V_{GS} = -10$ ) (Note 1)	$T_C = 25^\circ C$	-110
	Pulsed Drain Current	$T_C = 25^\circ C$	See Figure 4
$E_{AS}$	Single Pulse Avalanche Energy (Note 2)	984	mJ
$P_D$	Power Dissipation	333	W
	Derate Above $25^\circ C$	2.22	W/ $^\circ C$
$T_J, T_{STG}$	Operating and Storage Temperature	-55 to + 175	$^\circ C$
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.45	$^\circ C/W$
$R_{\theta JA}$	Maximum Thermal Resistance, Junction to Ambient (Note 3)	43	$^\circ C/W$

#### Notes:

- 1: Current is limited by wirebond configuration.
- 2: Starting  $T_J = 25^\circ C$ ,  $L = 0.3mH$ ,  $I_{AS} = -81A$ ,  $V_{DD} = -40V$  during inductor charging and  $V_{DD} = 0V$  during time in avalanche.
- 3:  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design, while  $R_{\theta JA}$  is determined by the board design. The maximum rating presented here is based on mounting on a 1 in<sup>2</sup> pad of 2oz copper.

#### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB9503L	FDB9503L-F085	TO-263AB	330mm	24mm	800 units

## Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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### Off Characteristics

$B_{V_{DSS}}$	Drain-to-Source Breakdown Voltage	$I_D = -250\mu\text{A}, V_{GS} = 0\text{V}$	-40	-	-	V
$I_{DSS}$	Drain-to-Source Leakage Current	$V_{DS} = -40\text{V}, T_J = 25^\circ\text{C}$	-	-	-1	$\mu\text{A}$
		$V_{GS} = 0\text{V}, T_J = 175^\circ\text{C}$ (Note 4)	-	-	-1	$\text{mA}$
$I_{GSS}$	Gate-to-Source Leakage Current	$V_{GS} = \pm 16\text{V}, V_{DS} = 0\text{V}$	-	-	$\pm 100$	$\text{nA}$

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = -250\mu\text{A}$	-1.0	-1.8	-3.0	V
$R_{DS(on)}$	Drain to Source On Resistance	$I_D = -80\text{A}, V_{GS} = -4.5\text{V}, T_J = 25^\circ\text{C}$	-	2.7	3.5	$\text{m}\Omega$
		$I_D = -80\text{A}, T_J = 25^\circ\text{C}$	-	2.0	2.6	$\text{m}\Omega$
		$V_{GS} = -10\text{V}, T_J = 175^\circ\text{C}$ (Note 4)	-	2.9	3.7	$\text{m}\Omega$

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = -20\text{V}, V_{GS} = 0\text{V},$ $f = 1\text{MHz}$	-	8320	-	$\text{pF}$
$C_{oss}$	Output Capacitance		-	5620	-	$\text{pF}$
$C_{riss}$	Reverse Transfer Capacitance		-	102	-	$\text{pF}$
$R_g$	Gate Resistance	$f = 1\text{MHz}$	-	20	-	$\Omega$
$Q_{g(ToT)}$	Total Gate Charge at 10V	$V_{GS} = 0$ to $-10\text{V}$	-	196	255	$\text{nC}$
$Q_{g(th)}$	Threshold Gate Charge	$V_{GS} = 0$ to $-2\text{V}$				
$Q_{gs}$	Gate-to-Source Gate Charge	$V_{DD} = -32\text{V}$ $I_D = -80\text{A}$	-	44	-	$\text{nC}$
$Q_{gd}$	Gate-to-Drain "Miller" Charge		-	22	-	$\text{nC}$

### Switching Characteristics

$t_{on}$	Turn-On Time	$V_{DD} = -20\text{V}, I_D = -80\text{A},$ $V_{GS} = -10\text{V}, R_{GEN} = 6\Omega$	-	-	146	$\text{ns}$
$t_{d(on)}$	Turn-On Delay		-	12	-	$\text{ns}$
$t_r$	Rise Time		-	86	-	$\text{ns}$
$t_{d(off)}$	Turn-Off Delay		-	700	-	$\text{ns}$
$t_f$	Fall Time		-	310	-	$\text{ns}$
$t_{off}$	Turn-Off Time		-	-	1538	$\text{ns}$

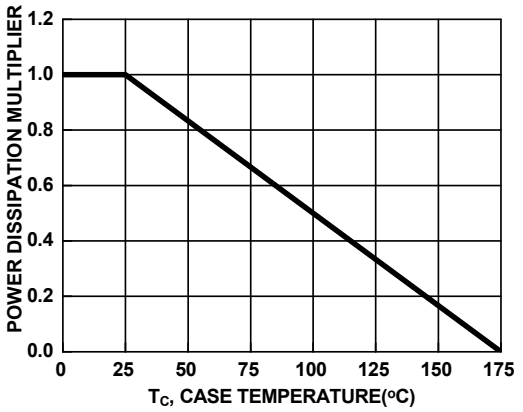
### Drain-Source Diode Characteristics

$V_{SD}$	Source-to-Drain Diode Voltage	$I_{SD} = -80\text{A}, V_{GS} = 0\text{V}$	-	-	-1.25	V
		$I_{SD} = -40\text{A}, V_{GS} = 0\text{V}$	-	-	-1.2	V
$t_{rr}$	Reverse-Recovery Time	$I_{SD} = -80\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s},$	-	124	186	$\text{ns}$
$Q_{rr}$	Reverse-Recovery Charge	$V_{DD} = -32\text{V}$	-	214	321	$\text{nC}$

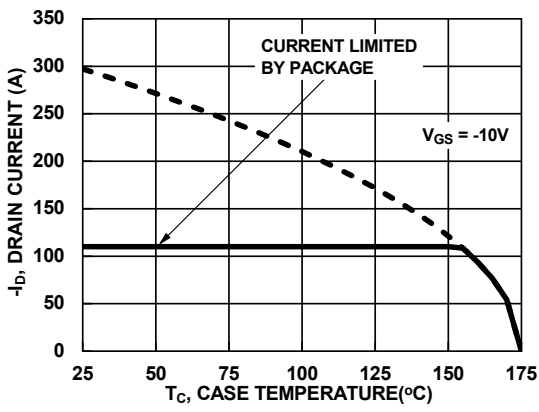
#### Note:

4: The maximum value is specified by design at  $T_J = 175^\circ\text{C}$ . Product is not tested to this condition in production.

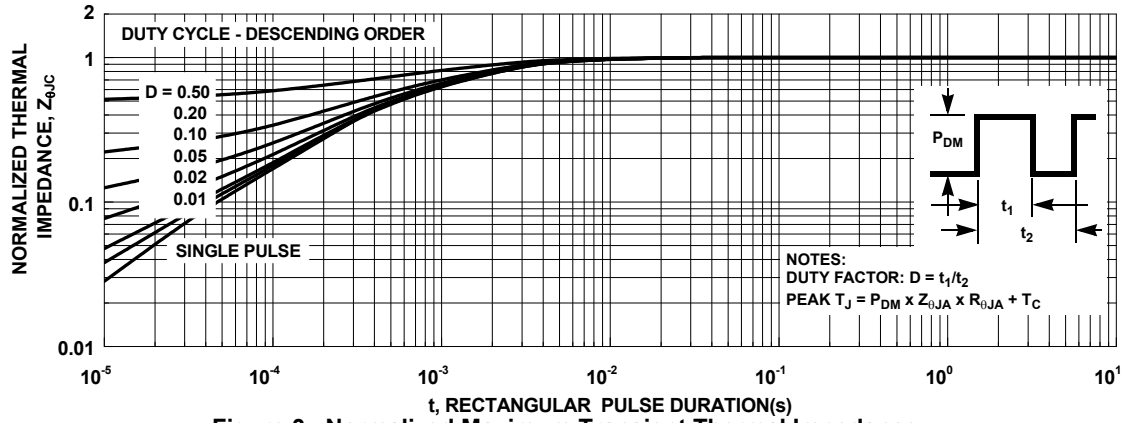
**Typical Characteristics**



**Figure 1. Normalized Power Dissipation vs. Case Temperature**



**Figure 2. Maximum Continuous Drain Current vs. Case Temperature**



**Figure 3. Normalized Maximum Transient Thermal Impedance**

## Typical Characteristics

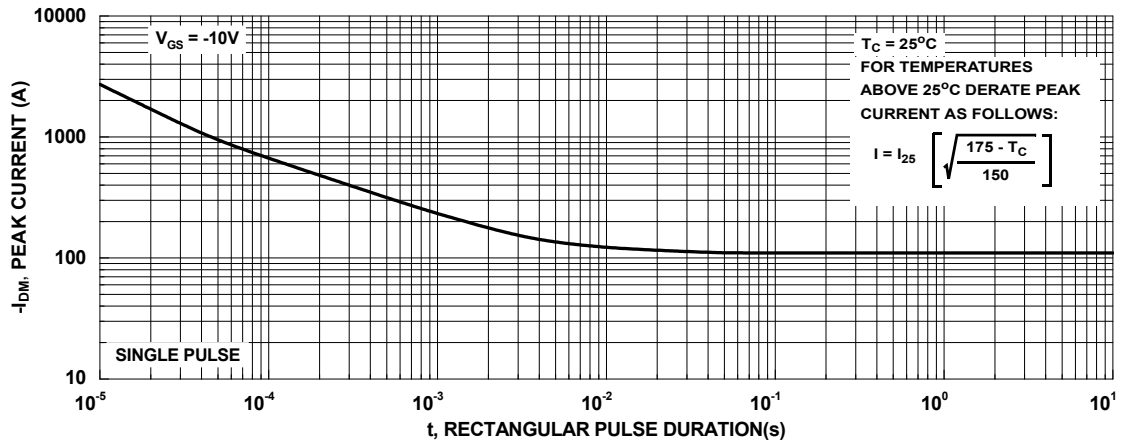


Figure 4. Peak Current Capability

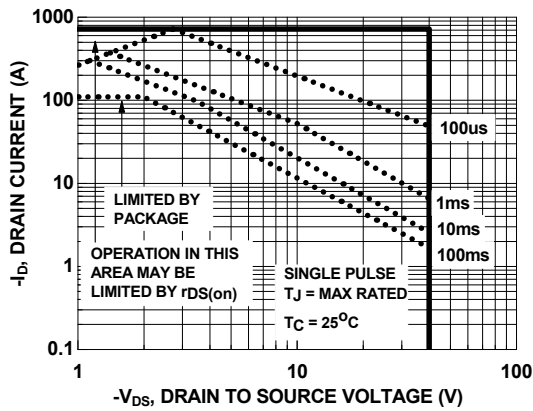
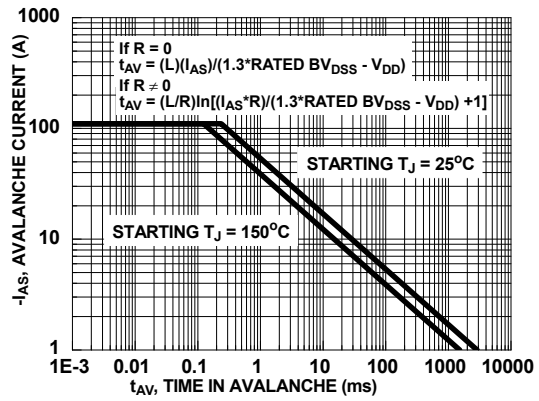


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to ON Semiconductor Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

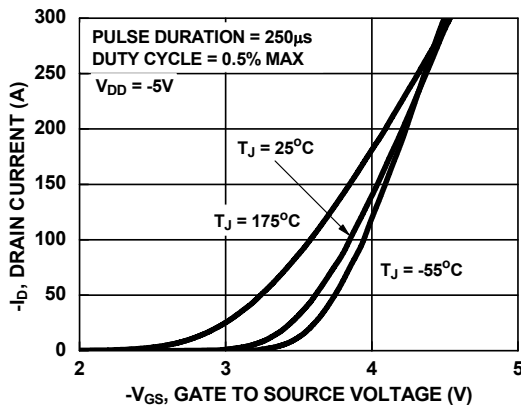


Figure 7. Transfer Characteristics

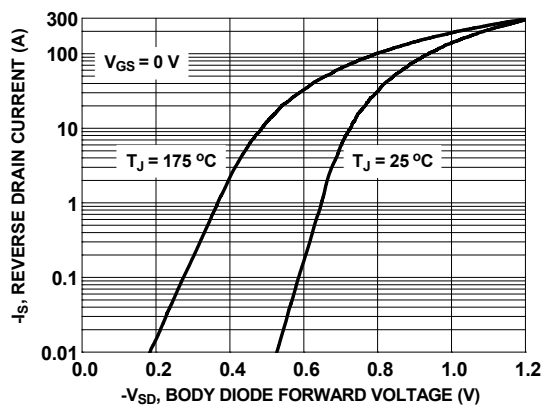


Figure 8. Forward Diode Characteristics

## Typical Characteristics

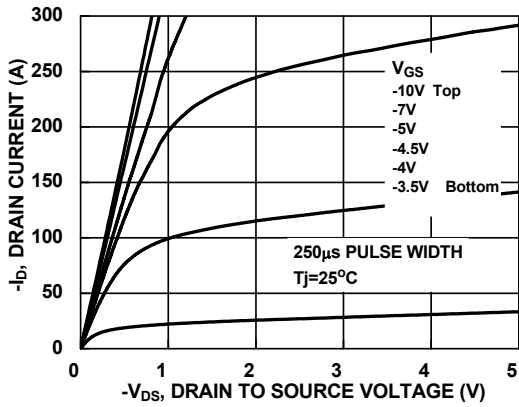


Figure 9. Saturation Characteristics

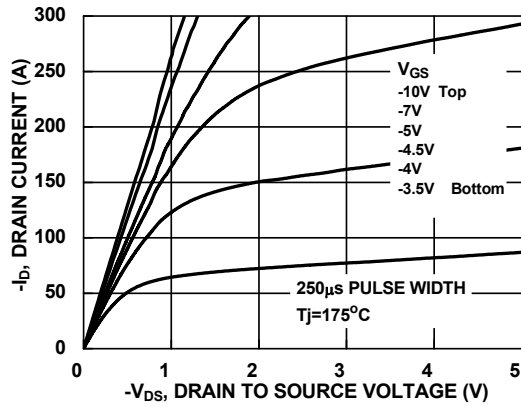


Figure 10. Saturation Characteristics

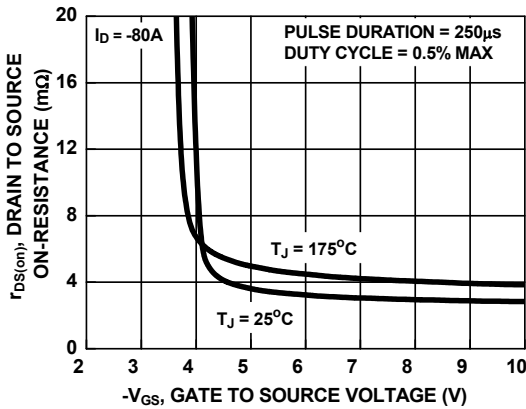


Figure 11.  $R_{DS(on)}$  vs. Gate Voltage

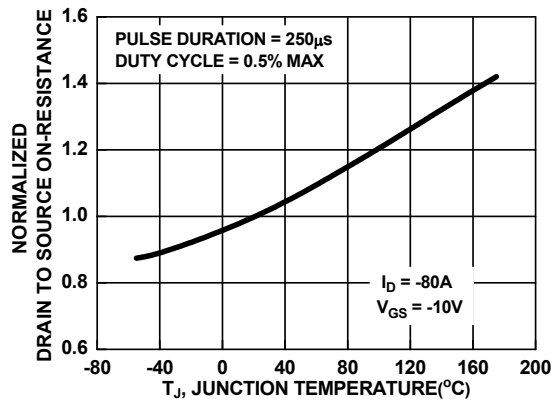


Figure 12. Normalized  $R_{DS(on)}$  vs. Junction Temperature

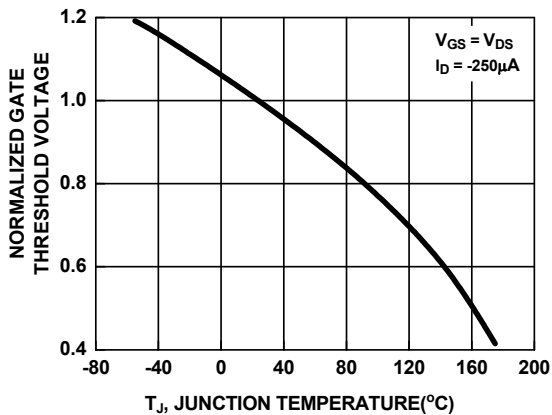


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

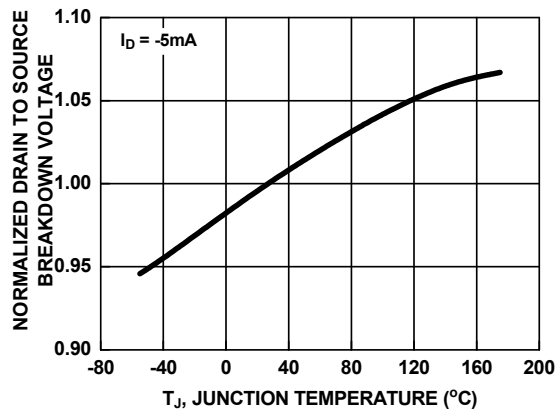


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

## Typical Characteristics

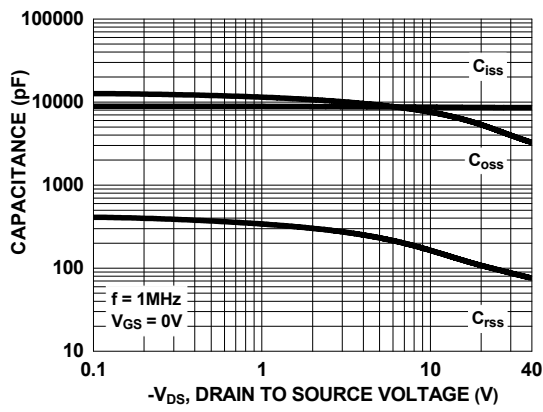


Figure 15. Capacitance vs. Drain to Source Voltage

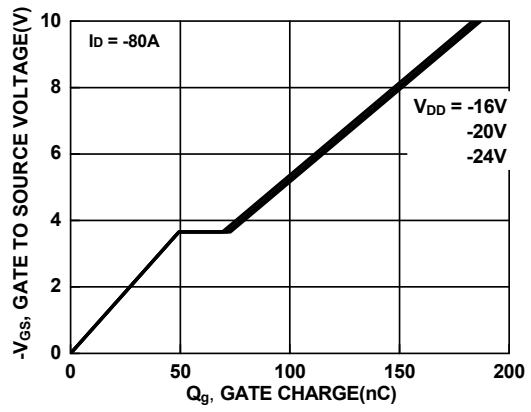


Figure 16. Gate Charge vs. Gate to Source Voltage

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