Cyclone V E Video Development System

The Cyclone V E Video Development System is an ideal video processing platform for high-performance, cost-effective video applications. The Cyclone® V E Development Kit offers a comprehensive general purpose development platform for many markets and applications. With multiple banks of DDR3 and LPDDR2 memory, this kit provides the ideal low-cost platform for high-bandwidth video processing. Additional features include an LCD character display, LEDs, user switches, USB and RJ-45 connectors.
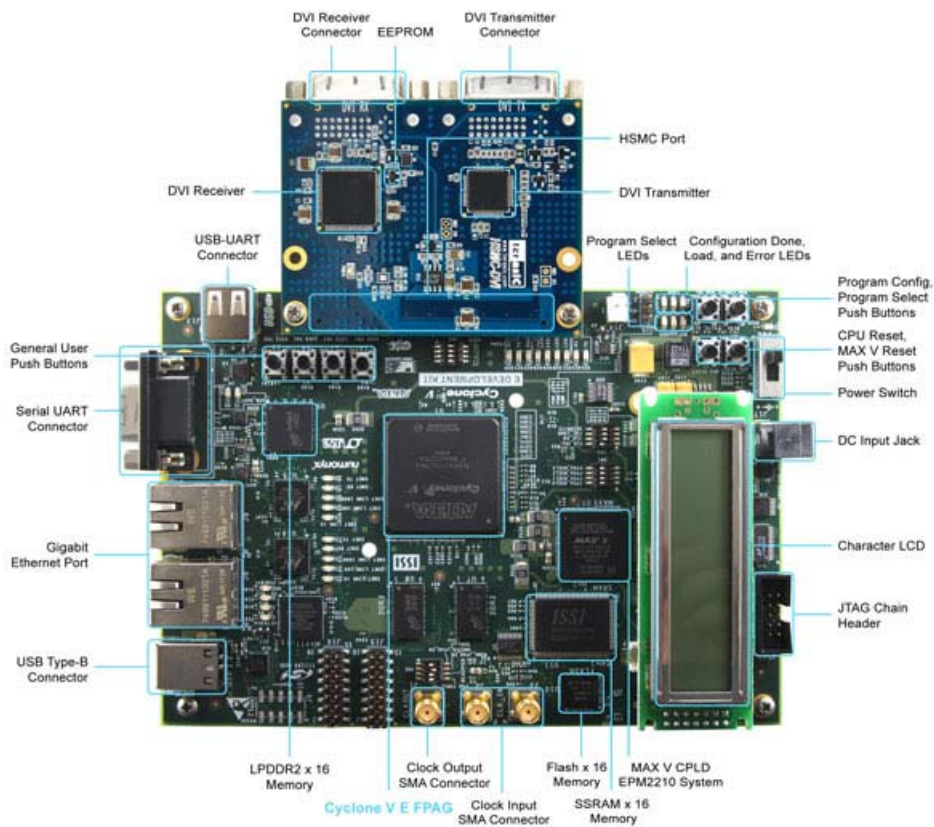
The DVI-HSMC daughter card part of the bundled package will allow developers to access high quality and high resolution video signals that can support resolution up to 1600x1200. A complete DVI video controller design with source code is provided.

Terasic recognized for its strong design expertise in high-end video, imaging and multimedia products have made available a video development package that targets video processing development. The platform can also allow users to experience advanced image processing designs incorporating VIP (Altera's Video and Image Processing Suite MegaCore Functions).

Cyclone V E Video Development System

DVI Receiver Connector EEPROM DVI Transmitter Connector

DVI Receiver

USB-UART Connector

General User Push Buttons

Serial UART Connector

Gigabit Ethernet Port

USB Type-B Connector

HSMC Port

DVI Transmitter

Program Select LEDs Configuration Done, Load, and Error LEDs

Program Config, Program Select Push Buttons

CPU Reset, MAX V Reset Push Buttons

Power Switch

DC Input Jack

Character LCD

JTAG Chain Header

LPDDR2 x 16 Memory Clock Output SMA Connector Flash x 16 Memory MAX V CPLD EPM2210 System

Cyclone V E FPAG Clock Input SMA Connector SSRAM x 16 Memory

Cyclone V E Video Development System

Altera Cyclone V E Video Development System

Featured devices:

- Cyclone V E FPGA - 5CEFA7F31C7NES
- MAX V CPLD - 5M2210ZF256I5N (system controller)
- MAX II CPLD - EPM240M100I5N (embedded USB Blaster II)

Configuration:

- On-board USB-Blaster™ II cable (USB, PHY, Max®V CPLD)
- JTAG direct via JTAG header

Memory devices

- DDR3 x32 at 300 MHz (soft memory controller)
- LPDDR2 x16 (soft memory controller)
- Flash (512 Mb)
- SSRAM (18 Mb)
- EEPROM (64 Kb)

General user input/output

- User control
- Four pushbuttons
- Five LEDs
- Four DIP switches
- 2x Resets (CPU reset, Dev Clear)
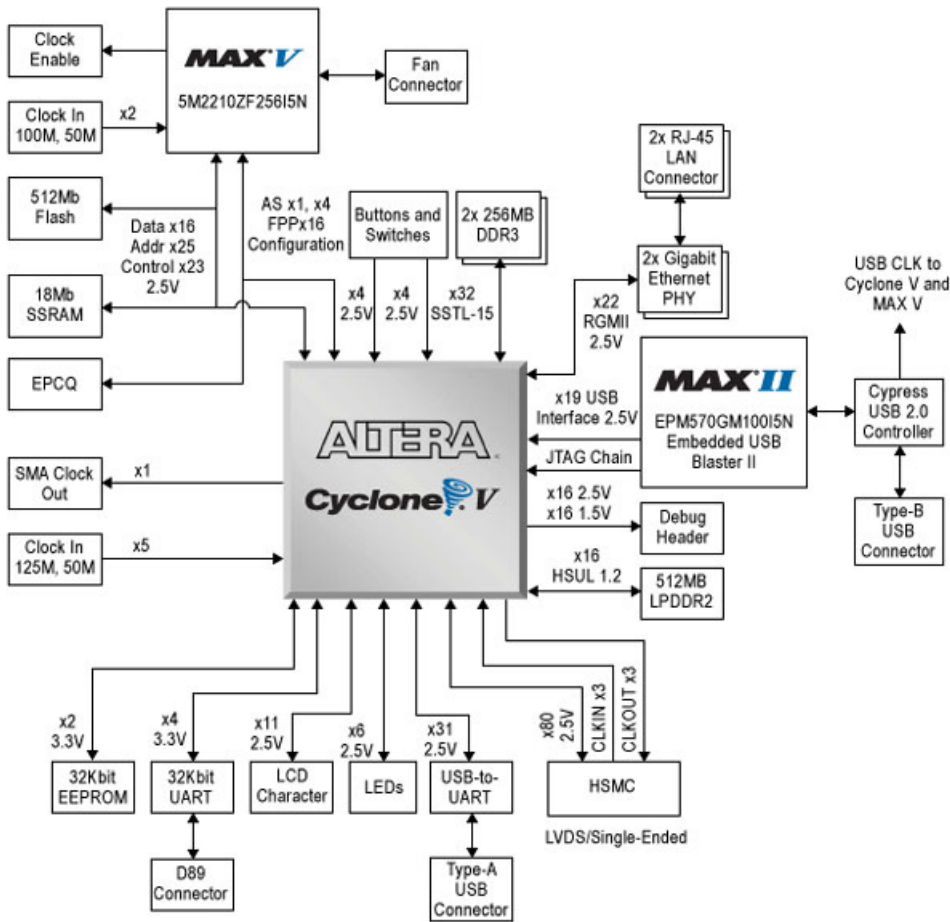- LCD: Character LCD (16x2)

Components and interfaces

- RJ45 for Ethernet
- UART interface

Quartus®II design software information

- Quartus II Web Edition Software

Altera Cyclone V E FPGA Development Board Block Diagram

Clock Enable

MAX V
5M2210ZF256I5N

Fan Connector

Clock In 100M, 50M   x2

512Mb Flash

Data x16
Addr x25
Control x23
2.5V

AS x1, x4
FPPx16
Configuration

Buttons and Switches

2x 256MB DDR3

2x RJ-45 LAN Connector

2x Gigabit Ethernet PHY

USB CLK to Cyclone V and MAX V

18Mb SSRAM

EPCQ

x4 2.5V   x4 2.5V   x32 SSTL-15

x22 RGMII 2.5V

MAX II
EPM570GM100I5N
Embedded USB Blaster II

Cypress USB 2.0 Controller

x19 USB Interface 2.5V

ALTERA
Cyclone V

JTAG Chain

SMA Clock Out   x1

Clock In 125M, 50M   x5

x16 2.5V
x16 1.5V

Debug Header

Type-B USB Connector

x16 HSUL 1.2

512MB LPDDR2

x2 3.3V   x4 3.3V   x11 2.5V   x6 2.5V   x31 2.5V   x80 2.5V   CLKIN x3   CLKOUT x3

32Kbit EEPROM   32Kbit UART   LCD Character   LEDs   USB-to-UART   HSMC

LVDS/Single-Ended

D89 Connector

Type-A USB Connector

Terasic DVI-HSMC Card

Digital Transmitter

- One DVI transmitter with single transmitting port
- Digital Visual Interface (DVI) Compliant
- Supports resolutions from VGA to UXGA (25 MHz – 165 MHz Pixel Rates)
- Universal Graphics Controller Interface
  - 12-Bit, Dual-Edge and 24-Bit, Single-Edge Input Modes
  - Adjustable 1.1 V to 1.8 V and Standard 3.3 V CMOS Input Signal Levels
  - Fully Differential and Single-Ended Input Clocking Modes
  - Standard Intel 12-Bit Digital Video Port Compatible as on Intel™ 81x Chipsets
- Enhanced PLL Noise Immunity
  - On-Chip Regulators and Bypass Capacitors for Reducing System Costs
- Enhanced Jitter Performance
  - No HSYNC Jitter Anomaly
  - Negligible Data-Dependent Jitter
    - Programmable Using I²C Serial Interface
    - Single 3.3-V Supply Operation

Digital Receiver

- One DVI receiver with single receiving port

- Supports UXGA Resolution (Output Pixel Rates Up to 165 MHz)
- Digital Visual Interface (DVI) Specification Compliant
- True-Color, 24 Bit/Pixel, 16.7M Colors at 1 or 2-Pixels Per Clock
- Laser Trimmed Internal termination Resistors for Optimum Fixed Impedance Matching
- 4x Over-Sampling
- Reduced Ground Bounce Using Time Staggered Pixel Outputs
- Lowest Noise and Best Power Dissipation Using TI PowerPAD™ Packaging

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