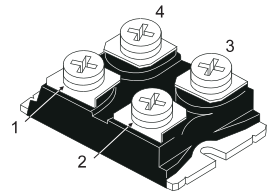
# STE88N65M5

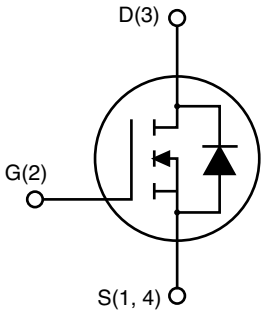
## N-channel 650 V, 0.024 Ω typ., 88 A, MDmesh™ V Power MOSFET in a ISOTOP™ package

**Datasheet - production data**




**ISOTOP™**

**Figure 1. Internal schematic diagram**




## Features

| Order code | $V_{DS}$ @$T_{jmax}$ | $R_{DS(on)}$ max | $I_D$ |
|---|---|---|---|
| STE88N65M5 | 710 V | 0.029 Ω | 88 A |

- Very low $R_{DS(on)}$
- Higher $V_{DSS}$ rating
- Higher dv/dt capability
- Excellent switching performance
- 100% avalanche tested

## Applications

- Switching applications

## Description

This device is an N-channel MDmesh™ V Power MOSFET based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

**Table 1. Device summary**

| Order code | Marking | Packages | Packaging |
|---|---|---|---|
| STE88N65M5 | 88N65M5 | ISOTOP | Tube |

# Contents

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{GS}$ | Gate- source voltage | ± 25 | V |
| $I_D$ | Drain current (continuous) at $T_C$ = 25 °C | 88 | A |
| $I_D$ | Drain current (continuous) at $T_C$ = 100 °C | 55.7 | A |
| $I_{DM}$ (1) | Drain current (pulsed) | 352 | A |
| $P_{TOT}$ | Total dissipation at $T_C$ = 25 °C | 494 | W |
| $I_{AR}$ | Max current during repetitive or single pulse avalanche (pulse width limited by $T_{JMAX}$) | 15 | A |
| $E_{AS}$ | Single pulse avalanche energy (starting $T_j$ = 25°C, $I_D$ = $I_{AR}$, $V_{DD}$ = 50V) | 2000 | mJ |
| dv/dt(2) | Peak diode recovery voltage slope | 15 | V/ns |
| $T_{stg}$ | Storage temperature | - 55 to 150 | °C |
| $T_j$ | Max. operating junction temperature | 150 | °C |

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq$ 88 A, di/dt = 400 A/$\mu$s, $V_{DD}$ = 400 V, $V_{DS\ (peak)} < V_{(BR)DSS}$.

**Table 3. Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{thj\text{-}case}$ | Thermal resistance junction-case max | 0.253 | °C/W |
| $R_{thj\text{-}amb}$ | Thermal resistance junction-ambient max | 30 | °C/W |

# 2 Electrical characteristics

($T_C$ = 25 °C unless otherwise specified)

**Table 4. On /off states**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $I_D$ = 1 mA, $V_{GS}$ = 0 | 650 | | | V |
| $I_{DSS}$ | Zero gate voltage drain current ($V_{GS}$ = 0) | $V_{DS}$ = 650 V | | | 1 | µA |
| | | $V_{DS}$ = 650 V, $T_C$=125 °C | | | 100 | µA |
| $I_{GSS}$ | Gate-body leakage current ($V_{DS}$ = 0) | $V_{GS}$ = ± 25 V | | | ±100 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 3 | 4 | 5 | V |
| $R_{DS(on)}$ | Static drain-source on- resistance | $V_{GS}$ = 10 V, $I_D$ = 42 A | | 0.024 | 0.029 | Ω |

**Table 5. Dynamic**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $C_{iss}$ | Input capacitance | $V_{DS}$ = 100 V, f = 1 MHz, $V_{GS}$ = 0 | - | 8825 | - | pF |
| $C_{oss}$ | Output capacitance | | - | 223 | - | pF |
| $C_{rss}$ | Reverse transfer capacitance | | - | 11 | - | pF |
| $C_{o(tr)}$(1) | Equivalent capacitance time related | $V_{GS}$ = 0, $V_{DS}$ = 0 to 520 V | - | 778 | - | pF |
| $C_{o(er)}$(2) | Equivalent capacitance energy related | $V_{GS}$ = 0, $V_{DS}$ = 0 to 520 V | - | 202 | - | pF |
| $R_G$ | Intrinsic gate resistance | f = 1 MHz open drain | - | 1.79 | - | Ω |
| $Q_g$ | Total gate charge | $V_{DD}$ = 520 V, $I_D$ = 42 A, $V_{GS}$ = 10 V (see *Figure 16*) | - | 204 | - | nC |
| $Q_{gs}$ | Gate-source charge | | - | 51 | - | nC |
| $Q_{gd}$ | Gate-drain charge | | - | 84 | - | nC |

1. $C_{o(tr)}$ is a constant capacitance value that gives the same charging time as $C_{oss}$ while $V_{DS}$ is rising from 0 to 80% $V_{DSS}$.
2. $C_{o(er)}$ is a constant capacitance value that gives the same stored energy as $C_{oss}$ while $V_{DS}$ is rising from 0 to 80% $V_{DSS}$.

**Table 6. Switching times**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(v)}$ | Voltage delay time | $V_{DD}$ = 400 V, $I_D$ = 56 A, $R_G$ = 4.7 Ω, $V_{GS}$ = 10 V (see *Figure 17*) (see *Figure 20*) | - | 141 | - | ns |
| $t_{r(v)}$ | Voltage rise time | | - | 16 | - | ns |
| $t_{f(i)}$ | Current fall time | | - | 29 | - | ns |
| $t_{c(off)}$ | Crossing time | | - | 56 | - | ns |

**Table 7. Source drain diode**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$ | Source-drain current | | - | | 88 | A |
| $I_{SDM}$ (1) | Source-drain current (pulsed) | | - | | 352 | A |
| $V_{SD}$ (2) | Forward on voltage | $I_{SD}$ = 88 A, $V_{GS}$ = 0 | - | | 1.5 | V |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 84 A, di/dt = 100 A/µs $V_{DD}$ = 100 V (see *Figure 17*) | - | 544 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 14 | | µC |
| $I_{RRM}$ | Reverse recovery current | | - | 50 | | A |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 84 A, di/dt = 100 A/µs $V_{DD}$ = 100 V, $T_j$ = 150 °C (see *Figure 17*) | - | 660 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 20 | | µC |
| $I_{RRM}$ | Reverse recovery current | | - | 60 | | A |

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

**Figure 2. Safe operating area**

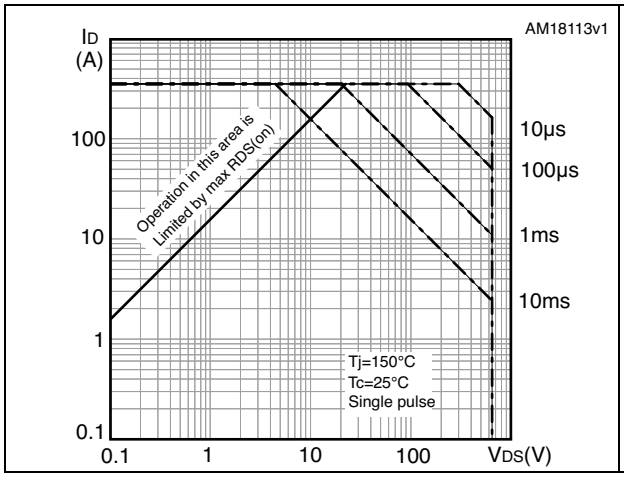



**Figure 3. Thermal impedance**

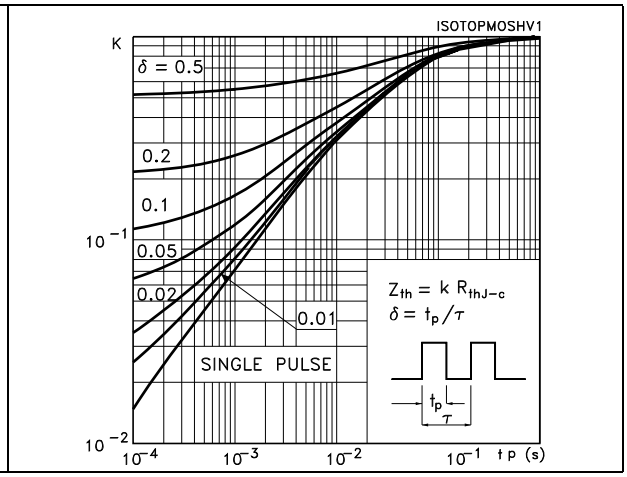



**Figure 4. Output characteristics**

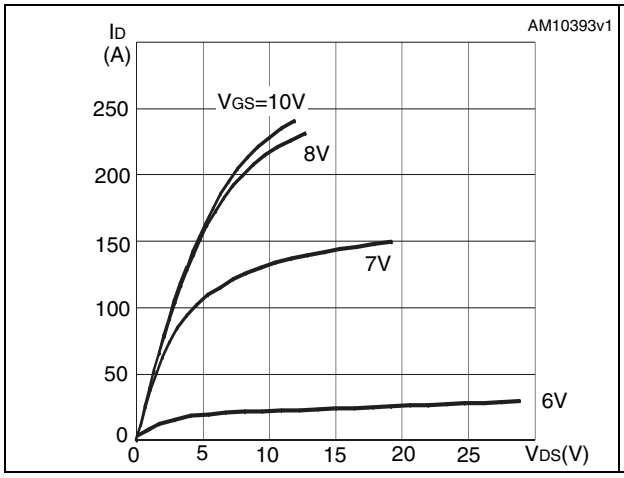



**Figure 5. Transfer characteristics**

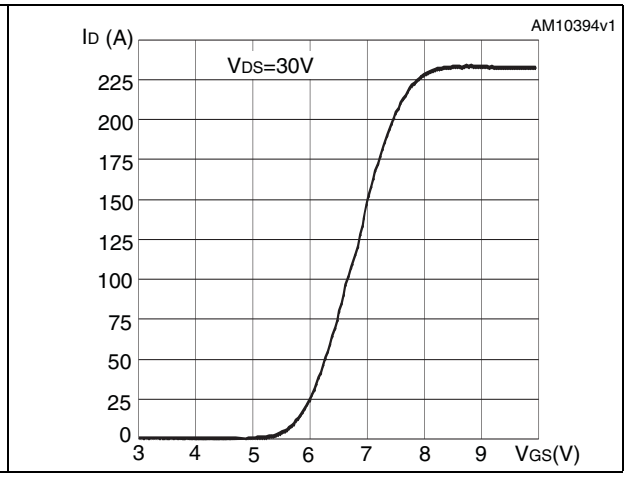



**Figure 6. Normalized $V_{(BR)DSS}$ vs temperature**

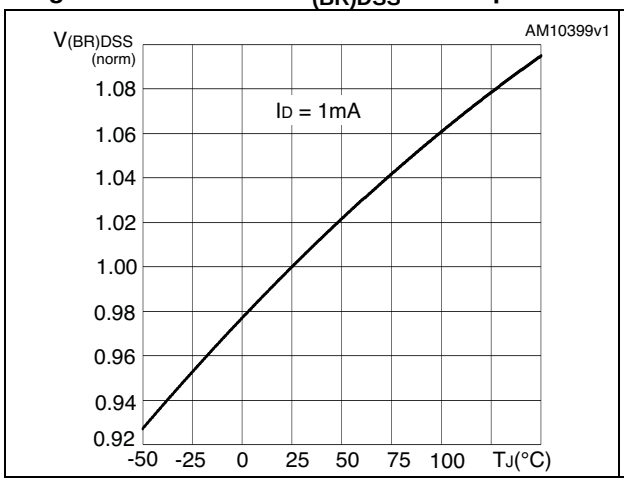



**Figure 7. Static drain-source on-resistance**

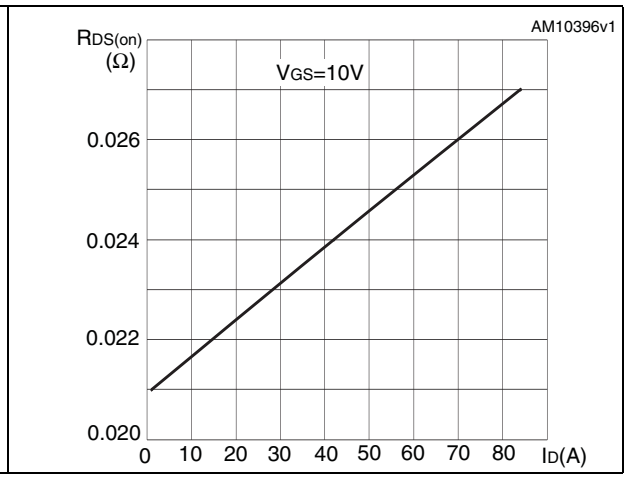


**Figure 8. Gate charge vs gate-source voltage**

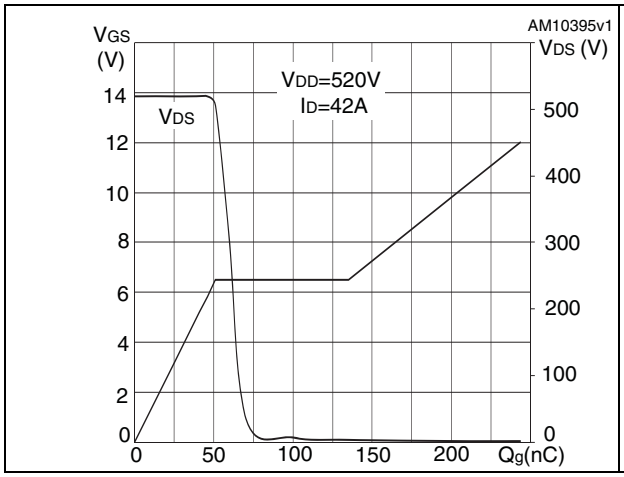



**Figure 9. Capacitance variations**

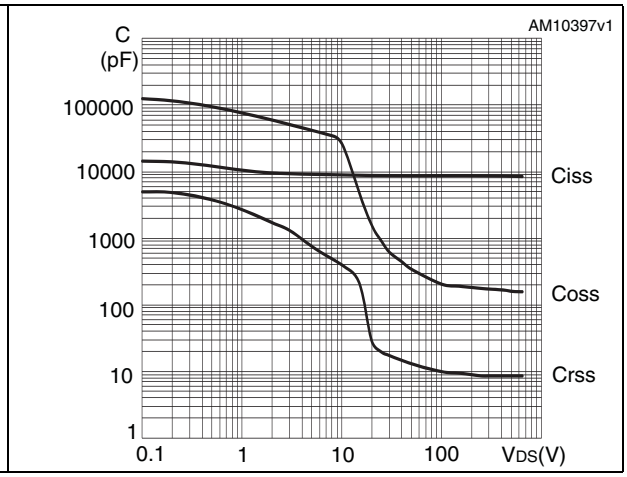



**Figure 10. Normalized gate threshold voltage vs temperature**

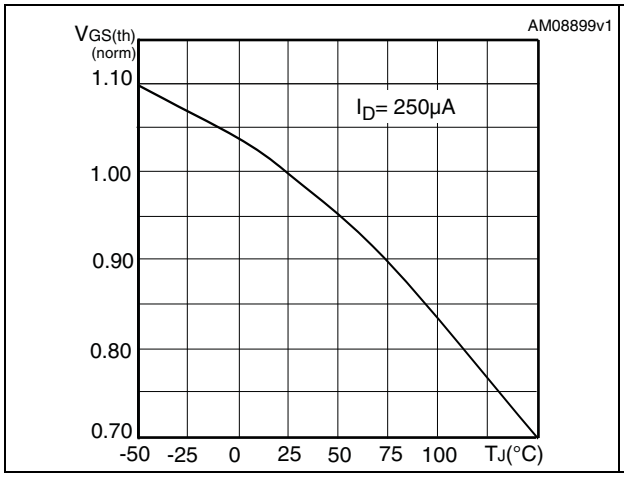



**Figure 11. Normalized on-resistance vs temperature**

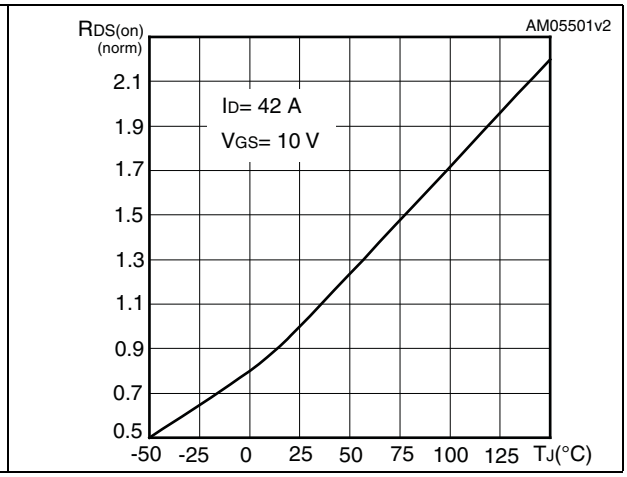



**Figure 12. Source-drain diode forward characteristics**

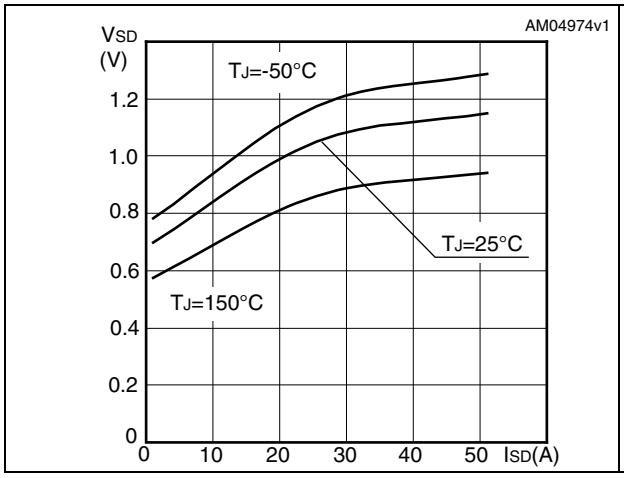



**Figure 13. Output capacitance stored energy**

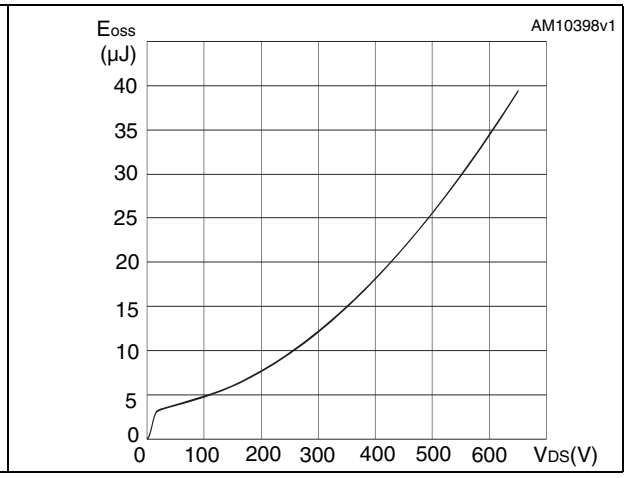
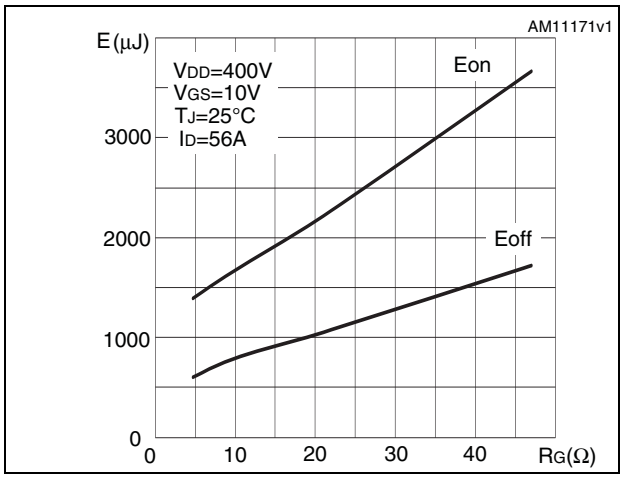


**Figure 14. Switching losses vs gate resistance (1)**




1. Eon including reverse recovery of a SiC diode.

# 3 Test circuits

**Figure 15. Switching times test circuit for resistive load**

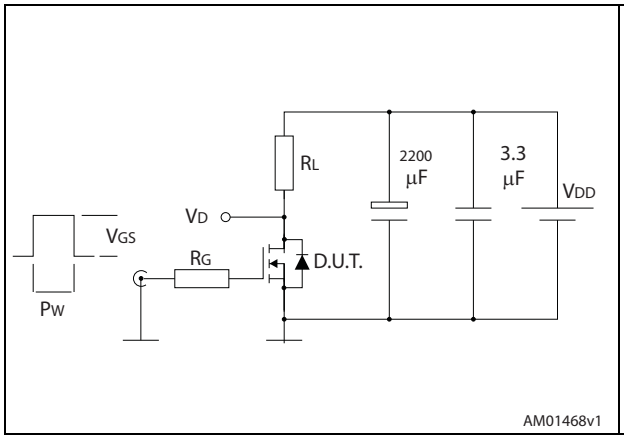



**Figure 16. Gate charge test circuit**

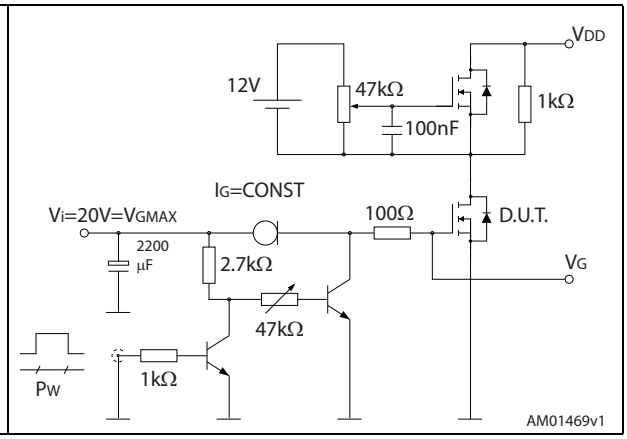



**Figure 17. Test circuit for inductive load switching and diode recovery times**

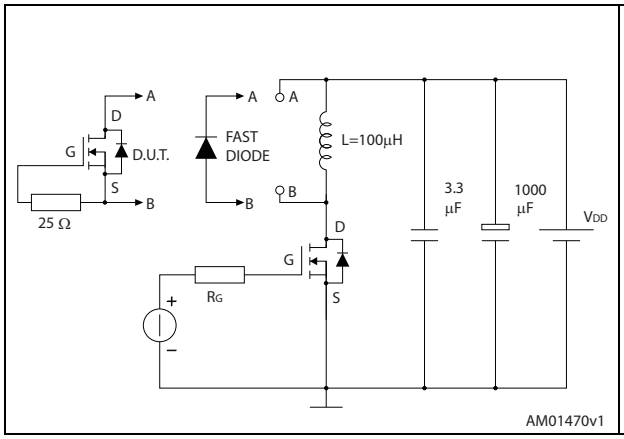



**Figure 18. Unclamped inductive load test circuit**

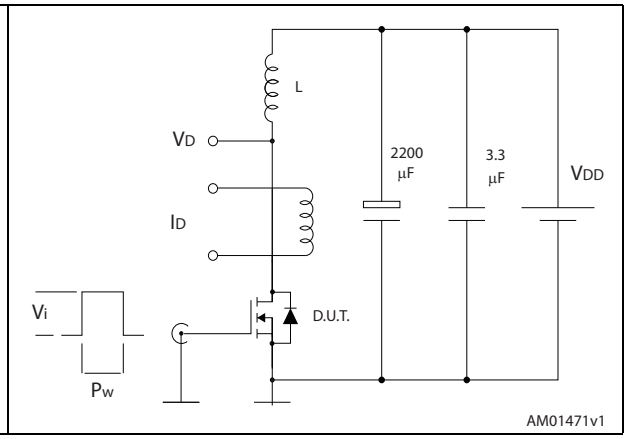



**Figure 19. Unclamped inductive waveform**

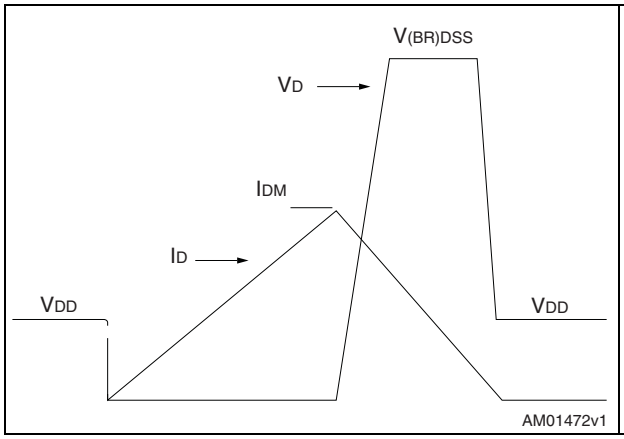
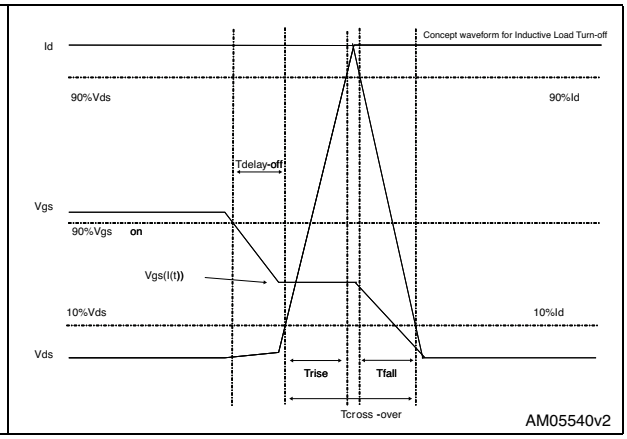



**Figure 20. Switching time waveform**



# 4 Package mechanical data

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**Figure 21. ISOTOP drawing**

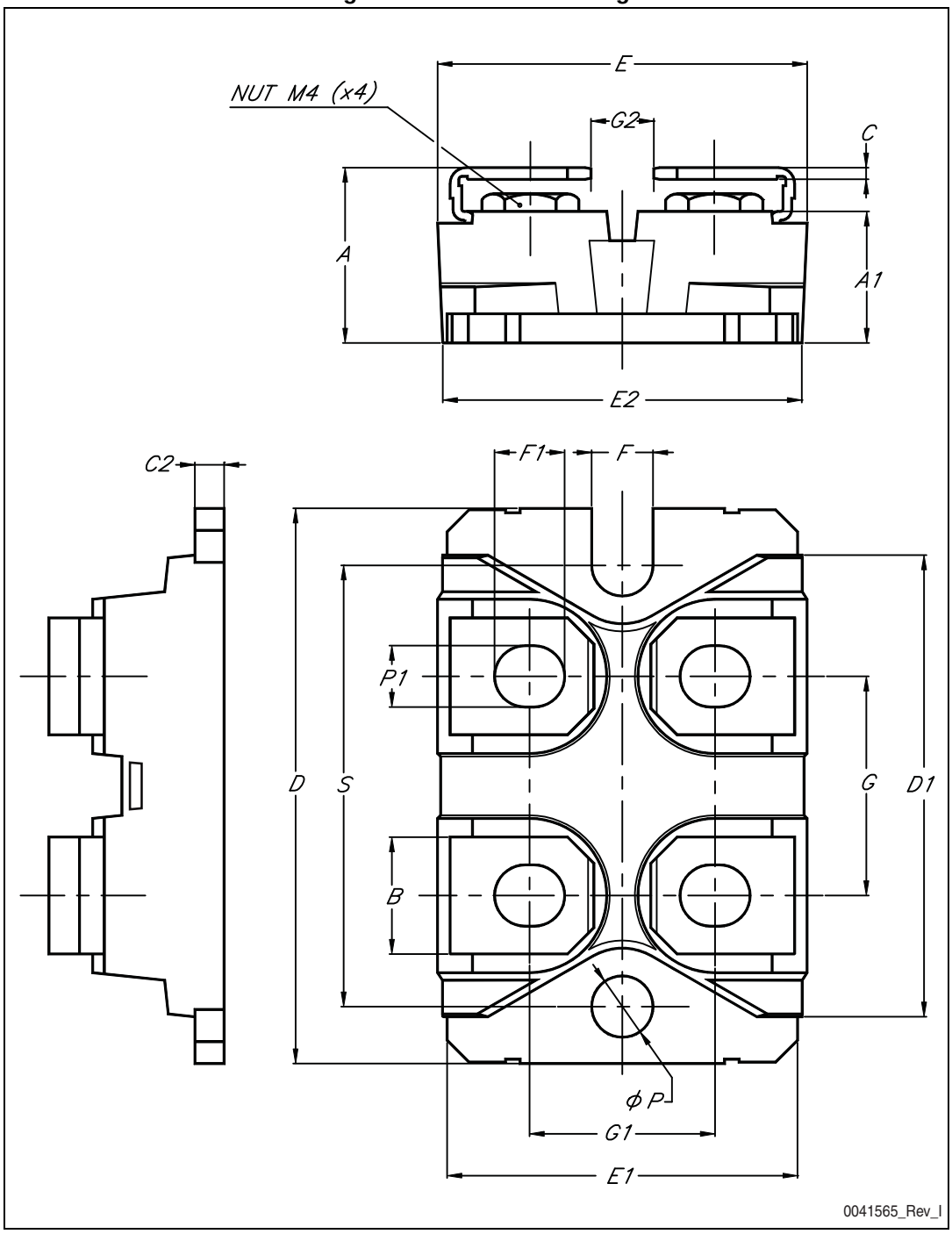

Table 8. ISOTOP mechanical data

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 11.80 | | 12.20 |
| A1 | 8.90 | | 9.10 |
| B | 7.80 | | 8.20 |
| C | 0.75 | | 0.85 |
| C2 | 1.95 | | 2.05 |
| D | 37.80 | | 38.20 |
| D1 | 31.50 | | 31.70 |
| E | 25.15 | | 25.50 |
| E1 | 23.85 | | 24.15 |
| E2 | | 24.80 | |
| G | 14.90 | | 15.10 |
| G1 | 12.60 | | 12.80 |
| G2 | 3.50 | | 4.30 |
| F | 4.10 | | 4.30 |
| F1 | 4.60 | | 5 |
| ϕP | 4 | | 4.30 |
| P1 | 4 | | 4.40 |
| S | 30.10 | | 30.30 |

# 5 Revision history

Table 9. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 24-Feb-2014 | 1 | Initial release. |

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