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April 1st, 2010
Renesas Electronics Corporation

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1. Overview

1.1 Features

The R8C/36E Group, R8C/36F Group, R8C/36G Group, and R8C/36H Group of single-chip MCUs incorporate the R8C/Tiny Series CPU core, employing sophisticated instructions for a high level of efficiency. With 1 Mbyte of address space, and it is capable of executing instructions at high speed. In addition, the CPU core boasts a multiplier for high-speed operation processing.
Power consumption is low, and the supported operating modes allow additional power control. These MCUs are designed to maximize EMI/EMS performance.
Integration of many peripheral functions, including multifunction timer and serial interface, reduces the number of system components.
The R8C/36E Group and R8C/36F Group have a single channel CAN module and are suitable for LAN systems in vehicles and for FA.
The R8C/36G Group and the R8C/36H Group do not have CAN modules.
The R8C/36E Group and the R8C/36G Group have data flash (1 KB × 4 blocks) with the background operation (BGO) function.

1.1.1 Applications

Automobiles and others

1.1.2 Specifications

Tables 1.1 and 1.2 outline the Specifications for R8C/36E Group, tables 1.3 and 1.4 outline the Specifications for R8C/36F Group, tables 1.5 and 1.6 outline the Specifications for R8C/36G Group, tables 1.7 and 1.8 outline the Specifications for R8C/36H Group.

Table 1.1 Specifications for R8C/36E Group (1)

Item	Function	Specification
CPU	Central processing unit	R8C/Tiny series core • Number of fundamental instructions: 89 • Minimum instruction execution time: 50 ns (f(XIN) = 20 MHz, VCC = 2.7 to 5.5 V) • Multiplier: 16 bits × 16 bits → 32 bits • Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits • Operation mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM, RAM, Data flash	Refer to **Table 1.9 Product List for R8C/36E Group**.
Power Supply Voltage Detection	Voltage detection circuit	• Power-on reset • Voltage detection 3 (detection level of voltage detection 1 selectable)
I/O Ports	Programmable I/O ports	• Input-only: 1 pin • CMOS I/O ports: 59, selectable pull-up resistor
Clock	Clock generation circuits	3 circuits: XIN clock oscillation circuit (with on-chip feedback resistor), High-speed on-chip oscillator (with frequency adjustment function), Low-speed on-chip oscillator • Oscillation stop detection: XIN clock oscillation stop detection function • Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16 • Low power consumption modes: Standard operating mode (high-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode
Interrupts		• Interrupt Vectors: 69 • External: 9 sources ($\overline{\text{INT}}$ × 5 , key input × 4) • Priority levels: 7 levels
Watchdog Timer		• 15 bits × 1 (with prescaler) • Reset start selectable • Low-speed on-chip oscillator for watchdog timer selectable
DTC (Data Transfer Controller)		• 1 channel • Activation sources: 40 • Transfer modes: 2 (normal mode, repeat mode)
Timer	Timer RA0 Timer RA1	8 bits (with 8-bit prescaler) Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RB	8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timer RC	16 bits × 1 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin)
	Timer RD	16 bits × 2 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output 6 pins), reset synchronous PWM mode (output three-phase waveforms (6 pins), sawtooth wave modulation), complementary PWM mode (output three-phase waveforms (6 pins), triangular wave modulation), PWM3 mode (PWM output 2 pins with fixed period)
	Timer RE	8 bits × 1 Output compare mode
	Timer RF	16 bits × 1 Input capture mode (input capture circuit), output compare mode (output compare circuit)

Table 1.2 Specifications for R8C/36E Group (2)

Item	Function	Specification
Timer	Timer RG	16 bits × 1 Timer mode (input capture function, output compare function), PWM mode (output 1 pin), phase counting mode (available automatic measurement for the counts of 2-phase encoder)
Serial Interface	UART0, 1	Clock synchronous serial I/O/UART × 2 channel
	UART2	Clock synchronous serial I/O, UART, I²C mode (I²C-bus), IE mode (IE BUS (1)), multiprocessor communication function
Synchronous Serial Communication Unit (SSU)		1
LIN Module		Hardware LIN: 2 (timer RA0, timer RA1, UART0, UART1)
CAN module		One channel, 16 Mailboxes (conforms to the ISO 11898-1)
A/D Converter		10-bit resolution × 16 channels, includes sample and hold function, with sweep mode
Flash Memory		• Programming and erasure voltage: VCC = 2.7 to 5.5 V • Programming and erasure endurance: 10,000 times (data flash) 1,000 times (program ROM) • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function • Background operation (BGO) function (data flash)
Operating Frequency/Supply Voltage		f(XIN) = 20 MHz (VCC = 2.7 to 5.5 V)
Current consumption		TBD (VCC = 5.0 V, f(XIN) = 20 MHz) TBD (VCC = 3.0 V, f(XIN) = 20 MHz)
Operating Ambient Temperature		-40 to 85°C (J version) -40 to 125°C (K version) (2)
Package		64-pin LQFP Package code: PLQP0064KB-A (previous code: 64P6Q-A)

Notes:
1. IE BUS is a trademark of NEC Electronics Corporation.
2. Specify the K version if K version functions are to be used.

Table 1.3 Specifications for R8C/36F Group (1)

Item	Function	Specification
CPU	Central processing unit	R8C/Tiny series core • Number of fundamental instructions: 89 • Minimum instruction execution time: 50 ns (f(XIN) = 20 MHz, VCC = 2.7 to 5.5 V) • Multiplier: 16 bits × 16 bits → 32 bits • Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits • Operation mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM, RAM, Data flash	Refer to **Table 1.10 Product List for R8C/36F Group**.
Power Supply Voltage Detection	Voltage detection circuit	• Power-on reset • Voltage detection 3 (detection level of voltage detection 1 selectable)
I/O Ports	Programmable I/O ports	• Input-only: 1 pin • CMOS I/O ports: 59, selectable pull-up resistor
Clock	Clock generation circuits	3 circuits: XIN clock oscillation circuit (with on-chip feedback resistor), High-speed on-chip oscillator (with frequency adjustment function), Low-speed on-chip oscillator • Oscillation stop detection: XIN clock oscillation stop detection function • Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16 • Low power consumption modes: Standard operating mode (high-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode
Interrupts		• Interrupt Vectors: 69 • External: 9 sources ($\overline{\text{INT}}$ × 5 , key input × 4) • Priority levels: 7 levels
Watchdog Timer		• 15 bits × 1 (with prescaler) • Reset start selectable • Low-speed on-chip oscillator for watchdog timer selectable
DTC (Data Transfer Controller)		• 1 channel • Activation sources: 40 • Transfer modes: 2 (normal mode, repeat mode)
Timer	Timer RA0 Timre RA1	8 bits (with 8-bit prescaler) Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RB	8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timer RC	16 bits × 1 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin)
	Timer RD	16 bits × 2 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output 6 pins), reset synchronous PWM mode (output three-phase waveforms (6 pins), sawtooth wave modulation), complementary PWM mode (output three-phase waveforms (6 pins), triangular wave modulation), PWM3 mode (PWM output 2 pins with fixed period)
	Timer RE	8 bits × 1 Output compare mode
	Timer RF	16 bits × 1 Input capture mode (input capture circuit), output compare mode (output compare circuit)
	Timer RG	16 bits × 1 Timer mode (input capture function, output compare function), PWM mode (output 1 pin), phase counting mode (available automatic measurement for the counts of 2-phase encoder)

Table 1.4 Specifications for R8C/36F Group (2)

Item	Function	Specification
Serial Interface	UART0, 1	Clock synchronous serial I/O/UART × 2 channel
	UART2	Clock synchronous serial I/O, UART, I²C mode (I²C-bus), IE mode (IE BUS (1)), multiprocessor communication function
Synchronous Serial Communication Unit (SSU)		1
LIN Module		Hardware LIN: 2 (timer RA0, timer RA1, UART0, UART1)
CAN module		One channel, 16 Mailboxes (conforms to the ISO 11898-1)
A/D Converter		10-bit resolution × 16 channels, includes sample and hold function, with sweep mode
Flash Memory		• Programming and erasure voltage: VCC = 2.7 to 5.5 V • Programming and erasure endurance: 100 times (program ROM) • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function
Operating Frequency/Supply Voltage		f(XIN) = 20 MHz (VCC = 2.7 to 5.5 V)
Current consumption		TBD (VCC = 5.0 V, f(XIN) = 20 MHz) TBD (VCC = 3.0 V, f(XIN) = 20 MHz)
Operating Ambient Temperature		-40 to 85°C (J version) -40 to 125°C (K version) (2)
Package		64-pin LQFP Package code: PLQP0064KB-A (previous code: 64P6Q-A)

Notes:
1. IE BUS is a trademark of NEC Electronics Corporation.
2. Specify the K version if K version functions are to be used.

Table 1.5 Specifications for R8C/36G Group (1)

Item	Function	Specification
CPU	Central processing unit	R8C/Tiny series core • Number of fundamental instructions: 89 • Minimum instruction execution time: 50 ns (f(XIN) = 20 MHz, VCC = 2.7 to 5.5 V) • Multiplier: 16 bits × 16 bits → 32 bits • Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits • Operation mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM, RAM, Data flash	Refer to **Table 1.11 Product List for R8C/36G Group**.
Power Supply Voltage Detection	Voltage detection circuit	• Power-on reset • Voltage detection 3 (detection level of voltage detection 1 selectable)
I/O Ports	Programmable I/O ports	• Input-only: 1 pin • CMOS I/O ports: 59, selectable pull-up resistor
Clock	Clock generation circuits	3 circuits: XIN clock oscillation circuit (with on-chip feedback resistor), High-speed on-chip oscillator (with frequency adjustment function), Low-speed on-chip oscillator • Oscillation stop detection: XIN clock oscillation stop detection function • Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16 • Low power consumption modes: Standard operating mode (high-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode
Interrupts		• Interrupt Vectors: 69 • External: 9 sources ($\overline{\text{INT}}$ × 5 , key input × 4) • Priority levels: 7 levels
Watchdog Timer		• 15 bits × 1 (with prescaler) • Reset start selectable • Low-speed on-chip oscillator for watchdog timer selectable
DTC (Data Transfer Controller)		• 1 channel • Activation sources: 40 • Transfer modes: 2 (normal mode, repeat mode)
Timer	Timer RA0 Timre RA1	8 bits (with 8-bit prescaler) Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RB	8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timer RC	16 bits × 1 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin)
	Timer RD	16 bits × 2 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output 6 pins), reset synchronous PWM mode (output three-phase waveforms (6 pins), sawtooth wave modulation), complementary PWM mode (output three-phase waveforms (6 pins), triangular wave modulation), PWM3 mode (PWM output 2 pins with fixed period)
	Timer RE	8 bits × 1 Output compare mode
	Timer RF	16 bits × 1 Input capture mode (input capture circuit), output compare mode (output compare circuit)
	Timer RG	16 bits × 1 Timer mode (input capture function, output compare function), PWM mode (output 1 pin), phase counting mode (available automatic measurement for the counts of 2-phase encoder)

Table 1.6 Specifications for R8C/36G Group (2)

Item	Function	Specification
Serial Interface	UART0, 1	Clock synchronous serial I/O/UART × 2 channel
	UART2	Clock synchronous serial I/O, UART, I²C mode (I²C-bus), IE mode (IE BUS (1)), multiprocessor communication function
Synchronous Serial Communication Unit (SSU)		1
LIN Module		Hardware LIN: 2 (timer RA0, timer RA1, UART0, UART1)
A/D Converter		10-bit resolution × 16 channels, includes sample and hold function, with sweep mode
Flash Memory		• Programming and erasure voltage: VCC = 2.7 to 5.5 V • Programming and erasure endurance: 10,000 times (data flash) 1,000 times (program ROM) • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function • Background operation (BGO) function (data flash)
Operating Frequency/Supply Voltage		f(XIN) = 20 MHz (VCC = 2.7 to 5.5 V)
Current consumption		TBD (VCC = 5.0 V, f(XIN) = 20 MHz) TBD (VCC = 3.0 V, f(XIN) = 20 MHz)
Operating Ambient Temperature		-40 to 85°C (J version) -40 to 125°C (K version) (2)
Package		64-pin LQFP Package code: PLQP0064KB-A (previous code: 64P6Q-A)

Notes:
1. IE BUS is a trademark of NEC Electronics Corporation.
2. Specify the K version if K version functions are to be used.

Table 1.7 Specifications for R8C/36H Group (1)

Item	Function	Specification
CPU	Central processing unit	R8C/Tiny series core • Number of fundamental instructions: 89 • Minimum instruction execution time: 50 ns (f(XIN) = 20 MHz, VCC = 2.7 to 5.5 V) • Multiplier: 16 bits × 16 bits → 32 bits • Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits • Operation mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM, RAM, Data flash	Refer to **Table 1.12 Product List for R8C/36H Group**.
Power Supply Voltage Detection	Voltage detection circuit	• Power-on reset • Voltage detection 3 (detection level of voltage detection 1 selectable)
I/O Ports	Programmable I/O ports	• Input-only: 1 pin • CMOS I/O ports: 59, selectable pull-up resistor
Clock	Clock generation circuits	3 circuits: XIN clock oscillation circuit (with on-chip feedback resistor), High-speed on-chip oscillator (with frequency adjustment function), Low-speed on-chip oscillator • Oscillation stop detection: XIN clock oscillation stop detection function • Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16 • Low power consumption modes: Standard operating mode (high-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode
Interrupts		• Interrupt Vectors: 69 • External: 9 sources ($\overline{\text{INT}}$ × 5 , key input × 4) • Priority levels: 7 levels
Watchdog Timer		• 15 bits × 1 (with prescaler) • Reset start selectable • Low-speed on-chip oscillator for watchdog timer selectable
DTC (Data Transfer Controller)		• 1 channel • Activation sources: 40 • Transfer modes: 2 (normal mode, repeat mode)
Timer	Timer RA0 Timer RA1	8 bits (with 8-bit prescaler) Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RB	8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timer RC	16 bits × 1 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin)
	Timer RD	16 bits × 2 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output 6 pins), reset synchronous PWM mode (output three-phase waveforms (6 pins), sawtooth wave modulation), complementary PWM mode (output three-phase waveforms (6 pins), triangular wave modulation), PWM3 mode (PWM output 2 pins with fixed period)
	Timer RE	8 bits × 1 Output compare mode
	Timer RF	16 bits × 1 Input capture mode (input capture circuit), output compare mode (output compare circuit)
	Timer RG	16 bits × 1 Timer mode (input capture function, output compare function), PWM mode (output 1 pin), phase counting mode (available automatic measurement for the counts of 2-phase encoder)

Table 1.8 Specifications for R8C/36H Group (2)

Item	Function	Specification
Serial Interface	UART0, 1	Clock synchronous serial I/O/UART × 2 channel
	UART2	Clock synchronous serial I/O, UART, I²C mode (I²C-bus), IE mode (IE BUS (1)), multiprocessor communication function
Synchronous Serial Communication Unit (SSU)		1
LIN Module		Hardware LIN: 2 (timer RA0, timer RA1, UART0, UART1)
A/D Converter		10-bit resolution × 16 channels, includes sample and hold function, with sweep mode
Flash Memory		• Programming and erasure voltage: VCC = 2.7 to 5.5 V • Programming and erasure endurance: 100 times (program ROM) • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function
Operating Frequency/Supply Voltage		f(XIN) = 20 MHz (VCC = 2.7 to 5.5 V)
Current consumption		TBD (VCC = 5.0 V, f(XIN) = 20 MHz) TBD (VCC = 3.0 V, f(XIN) = 20 MHz)
Operating Ambient Temperature		-40 to 85°C (J version) -40 to 125°C (K version) (2)
Package		64-pin LQFP Package code: PLQP0064KB-A (previous code: 64P6Q-A)

Notes:
1. IE BUS is a trademark of NEC Electronics Corporation.
2. Specify the K version if K version functions are to be used.

1.2 Product List

Table 1.9 lists Product List for R8C/36E Group, Table 1.10 lists Product List for R8C/36F Group, Table 1.11 lists Product List for R8C/36G Group, Table 1.12 lists Product List for R8C/36H Group.

Table 1.9 Product List for R8C/36E Group **Current of Apr. 2008**

Part No.	ROM Capacity		RAM Capacity	Package Type	Remarks
	Program ROM	Data flash			
R5F21368EJFP (D)	64 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064KB-A	J version
R5F2136AEJFP (D)	96 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064KB-A	
R5F2136CEJFP (D)	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064KB-A	
R5F21368EKFP (D)	64 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064KB-A	K version
R5F2136AEKFP (D)	96 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064KB-A	
R5F2136CEKFP (D)	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064KB-A	

(D): Under development

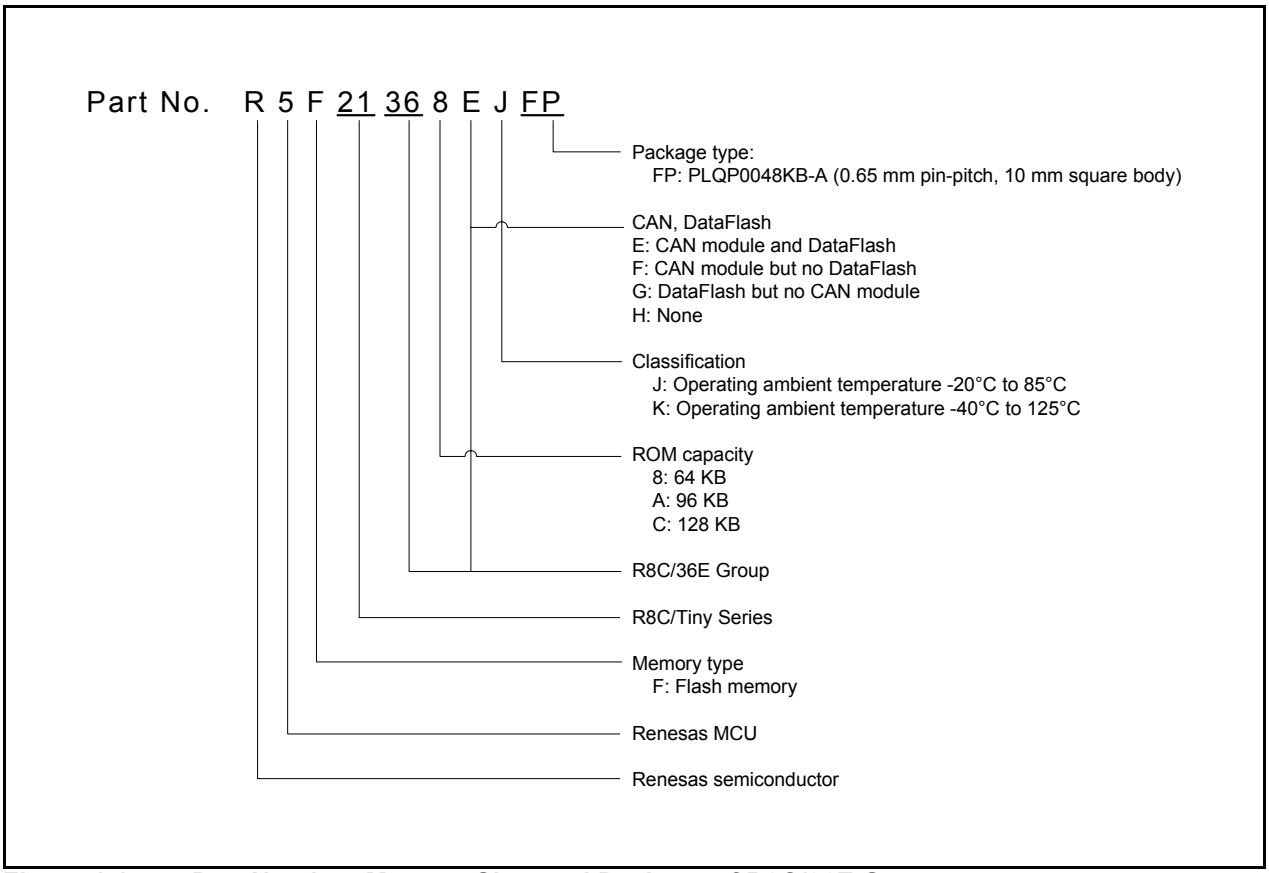


Figure 1.1 Part Number, Memory Size, and Package of R8C/36E Group

Table 1.10 Product List for R8C/36F Group **Current of Apr. 2008**

Part No.	ROM Capacity Program ROM	RAM Capacity	Package Type	Remarks
R5F21368FJFP (D)	64 Kbytes	6 Kbytes	PLQP0064KB-A	J version
R5F2136AFJFP (D)	96 Kbytes	8 Kbytes	PLQP0064KB-A	
R5F2136CFJFP (D)	128 Kbytes	10 Kbytes	PLQP0064KB-A	
R5F21368FKFP (D)	64 Kbytes	6 Kbytes	PLQP0064KB-A	K version
R5F2136AFKFP (D)	96 Kbytes	8 Kbytes	PLQP0064KB-A	
R5F2136CFKFP (D)	128 Kbytes	10 Kbytes	PLQP0064KB-A	

(D): Under development

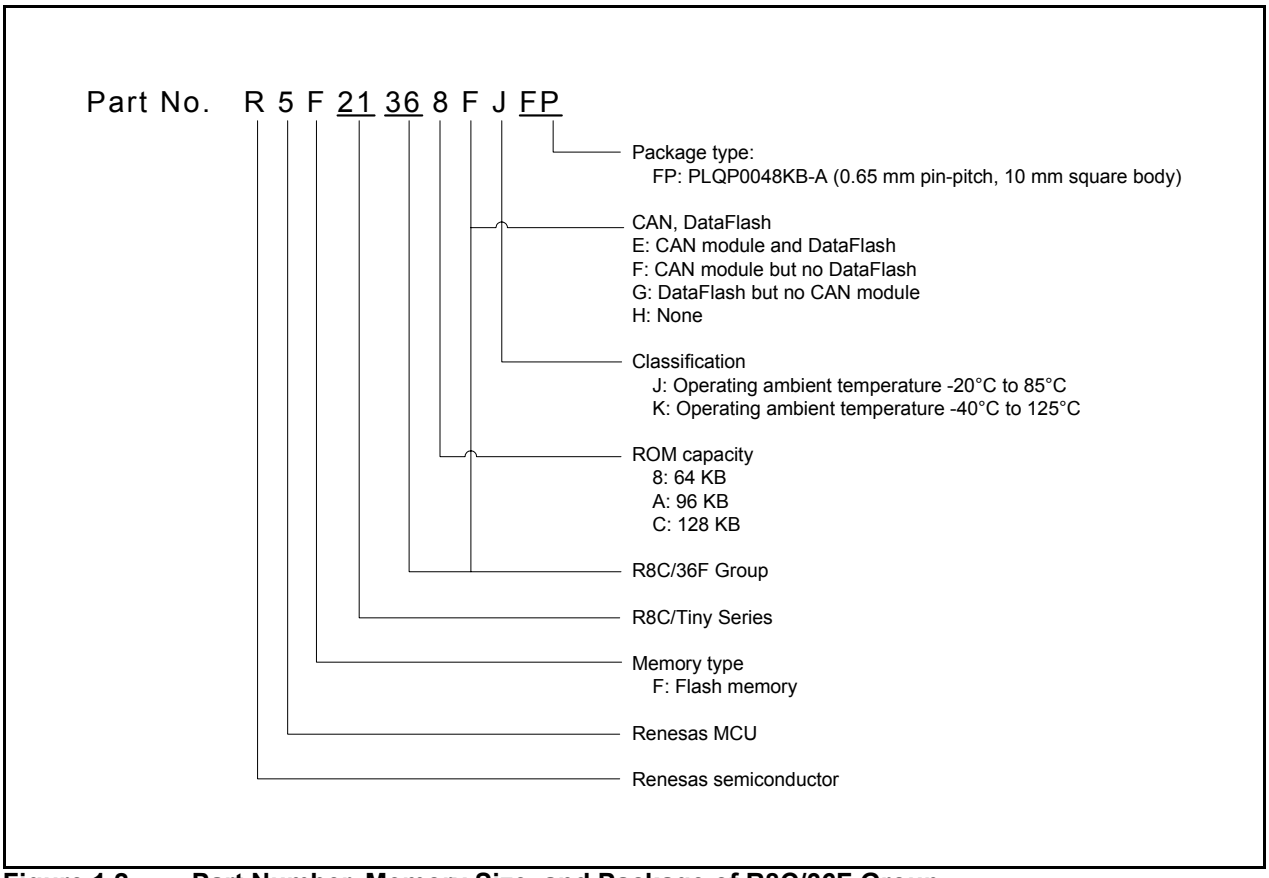


Figure 1.2 Part Number, Memory Size, and Package of R8C/36F Group

Table 1.11 Product List for R8C/36G Group **Current of Apr. 2008**

Part No.	ROM Capacity		RAM Capacity	Package Type	Remarks
	Program ROM	Data flash			
R5F21368GJFP (D)	64 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064KB-A	J version
R5F2136AGJFP (D)	96 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064KB-A	
R5F2136CGJFP (D)	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064KB-A	
R5F21368GKFP (D)	64 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064KB-A	K version
R5F2136AGKFP (D)	96 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064KB-A	
R5F2136CGKFP (D)	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064KB-A	

(D): Under development

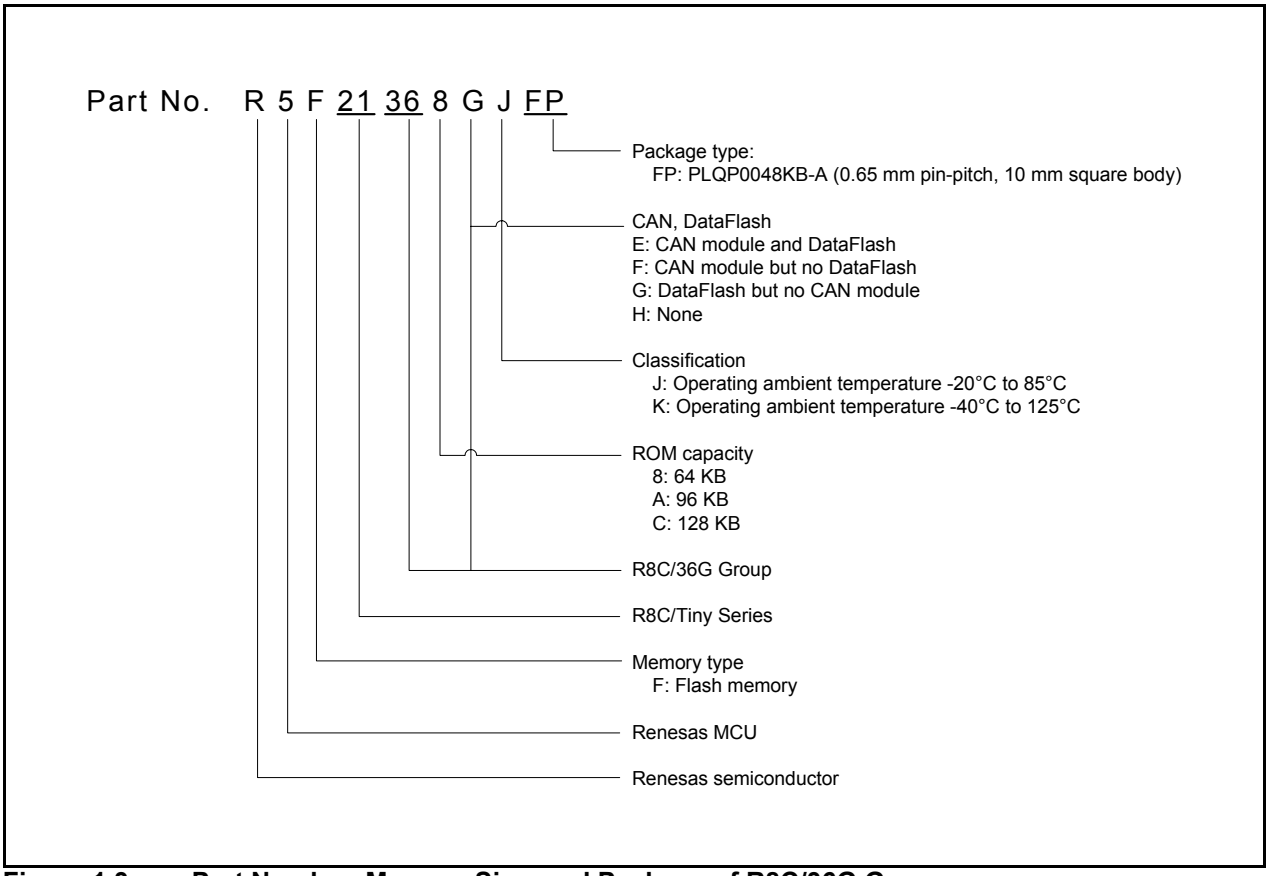


Figure 1.3 Part Number, Memory Size, and Package of R8C/36G Group

Table 1.12 Product List for R8C/36H Group **Current of Apr. 2008**

Part No.	ROM Capacity Program ROM	RAM Capacity	Package Type	Remarks
R5F21368HJFP (D)	64 Kbytes	6 Kbytes	PLQP0064KB-A	J version
R5F2136AHJFP (D)	96 Kbytes	8 Kbytes	PLQP0064KB-A	
R5F2136CHJFP (D)	128 Kbytes	10 Kbytes	PLQP0064KB-A	
R5F21368HKFP (D)	64 Kbytes	6 Kbytes	PLQP0064KB-A	K version
R5F2136AHKFP (D)	96 Kbytes	8 Kbytes	PLQP0064KB-A	
R5F2136CHKFP (D)	128 Kbytes	10 Kbytes	PLQP0064KB-A	

(D): Under development

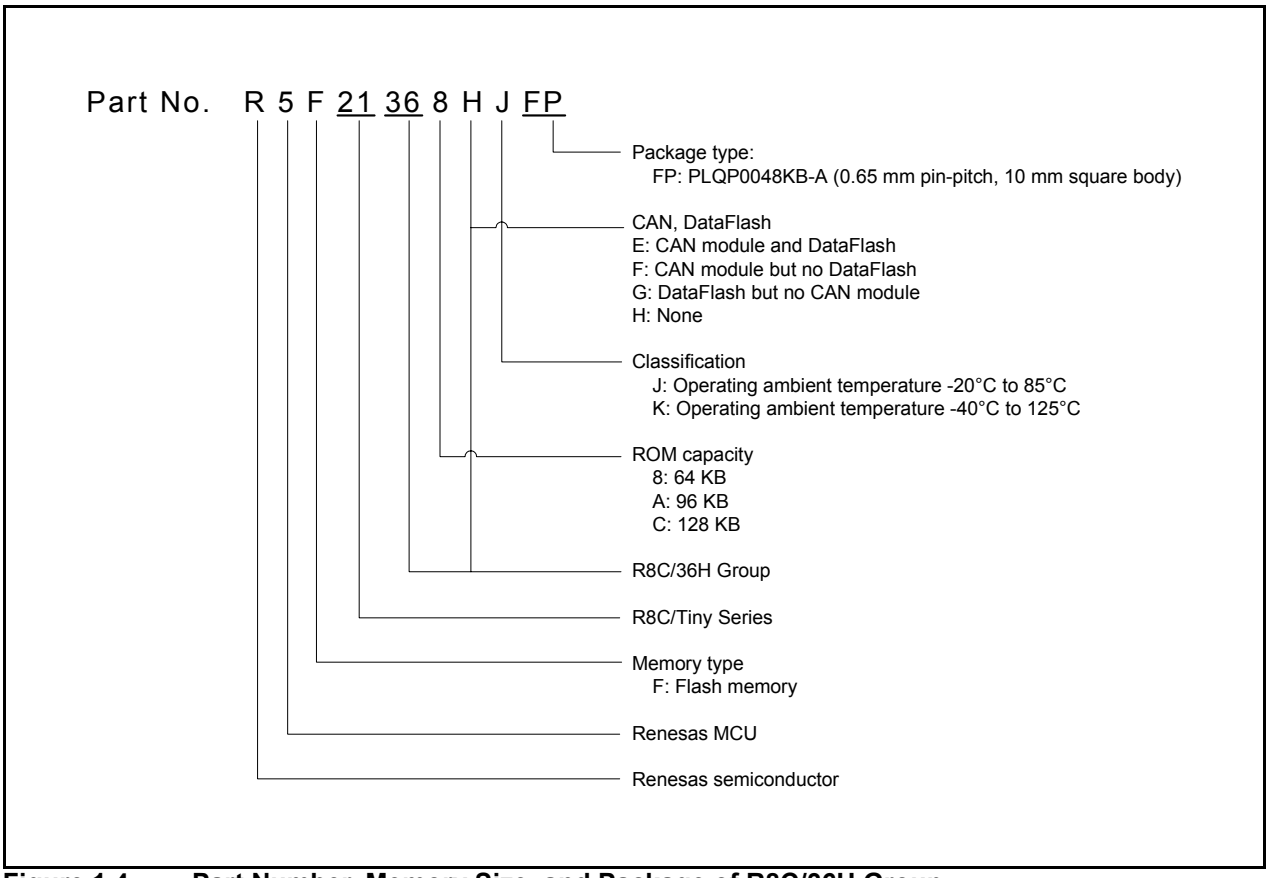


Figure 1.4 Part Number, Memory Size, and Package of R8C/36H Group

1.3 Block Diagram

Figure 1.5 shows a Block Diagram.

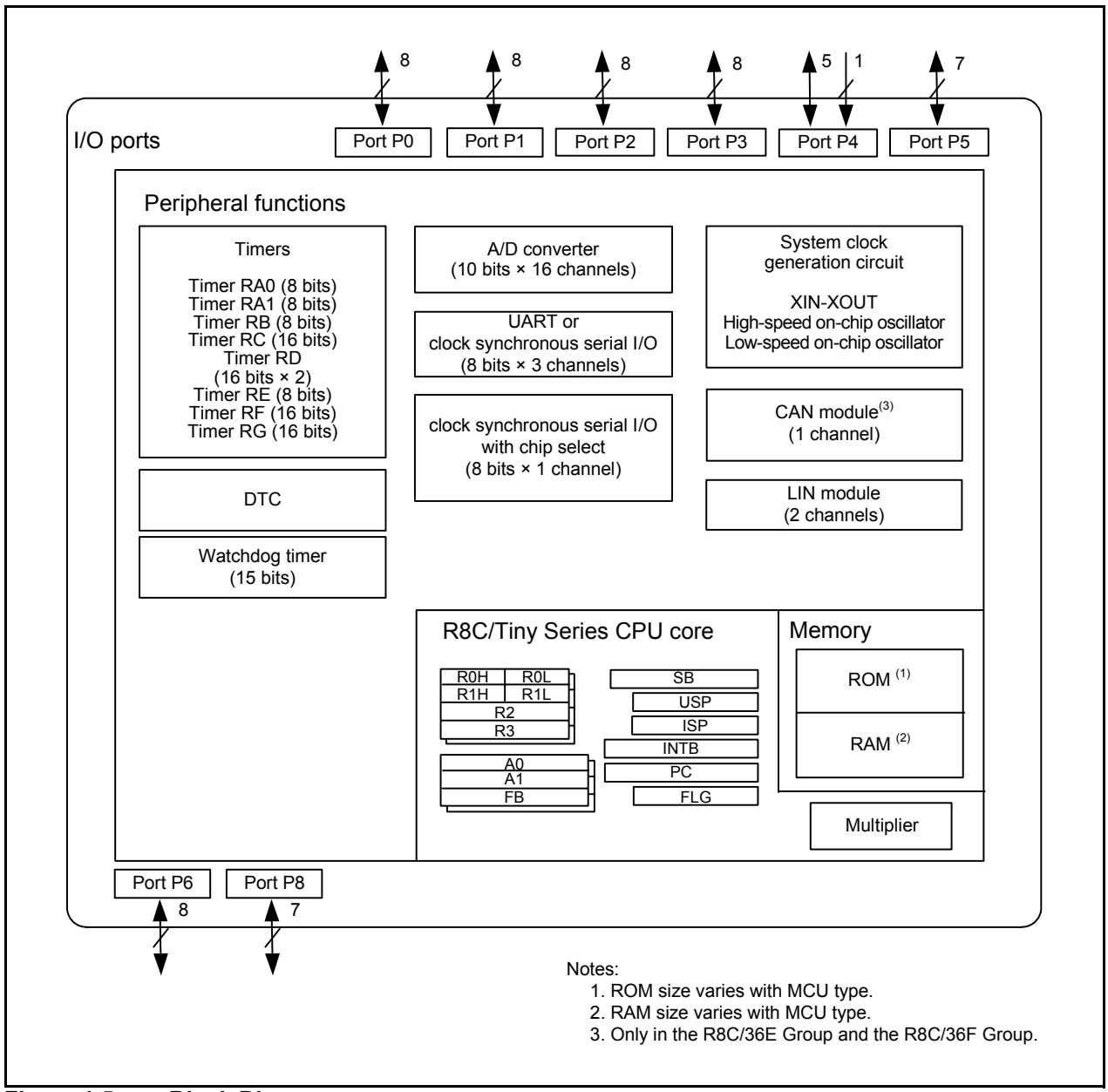
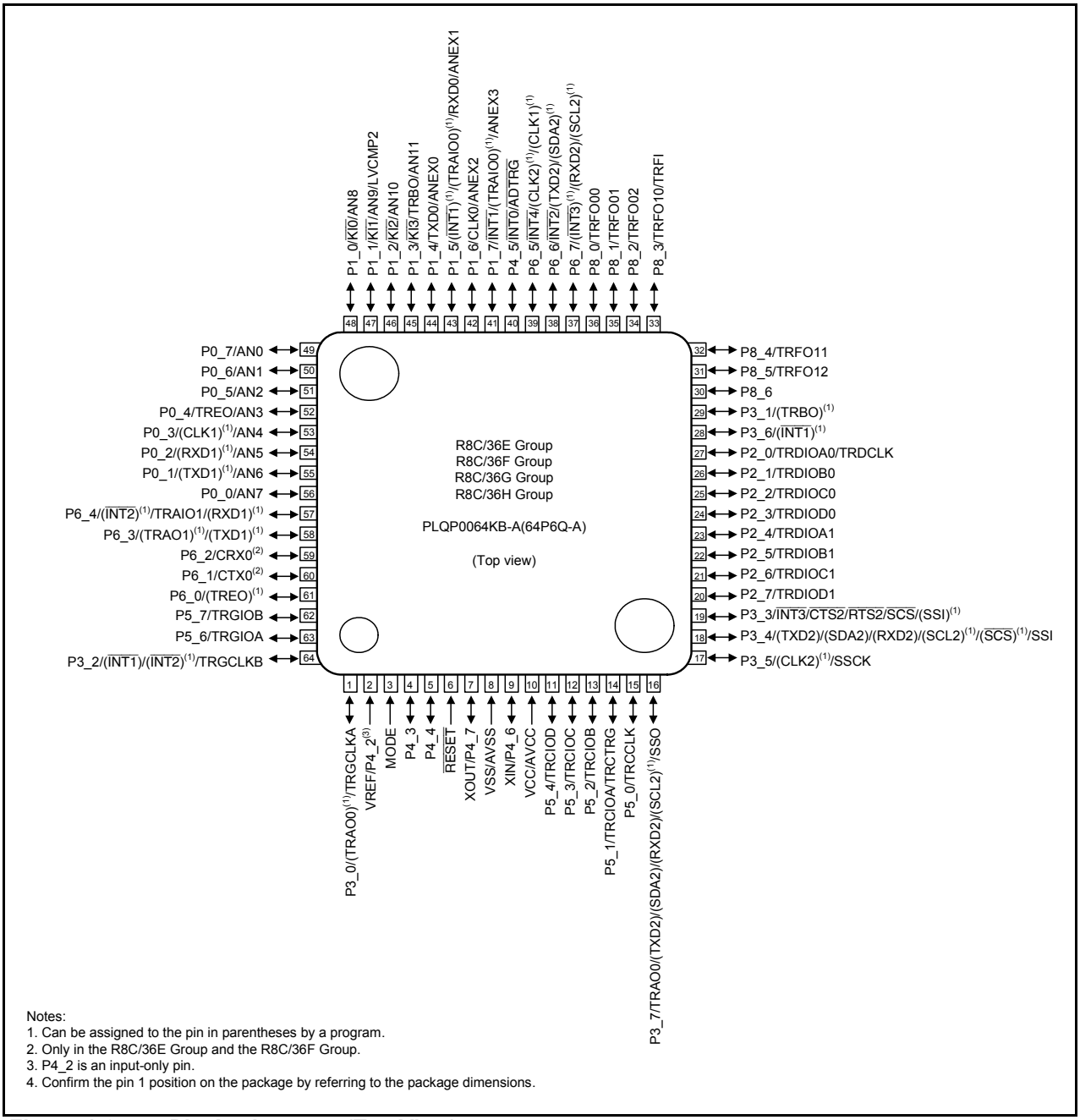


Figure 1.5 Block Diagram

1.4 Pin Assignment

Figure 1.6 shows Pin Assignment (Top View). Tables 1.13 and 1.14 outlines the Pin Name Information by Pin Number.



Notes:
1. Can be assigned to the pin in parentheses by a program.
2. Only in the R8C/36E Group and the R8C/36F Group.
3. P4_2 is an input-only pin.
4. Confirm the pin 1 position on the package by referring to the package dimensions.

Figure 1.6 Pin Assignment (Top View)

Table 1.13 Pin Name Information by Pin Number (1)

Pin Number	Control Pin	Port	I/O Pin Functions for of Peripheral Modules					
			Interrupt	Timer	Serial Interface	Clock Synchronous Serial I/O with Chip Select	CAN Module(2)	A/D Converter Voltage Detection Circuit
1		P3_0		(TRAO0)(1)/ TRGCLKA				
2		P4_2						VREF
3	MODE							
4		P4_3						
5		P4_4						
6	$\overline{\text{RESET}}$							
7	XOUT	P4_7						
8	VSS/AVSS							
9	XIN	P4_6						
10	VCC/AVCC							
11		P5_4		TRCIOD				
12		P5_3		TRCIOC				
13		P5_2		TRCIOB				
14		P5_1		TRCIOA/ TRCTRG				
15		P5_0		TRCCLK				
16		P3_7		TRAO0	(TXD2)/(SDA2)/ (RXD2)/(SCL2)(1)	SSO		
17		P3_5			(CLK2)(1)	SSCK		
18		P3_4			(TXD2)/(SDA2)/ (RXD2)/(SCL2)(1)	($\overline{\text{SCS}}$)(1)/SSI		
19		P3_3	$\overline{\text{INT3}}$		$\overline{\text{CTS2}}/\overline{\text{RTS2}}$	$\overline{\text{SCS}}$/(SSI)(1)		
20		P2_7		TRDIOD1				
21		P2_6		TRDIOC1				
22		P2_5		TRDIOB1				
23		P2_4		TRDIOA1				
24		P2_3		TRDIOD0				
25		P2_2		TRDIOC0				
26		P2_1		TRDIOB0				
27		P2_0		TRDIOA0/ TRDCLK				
28		P3_6	($\overline{\text{INT1}}$)(1)					
29		P3_1		(TRBO)(1)				
30		P8_6						
31		P8_5		TRFO12				
32		P8_4		TRFO11				
33		P8_3		TRFO10/TRFI				
34		P8_2		TRFO02				
35		P8_1		TRFO01				
36		P8_0		TRFO00				
37		P6_7	($\overline{\text{INT3}}$)(1)		(RXD2)/(SCL2)(1)			
38		P6_6	$\overline{\text{INT2}}$		(TXD2)/(SDA2)(1)			
39		P6_5	$\overline{\text{INT4}}$		(CLK2)(1)/(CLK1)(1)			
40		P4_5	$\overline{\text{INT0}}$					$\overline{\text{ADTRG}}$
41		P1_7	$\overline{\text{INT1}}$	TRAIO0(1)				ANEX3
42		P1_6			CLK0			ANEX2
43		P1_5	($\overline{\text{INT1}}$)(1)	(TRAIO0)(1)	RXD0			ANEX1
44		P1_4			TXD0			ANEX0
45		P1_3	$\overline{\text{KI3}}$	TRBO				AN11

Note:
1. This can be assigned to the pin in parentheses by a program.
2. Only for R8C/36E group and R8C/36F group.

Table 1.14 Pin Name Information by Pin Number (2)

Pin Number	Control Pin	Port	I/O Pin Functions for of Peripheral Modules					
			Interrupt	Timer	Serial Interface	Clock Synchronous Serial I/O with Chip Select	CAN Module(2)	A/D Converter Voltage Detection Circuit
46		P1_2	$\overline{KI2}$					AN10
47		P1_1	$\overline{KI1}$					AN9/LVCMP2
48		P1_0	$\overline{KI0}$					AN8
49		P0_7						AN0
50		P0_6						AN1
51		P0_5						AN2
52		P0_4		TREO				AN3
53		P0_3			(CLK1)(1)			AN4
54		P0_2			(RXD1)(1)			AN5
55		P0_1			(TXD1)(1)			AN6
56		P0_0						AN7
57		P6_4	($\overline{INT2}$)(1)	TRAIO1	(RXD1)(1)			
58		P6_3		(TRAO1)(1)	(TXD1)(1)			
59		P6_2					CRX0(2)	
60		P6_1					CTX0(2)	
61		P6_0		(TREO)(1)				
62		P5_7		TRGIOB				
63		P5_6		TRGIOA				
64		P3_2	($\overline{INT1}$)/ ($\overline{INT2}$)(1)	TRGCLKB				

Note:
1. This can be assigned to the pin in parentheses by a program.
2. Only for R8C/36E group and R8C/36F group.

1.5 Pin Functions

Tables 1.15 and 1.16 list Pin Functions.

Table 1.15 Pin Functions (1)

Item	Pin Name	I/O Type	Description
Power supply input	VCC, VSS	–	Apply 2.7 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	–	Power supply for the A/D converter. Connect a capacitor between AVCC and AVSS.
Reset input	$\overline{\text{RESET}}$	I	Input “L” on this pin resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
XIN clock input	XIN	I	These pins are provided for XIN clock generation circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins (1). To use an external clock, input it to the XIN pin and leave the XOUT pin open.
XIN clock output	XOUT	O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT4}}$	I	$\overline{\text{INT}}$ interrupt input pins.
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Key input interrupt input pins
Timer RA0	TRAIO0, TRAIO1	I/O	Timer RA I/O pin
Timer RA1	TRAO0, TRAO1	O	Timer RA output pin
Timer RB	TRBO	O	Timer RB output pin
Timer RC	TRCCLK	I	External clock input pin
	TRCTRG	I	External trigger input pin
	TRCIOA, TRCIOB, TRCIOC, TRCIOD	I/O	Timer RC I/O pins
Timer RD	TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1	I/O	Timer RD I/O pins
	TRDCLK	I	External clock input pin
Timer RE	TREO	O	Divided clock output pin
Timer RF	TRFO00, TRFO10, TRFO01,TRFO11, TRFO02,TRFO12	O	Timer RF output pins.
	TRFI	I	Timer RF input pin.
Timer RG	TRGIOA, TRGIOB	I/O	Timer RG I/O ports.
	TRGCLKA, TRGCLKB	I	External clock input pints.
Serial interface	CLK0, CLK1, CLK2	I/O	Transfer clock I/O pins
	RXD0, RXD1, RXD2	I	Serial data input pins
	TXD0, TXD1, TXD2	O	Serial data output pins
	$\overline{\text{CTS2}}$	I	Transmission control input pin
	$\overline{\text{RTS2}}$	O	Reception control output pin
	SCL2	I/O	I^2C mode clock I/O pin
	SDA2	I/O	I^2C mode data I/O pin
SSU	SSI	I/O	Data I/O pin
	$\overline{\text{SCS}}$	I/O	Chip-select signal I/O pin
	SSCK	I/O	Clock I/O pin
	SSO	I/O	Data I/O pin

I: Input O: Output I/O: Input and output

Note:

1. Refer to the oscillator manufacturer for oscillation characteristics.

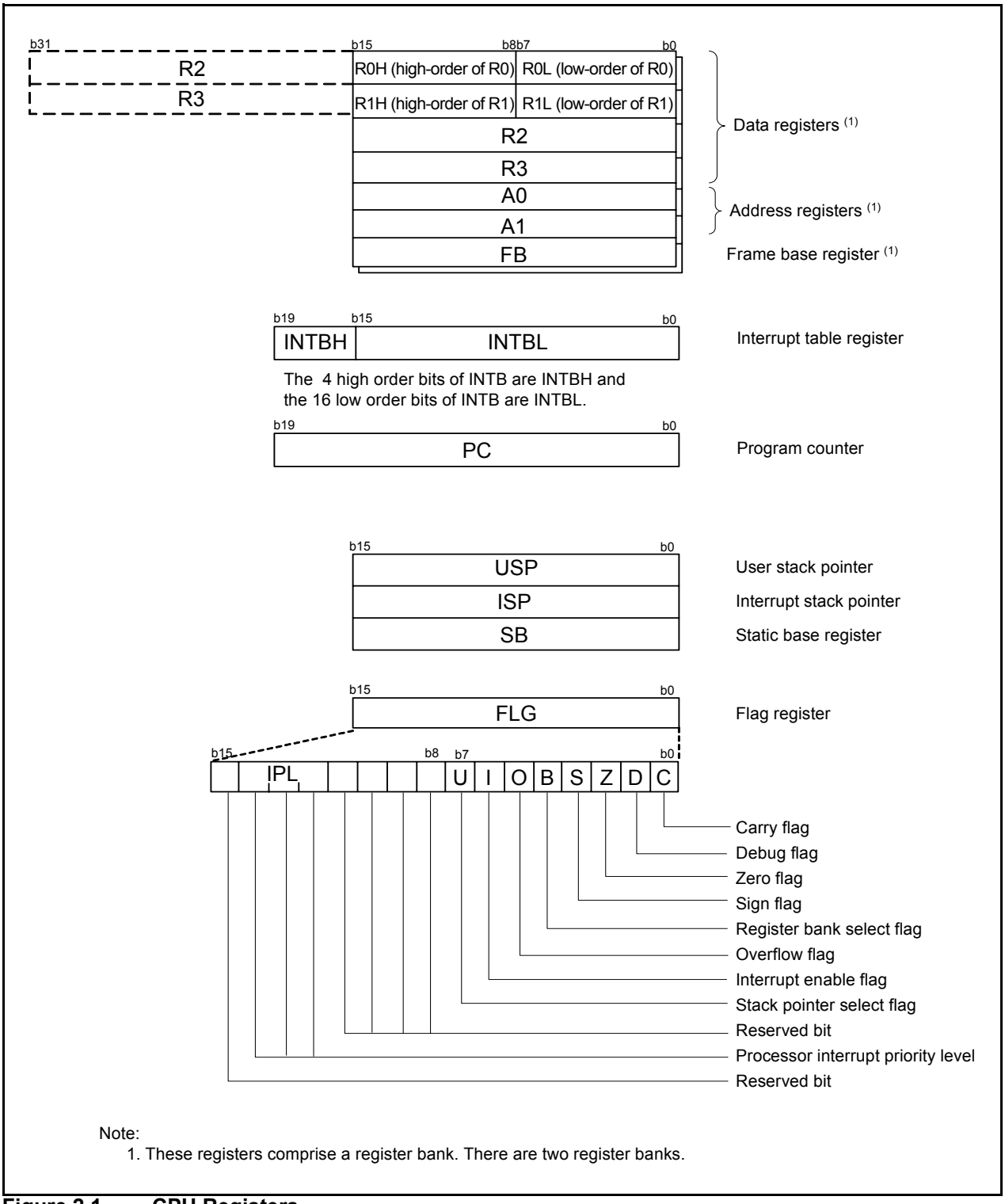
Table 1.16 Pin Functions (2)

Item	Pin Name	I/O Type	Description
CAN module	CRX0(2)	I	CAN data input pin
	CTX0(2)	O	CAN data output pin
Reference voltage input	VREF	I	Reference voltage input pin to A/D converter
A/D converter	AN0 to AN11 ANEX0 to ANEX3	I	Analog input pins to A/D converter
	$\overline{\text{ADTRG}}$	I	AD external trigger input pin
Voltage Detection Circuit	LVCMP2	I	Detection target voltage pin for voltage detection 2
I/O port	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_3 to P4_7, P5_0 to P5_4, P5_6, P5_7, P6_0 to P6_7, P8_0 to P8_6	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program.
Input port	P4_2	I	Input-only ports

I: Input O: Output I/O: Input and output
Note:
2. Only in the R8C/36E Group and the R8C/36F Group.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.



Note:
1. These registers comprise a register bank. There are two register banks.

Figure 2.1 CPU Registers

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP, and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.
Interrupt are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.
The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has higher priority than IPL, the interrupt is enabled.

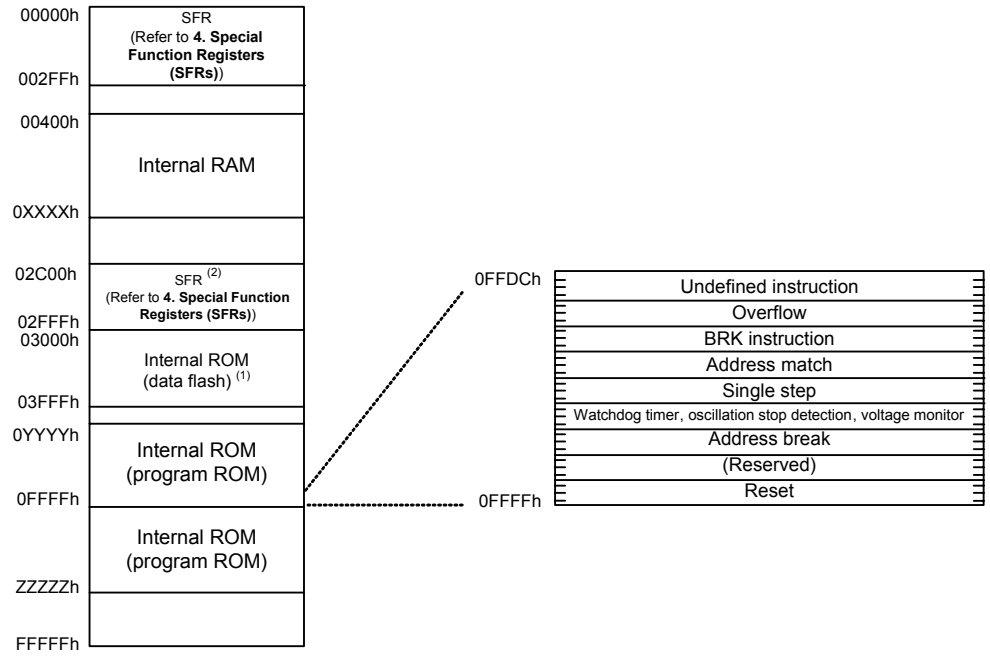
2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

3. Memory

3.1 R8C/36E Group

Figure 3.1 is a Memory Map of R8C/36E Group. The R8C/36E Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 64-Kbyte internal ROM area is allocated addresses 04000h to 13FFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.
The internal ROM (data flash) is allocated addresses 03000h to 03FFFh.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 6-Kbyte internal RAM area is allocated addresses 00400h to 01BFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh (the SFR areas for the CAN, DTC, and other modules). Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.



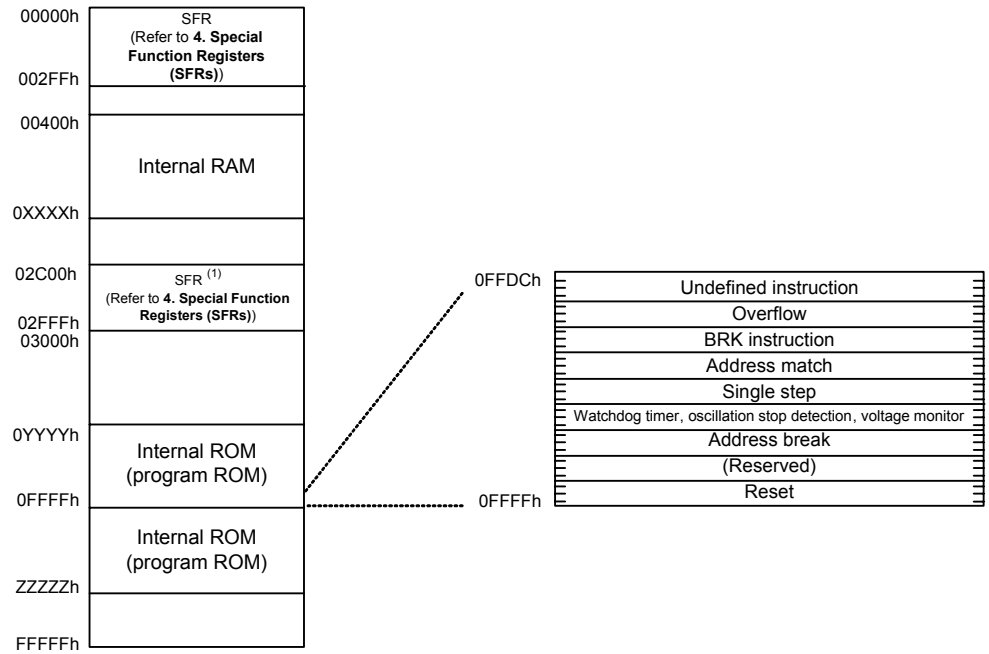
Notes:
1. The DataFlash memory indicates blocks A (1 Kbyte), B (1 Kbyte), C (1 Kbyte), and D (1 Kbyte).
2. The SFR areas for the CAN, DTC and other modules are allocated to addresses 02C00h to 02FFFh.
3. The blank areas are reserved and cannot be accessed by users.

Part Number	Internal ROM			Internal RAM	
	Size	Address 0YYYYh	Address ZZZZZh	Size	Address 0XXXXh
R5F21368EJFP, R5F21368EKFP	64 Kbytes	04000h	13FFFh	6 Kbytes	01BFFh
R5F2136AEJFP, R5F2136AEKFP	96 Kbytes	04000h	1BFFFh	8 Kbytes	023FFh
R5F2136CEJFP, R5F2136CEKFP	128 Kbytes	04000h	23FFFh	10 Kbytes	02BFFh

Figure 3.1 Memory Map of R8C/36E Group

3.2 R8C/36F Group

Figure 3.2 is a Memory Map of R8C/36F Group. The R8C/36F Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 64-Kbyte internal ROM area is allocated addresses 04000h to 13FFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 6-Kbyte internal RAM area is allocated addresses 00400h to 01BFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh (the SFR areas for the CAN, DTC, and other modules). Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.



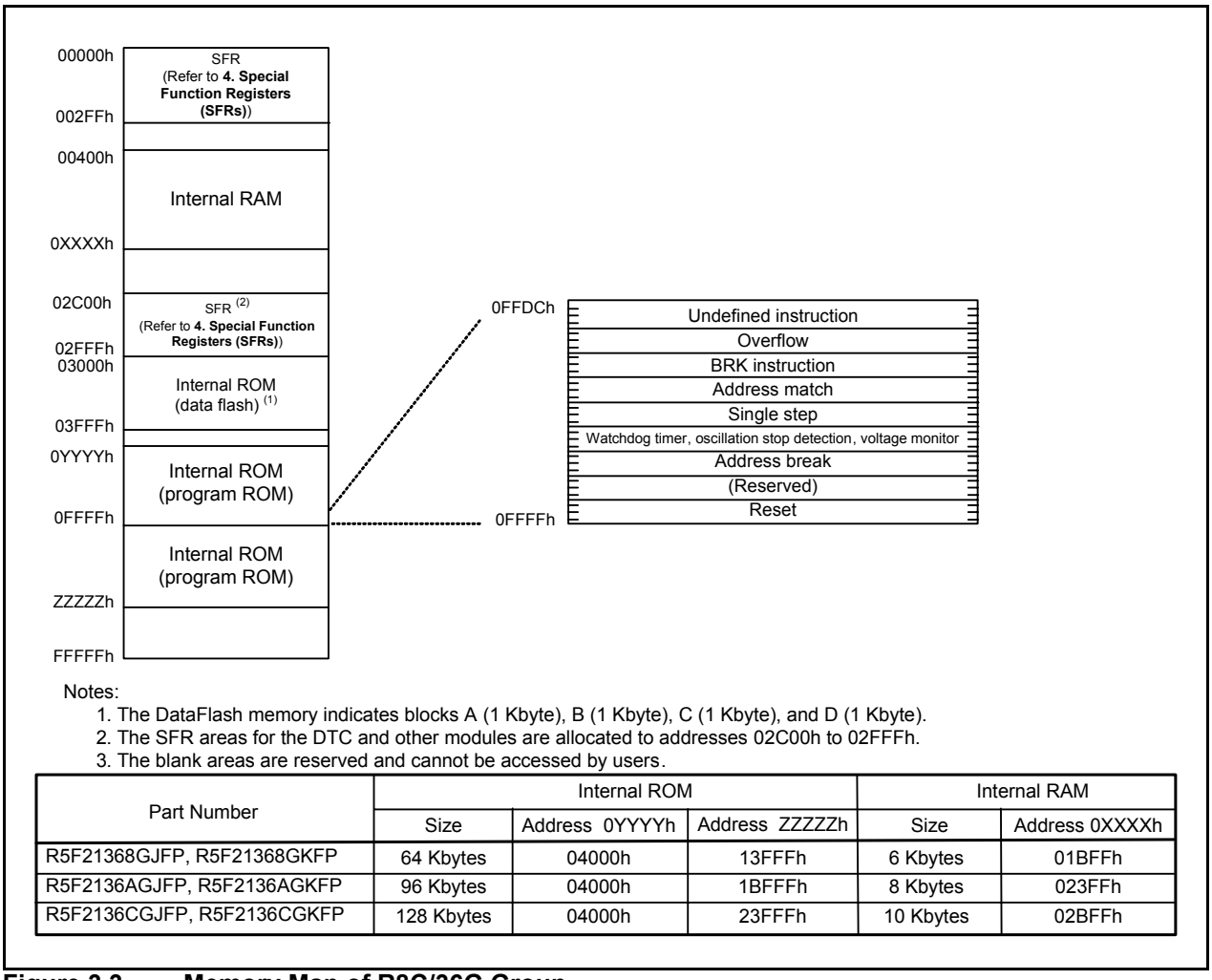
Notes:
1. The SFR areas for the CAN, DTC and other modules are allocated to addresses 02C00h to 02FFFh.
2. The blank areas are reserved and cannot be accessed by users.

Part Number	Internal ROM			Internal RAM	
	Size	Address 0YYYYh	Address ZZZZZh	Size	Address 0XXXXh
R5F21368FJFP, R5F21368FKFP	64 Kbytes	04000h	13FFFh	6 Kbytes	01BFFh
R5F2136AFJFP, R5F2136AFKFP	96 Kbytes	04000h	1BFFFh	8 Kbytes	023FFh
R5F2136CFJFP, R5F2136CFKFP	128 Kbytes	04000h	23FFFh	10 Kbytes	02BFFh

Figure 3.2 Memory Map of R8C/36F Group

3.3 R8C/36G Group

Figure 3.3 is a Memory Map of R8C/36G Group. The R8C/36G Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 64-Kbyte internal ROM area is allocated addresses 04000h to 13FFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.
The internal ROM (data flash) is allocated addresses 03000h to 03FFFh.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 6-Kbyte internal RAM area is allocated addresses 00400h to 01BFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh (the SFR areas for the DTC and other modules). Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.



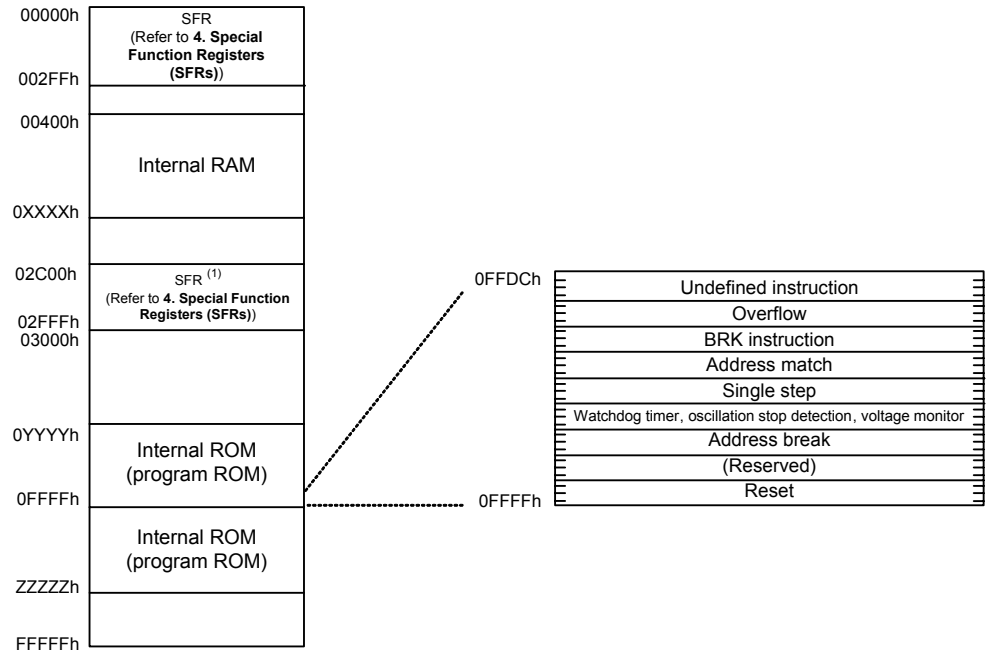
Notes:
1. The DataFlash memory indicates blocks A (1 Kbyte), B (1 Kbyte), C (1 Kbyte), and D (1 Kbyte).
2. The SFR areas for the DTC and other modules are allocated to addresses 02C00h to 02FFFh.
3. The blank areas are reserved and cannot be accessed by users.

Part Number	Internal ROM			Internal RAM	
	Size	Address 0YYYYh	Address ZZZZZh	Size	Address 0XXXXh
R5F21368GJFP, R5F21368GKFP	64 Kbytes	04000h	13FFFh	6 Kbytes	01BFFh
R5F2136AGJFP, R5F2136AGKFP	96 Kbytes	04000h	1BFFFh	8 Kbytes	023FFh
R5F2136CGJFP, R5F2136CGKFP	128 Kbytes	04000h	23FFFh	10 Kbytes	02BFFh

Figure 3.3 Memory Map of R8C/36G Group

3.4 R8C/36H Group

Figure 3.4 is a Memory Map of R8C/36H Group. The R8C/36H Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 64-Kbyte internal ROM area is allocated addresses 04000h to 13FFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 6-Kbyte internal RAM area is allocated addresses 00400h to 01BFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh (the SFR areas for the DTC and other modules). Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.



Notes:
1. The SFR areas for the DTC and other modules are allocated to addresses 02C00h to 02FFFh.
2. The blank areas are reserved and cannot be accessed by users.

Part Number	Internal ROM			Internal RAM	
	Size	Address 0YYYYh	Address ZZZZZh	Size	Address 0XXXXh
R5F21368HJFP, R5F21368HKFP	64 Kbytes	04000h	13FFFh	6 Kbytes	01BFFh
R5F2136AHJFP, R5F2136AHKFP	96 Kbytes	04000h	1BFFFh	8 Kbytes	023FFh
R5F2136CHJFP, R5F2136CHKFP	128 Kbytes	04000h	23FFFh	10 Kbytes	02BFFh

Figure 3.4 Memory Map of R8C/36H Group

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.17 list the special function registers.

Table 4.1 SFR Information (1) (1)

Address	Register	Symbol	After reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	00101000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h	Module Standby Control Register	MSTCR	00h
0009h	System Clock Control Register 3	CM3	00h
000Ah	Protect Register	PRCR	00h
000Bh	Reset Source Determination Register	RSTFR	0XXX00XXb (2)
000Ch	Oscillation Stop Detection Register	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDTC	00111111b
0010h			
0011h			
0012h			
0013h			
0014h			
0015h	High-Speed On-Chip Oscillator Control Register 7	FRA7	When shipping
0016h			
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h 10000000b (3)
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	00h
0024h	High-Speed On-Chip Oscillator Control Register 1	FRA1	When shipping
0025h	High-Speed On-Chip Oscillator Control Register 2	FRA2	00h
0026h	On-Chip Reference Voltage Control Register	OCVREFCR	00h
0027h			
0028h			
0029h	High-Speed On-Chip Oscillator Control Register 4	FRA4	When Shipping
002Ah	High-Speed On-Chip Oscillator Control Register 5	FRA5	When Shipping
002Bh	High-Speed On-Chip Oscillator Control Register 6	FRA6	When Shipping
002Ch			
002Dh			
002Eh			
002Fh	High-Speed On-Chip Oscillator Control Register 3	FRA3	When shipping
0030h	Voltage Monitor Circuit Control Register	CMPA	00h
0031h	Voltage Monitor Circuit Edge Select Register	VCAC	00h
0032h			
0033h	Voltage Detect Register 1	VCA1	00001000b
0034h	Voltage Detect Register 2	VCA2	00h (4) 00100000b (5)
0035h			
0036h	Voltage Detection 1 Level Select Register	VD1LS	00000111b
0037h			
0038h	Voltage Monitor 0 Circuit Control Register	VW0C	1100X010b (4) 1100X011b (5)
0039h	Voltage Monitor 1 Circuit Control Register	VW1C	10001010b

X : Undefined
NOTES:
1. The blank areas are reserved and cannot be accessed by users.
2. The CWR bit in the RSTFR register is set to 0 after power-on and voltage monitor 0 reset. Software reset, watchdog timer reset, or oscillation stop detection reset does not affect this bit.
3. The CSPROINI bit in the OFS register is set to 0.
4. The LVDAS bit in the OFS register is set to 1.
5. The LVDAS bit in the OFS register is set to 0.

Table 4.2 SFR Information (2) (1)

Address	Register	Symbol	After reset
003Ah	Voltage Monitor 2 Circuit Control Register	VW2C	10000010b
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			
0040h			
0041h	Flash Memory Ready Interrupt Control Register	FMRDYIC	XXXXX000b
0042h	Timer RA1 Interrupt Control Register	TRA1IC	XXXXX000b
0043h			
0044h			
0045h			
0046h	INT4 Interrupt Control Register	INT4IC	XX00X000b
0047h	Timer RC Interrupt Control Register	TRCIC	XXXXX000b
0048h	Timer RD0 Interrupt Control Register	TRD0IC	XXXXX000b
0049h	Timer RD1 Interrupt Control Register	TRD1IC	XXXXX000b
004Ah	Timer RE Interrupt Control Register	TREIC	XXXXX000b
004Bh	UART2 Transmit Interrupt Control Register	S2TIC	XXXXX000b
004Ch	UART2 Receive Interrupt Control Register	S2RIC	XXXXX000b
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh	SSU Interrupt Control Register	SSUIC	XXXXX000b
0050h	Timer RF Compare1 Interrupt Control Register	CMP1IC	XXXXX000b
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXXX000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXXX000b
0055h	INT2 Interrupt Control Register	INT2IC	XX00X000b
0056h	Timer RA0 Interrupt Control Register	TRA0IC	XXXXX000b
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh	Timer RF Interrupt Control Register	TRFIC	XXXXX000b
005Ch	Timer RF Compare0 Interrupt Control Register	CMP0IC	XXXXX000b
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh	UART2 Bus Collision Detection Interrupt Control Register	U2BCNIC	XXXXX000b
005Fh	Timer RF Capture Interrupt Control Register	CAPIC	XXXXX000b
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh	Timer RG Interrupt Control Register	TRGIC	XXXXX000b
006Ch	CAN0 Successful Reception Interrupt Control Register	C0RIC	XXXXX000b
006Dh	CAN0 Successful Transmission Interrupt Control Register	C0TIC	XXXXX000b
006Eh	CAN0 Receive FIFO Interrupt Control Register	C0FRIC	XXXXX000b
006Fh	CAN0 Transmit FIFO Interrupt Control Register	C0FTIC	XXXXX000b
0070h	CAN0 Error Interrupt Control Register	C0EIC	XXXXX000b
0071h	CAN0 Wake-up Interrupt Control Register	C0WIC	XXXXX000b
0072h	Voltage Monitor 1 Level Interrupt Control Register	VCMP1IC	XXXXX000b
0073h	Voltage Monitor 2 Level Interrupt Control Register	VCMP2IC	XXXXX000b
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

X : Undefined
NOTES:
1. The blank areas are reserved and cannot be accessed by users.

Table 4.3 SFR Information (3) (1)

Address	Register	Symbol	After reset
0080h	DTC Activation Control Register	DTCTL	00h
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h	DTC Activation Enable Register 0	DTCEN0	00h
0089h	DTC Activation Enable Register 1	DTCEN1	00h
008Ah	DTC Activation Enable Register 2	DTCEN2	00h
008Bh	DTC Activation Enable Register 3	DTCEN3	00h
008Ch	DTC Activation Enable Register 4	DTCEN4	00h
008Dh	DTC Activation Enable Register 5	DTCEN5	00h
008Eh	DTC Activation Enable Register 6	DTCEN6	00h
008Fh			
0090h	Timer RF Register	TRF	00h
0091h			00h
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah	Timer RF Control Register 0	TRFCR0	00h
009Bh	Timer RF Control Register 1	TRFCR1	00h
009Ch	Capture and Compare 0 Register	TRFM0	00h
009Dh			00h
009Eh	Compare 1 Register	TRFM1	FFh
009Fh			FFh
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h	UART2 Transmit/Receive Mode Register	U2MR	00h
00A9h	UART2 Bit Rate Register	U2BRG	XXh
00AAh	UART2 Transmit Buffer Register	U2TB	XXh
00ABh			XXh
00ACh	UART2 Transmit/Receive Control Register 0	U2C0	00001000b
00ADh	UART2 Transmit/Receive Control Register 1	U2C1	00000010b
00AEh	UART2 Receive Buffer Register	U2RB	XXh
00AFh			XXh
00B0h	UART2 Digital Filter Function Select Register	URXDF	00h
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h			
00B9h			
00BAh			
00BBh	UART2 Special Mode Register 5	U2SMR5	00h
00BCh	UART2 Special Mode Register 4	U2SMR4	00h
00BDh	UART2 Special Mode Register 3	U2SMR3	000X0X0Xb
00BEh	UART2 Special Mode Register 2	U2SMR2	X0000000b
00BFh	UART2 Special Mode Register	U2SMR	X0000000b

X : Undefined
Note:
1. The blank areas are reserved and cannot be accessed by users.

Table 4.4 SFR Information (4) (1)

Address	Register	Symbol	After reset
00C0h	A/D Register 0	AD0	XXh
00C1h			000000XXb
00C2h	A/D Register 1	AD1	XXh
00C3h			000000XXb
00C4h	A/D Register 2	AD2	XXh
00C5h			000000XXb
00C6h	A/D Register 3	AD3	XXh
00C7h			000000XXb
00C8h	A/D Register 4	AD4	XXh
00C9h			000000XXb
00CAh	A/D Register 5	AD5	XXh
00CBh			000000XXb
00CCh	A/D Register 6	AD6	XXh
00CDh			000000XXb
00CEh	A/D Register 7	AD7	XXh
00CFh			000000XXb
00D0h			
00D1h			
00D2h			
00D3h			
00D4h	A/D Mode Register	ADMOD	00h
00D5h	A/D Input Select Register	ADINSEL	11000000b
00D6h	A/D Control Register 0	ADCON0	00h
00D7h	A/D Control Register 1	ADCON1	00h
00D8h			
00D9h			
00DAh			
00DBh			
00DCh			
00DDh			
00DEh			
00DFh			
00E0h	Port P0 Register	P0	XXh
00E1h	Port P1 Register	P1	XXh
00E2h	Port P0 Direction Register	PD0	00h
00E3h	Port P1 Direction Register	PD1	00h
00E4h	Port P2 Register	P2	XXh
00E5h	Port P3 Register	P3	XXh
00E6h	Port P2 Direction Register	PD2	00h
00E7h	Port P3 Direction Register	PD3	00h
00E8h	Port P4 Register	P4	XXh
00E9h	Port P5 Register	P5	XXh
00EAh	Port P4 Direction Register	PD4	00h
00EBh	Port P5 Direction Register	PD5	00h
00ECh	Port P6 Register	P6	XXh
00EDh			
00EEh	Port P6 Direction Register	PD6	00h
00EFh			
00F0h	Port P8 Register	P8	XXh
00F1h			
00F2h	Port P8 Direction Register	PD8	00h
00F3h			
00F4h			
00F5h			
00F6h			
00F7h			
00F8h			
00F9h			
00FAh			
00FBh			
00FCh			
00FDh			
00FEh			
00FFh			

X : Undefined
Note:
1. The blank areas are reserved and cannot be accessed by users.

Table 4.5 SFR Information (5) (1)

Address	Register	Symbol	After reset
0100h	Timer RA0 Control Register	TRA0CR	00h
0101h	Timer RA0 I/O Control Register	TRA0IOC	00h
0102h	Timer RA0 Mode Register	TRA0MR	00h
0103h	Timer RA0 Prescaler Register	TRA0PRE	FFh
0104h	Timer RA0 Register	TRA0	FFh
0105h	LIN0 Control Register 2	LIN0CR2	00h
0106h	LIN0 Control Register	LIN0CR	00h
0107h	LIN0 Status Register	LIN0ST	00h
0108h	Timer RB Control Register	TRBCR	00h
0109h	Timer RB One-Shot Control Register	TRBOCR	00h
010Ah	Timer RB I/O Control Register	TRBIOC	00h
010Bh	Timer RB Mode Register	TRBMR	00h
010Ch	Timer RB Prescaler Register	TRBPRE	FFh
010Dh	Timer RB Secondary Register	TRBSC	FFh
010Eh	Timer RB Primary Register	TRBPR	FFh
010Fh			
0110h	Timer RA1 Control Register	TRA1CR	00h
0111h	Timer RA1 I/O Control Register	TRA1IOC	00h
0112h	Timer RA1 Mode Register	TRA1MR	00h
0113h	Timer RA1 Prescaler Register	TRA1PRE	FFh
0114h	Timer RA1 Register	TRA1	FFh
0115h	LIN1 Control Register 2	LIN1CR2	00h
0116h	LIN1 Control Register	LIN1CR	00h
0117h	LIN1 Status Register	LIN1ST	00h
0118h	Timer RE Counter Data Register	TRESEC	00h
0119h	Timer RE Compare Data Register	TREMIN	00h
011Ah			
011Bh			
011Ch	Timer RE Control Register 1	TRECR1	00h
011Dh	Timer RE Control Register 2	TRECR2	00h
011Eh	Timer RE Count Source Select Register	TRECSR	00001000b
011Fh			
0120h	Timer RC Mode Register	TRCMR	01001000b
0121h	Timer RC Control Register 1	TRCCR1	00h
0122h	Timer RC Interrupt Enable Register	TRCIER	01110000b
0123h	Timer RC Status Register	TRCSR	01110000b
0124h	Timer RC I/O Control Register 0	TRCIOR0	10001000b
0125h	Timer RC I/O Control Register 1	TRCIOR1	10001000b
0126h	Timer RC Counter	TRC	00h
0127h			00h
0128h	Timer RC General Register A	TRCGRA	FFh
0129h			FFh
012Ah	Timer RC General Register B	TRCGRB	FFh
012Bh			FFh
012Ch	Timer RC General Register C	TRCGRC	FFh
012Dh			FFh
012Eh	Timer RC General Register D	TRCGRD	FFh
012Fh			FFh
0130h	Timer RC Control Register 2	TRCCR2	00011000b
0131h	Timer RC Digital Filter Function Select Register	TRCDF	00h
0132h	Timer RC Output Master Enable Register	TRCOER	01111111b
0133h	Timer RC Trigger Control Register	TRCADCR	00h
0134h			
0135h			
0136h	Timer RD Trigger Control Register	TRDADCR	00h
0137h	Timer RD Start Register	TRDSTR	11111100b
0138h	Timer RD Mode Register	TRDMR	00001110b
0139h	Timer RD PWM Mode Register	TRDPMR	10001000b
013Ah	Timer RD Function Control Register	TRDFCR	10000000b
013Bh	Timer RD Output Master Enable Register 1	TRDOER1	FFh
013Ch	Timer RD Output Master Enable Register 2	TRDOER2	01111111b
013Dh	Timer RD Output Control Register	TRDOCR	00h
013Eh	Timer RD Digital Filter Function Select Register 0	TRDDF0	00h
013Fh	Timer RD Digital Filter Function Select Register 1	TRDDF1	00h

Note:
1. The blank areas are reserved and cannot be accessed by users.

Table 4.6 SFR Information (6) (1)

Address	Register	Symbol	After reset
0140h	Timer RD Control Register 0	TRDCR0	00h
0141h	Timer RD I/O Control Register A0	TRDIORA0	10001000b
0142h	Timer RD I/O Control Register C0	TRDIORC0	10001000b
0143h	Timer RD Status Register 0	TRDSR0	11100000b
0144h	Timer RD Interrupt Enable Register 0	TRDIER0	11100000b
0145h	Timer RD PWM Mode Output Level Control Register 0	TRDPOCR0	11111000b
0146h	Timer RD Counter 0	TRD0	00h
0147h			00h
0148h	Timer RD General Register A0	TRDGRA0	FFh
0149h			FFh
014Ah	Timer RD General Register B0	TRDGRB0	FFh
014Bh			FFh
014Ch	Timer RD General Register C0	TRDGRC0	FFh
014Dh			FFh
014Eh	Timer RD General Register D0	TRDGRD0	FFh
014Fh			FFh
0150h	Timer RD Control Register 1	TRDCR1	00h
0151h	Timer RD I/O Control Register A1	TRDIORA1	10001000b
0152h	Timer RD I/O Control Register C1	TRDIORC1	10001000b
0153h	Timer RD Status Register 1	TRDSR1	11000000b
0154h	Timer RD Interrupt Enable Register 1	TRDIER1	11100000b
0155h	Timer RD PWM Mode Output Level Control Register 1	TRDPOCR1	11111000b
0156h	Timer RD Counter 1	TRD1	00h
0157h			00h
0158h	Timer RD General Register A1	TRDGRA1	FFh
0159h			FFh
015Ah	Timer RD General Register B1	TRDGRB1	FFh
015Bh			FFh
015Ch	Timer RD General Register C1	TRDGRC1	FFh
015Dh			FFh
015Eh	Timer RD General Register D1	TRDGRD1	FFh
015Fh			FFh
0160h	UART1 Transmit/Receive Mode Register	U1MR	00h
0161h	UART1 Bit Rate Register	U1BRG	XXh
0162h	UART1 Transmit Buffer Register	U1TB	XXh
0163h			XXh
0164h	UART1 Transmit/Receive Control Register 0	U1C0	00001000b
0165h	UART1 Transmit/Receive Control Register 1	U1C1	00000010b
0166h	UART1 Receive Buffer Register	U1RB	XXh
0167h			XXh
0168h			
0169h			
016Ah			
016Bh			
016Ch			
016Dh			
016Eh			
016Fh			
0170h	Timer RG Mode Register	TRGMR	01000000b
0171h	Timer RG Count Control Register	TRGCNTC	00000000b
0172h	Timer RG Control Register	TRGCR	10000000b
0173h	Timer RG Interrupt Enable Register	TRGIER	11110000b
0174h	Timer RG Status Register	TRGSR	11100000b
0175h	Timer RG I/O Control Register	TRGIO	00000000b
0176h	Timer RG Counter	TRGC	00h
0177h			00h
0178h	Timer RG General Register A	TRGGRA	FFh
0179h			FFh
017Ah	Timer RG General Register B	TRGGRB	FFh
017Bh			FFh
017Ch	Timer RG General Register C	TRGGRC	FFh
017Dh			FFh
017Eh	Timer RG General Register D	TRGGRD	FFh
017Fh			FFh

X : Undefined
Note:
1. The blank areas are reserved and cannot be accessed by users.

Table 4.7 SFR Information (7) (1)

Address	Register	Symbol	After reset
0180h	Timer RA Pin Select Register	TRASR	00h
0181h	Timer RB/RC Pin Select Register	TRBRCSR	00h
0182h	Timer RC Pin Select Register 0	TRCPSR0	00h
0183h	Timer RC Pin Select Register 1	TRCPSR1	00h
0184h	Timer RD Pin Select Register 0	TRDPSR0	00h
0185h	Timer RD Pin Select Register 1	TRDPSR1	00h
0186h	Timer Pin Select Register	TIMSR	00h
0187h	Timer RF Output Control Register	TRFOUT	00h
0188h	UART0 Pin Select Register	U0SR	00h
0189h	UART1 Pin Select Register	U1SR	00h
018Ah	UART2 Pin Select Register 0	U2SR0	00h
018Bh	UART2 Pin Select Register 1	U2SR1	00h
018Ch	SSU Pin Select Register	SSUIICSR	00h
018Dh			
018Eh	INT Interrupt Input Pin Select Register	INTSR	00h
018Fh			
0190h			
0191h			
0192h			
0193h	SS Bit Counter Register	SSBR	11111000b
0194h	SS Transmit Data Register	SSTDR	FFh
0195h			FFh
0196h	SS Receive Data Register	SSRDR	FFh
0197h			FFh
0198h	SS Control Register H	SSCRH	00h
0199h	SS Control Register L	SSCRL	01111101b
019Ah	SS Mode Register	SSMR	00011000b
019Bh	SS Enable Register	SSER	00h
019Ch	SS Status Register	SSSR	00h
019Dh	SS Mode Register 2	SSMR2	00h
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01B0h			
01B1h			
01B2h	Flash Memory Status Register	FST	10000X00b
01B3h			
01B4h	Flash Memory Control Register 0	FMR0	00h
01B5h	Flash Memory Control Register 1	FMR1	00h
01B6h	Flash Memory Control Register 2	FMR2	00h
01B7h			
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			

X : Undefined
NOTES:
1. The blank areas are reserved and cannot be accessed by users.

Table 4.8 SFR Information (8) (1)

Address	Register	Symbol	After reset
01C0h	Address Match Interrupt Register 0	RMAD0	XXh
01C1h			XXh
01C2h			0000XXXXb
01C3h	Address Match Interrupt Enable Register 0	AIER0	00h
01C4h	Address Match Interrupt Register 1	RMAD1	XXh
01C5h			XXh
01C6h			0000XXXXb
01C7h	Address Match Interrupt Enable Register 1	AIER1	00h
01C8h			
01C9h			
01CAh			
01CBh			
01CCh			
01CDh			
01CEh			
01CFh			
01D0h			
01D1h			
01D2h			
01D3h			
01D4h			
01D5h			
01D6h			
01D7h			
01D8h			
01D9h			
01DAh			
01DBh			
01DCh			
01DDh			
01DEh			
01DFh			
01E0h	Pull-Up Control Register 0	PUR0	00h
01E1h	Pull-Up Control Register 1	PUR1	00h
01E2h	Pull-Up Control Register 2	PUR2	00h
01E3h			
01E4h			
01E5h			
01E6h			
01E7h			
01E8h			
01E9h			
01EAh			
01EBh			
01ECh			
01EDh			
01EEh			
01EFh			
01F0h			
01F1h			
01F2h			
01F3h			
01F4h			
01F5h	Input Threshold Control Register 0	VLT0	00h
01F6h	Input Threshold Control Register 1	VLT1	00h
01F7h	Input Threshold Control Register 2	VLT2	00h
01F8h			
01F9h			
01FAh	External Input Enable Register 0	INTEN	00h
01FBh	External Input Enable Register 1	INTEN1	00h
01FCh	INT Input Filter Select Register 0	INTF	00h
01FDh	INT Input Filter Select Register 1	INTF1	00h
01FEh	Key Input Enable Register 0	KIEN	00h
01FFh			

X : Undefined
Note:
1. The blank areas are reserved and cannot be accessed by users.

Table 4.9 SFR Information (9) (1)

Address	Register	Symbol	After reset
2C00h	DTC Transfer Vector Area		XXh
2C01h	DTC Transfer Vector Area		XXh
2C02h	DTC Transfer Vector Area		XXh
2C03h	DTC Transfer Vector Area		XXh
2C04h	DTC Transfer Vector Area		XXh
2C05h	DTC Transfer Vector Area		XXh
2C06h	DTC Transfer Vector Area		XXh
2C07h	DTC Transfer Vector Area		XXh
2C08h	DTC Transfer Vector Area		XXh
2C09h	DTC Transfer Vector Area		XXh
2C0Ah	DTC Transfer Vector Area		XXh
:	DTC Transfer Vector Area		XXh
:	DTC Transfer Vector Area		XXh
2C3Ah	DTC Transfer Vector Area		XXh
2C3Bh	DTC Transfer Vector Area		XXh
2C3Ch	DTC Transfer Vector Area		XXh
2C3Dh	DTC Transfer Vector Area		XXh
2C3Eh	DTC Transfer Vector Area		XXh
2C3Fh	DTC Transfer Vector Area		XXh
2C40h	DTC Control Data 0	DTCD0	XXh
2C41h			XXh
2C42h			XXh
2C43h			XXh
2C44h			XXh
2C45h			XXh
2C46h			XXh
2C47h			XXh
2C48h	DTC Control Data 1	DTCD1	XXh
2C49h			XXh
2C4Ah			XXh
2C4Bh			XXh
2C4Ch			XXh
2C4Dh			XXh
2C4Eh			XXh
2C4Fh			XXh
2C50h	DTC Control Data 2	DTCD2	XXh
2C51h			XXh
2C52h			XXh
2C53h			XXh
2C54h			XXh
2C55h			XXh
2C56h			XXh
2C57h			XXh
2C58h	DTC Control Data 3	DTCD3	XXh
2C59h			XXh
2C5Ah			XXh
2C5Bh			XXh
2C5Ch			XXh
2C5Dh			XXh
2C5Eh			XXh
2C5Fh			XXh
2C60h	DTC Control Data 4	DTCD4	XXh
2C61h			XXh
2C62h			XXh
2C63h			XXh
2C64h			XXh
2C65h			XXh
2C66h			XXh
2C67h			XXh
2C68h	DTC Control Data 5	DTCD5	XXh
2C69h			XXh
2C6Ah			XXh
2C6Bh			XXh
2C6Ch			XXh
2C6Dh			XXh
2C6Eh			XXh
2C6Fh			XXh

X : Undefined
Note:
1. The blank areas are reserved and cannot be accessed by users.

Table 4.10 SFR Information (10) (1)

Address	Register	Symbol	After reset
2C70h	DTC Control Data 6	DTCD6	XXh
2C71h			XXh
2C72h			XXh
2C73h			XXh
2C74h			XXh
2C75h			XXh
2C76h			XXh
2C77h			XXh
2C78h	DTC Control Data 7	DTCD7	XXh
2C79h			XXh
2C7Ah			XXh
2C7Bh			XXh
2C7Ch			XXh
2C7Dh			XXh
2C7Eh			XXh
2C7Fh			XXh
2C80h	DTC Control Data 8	DTCD8	XXh
2C81h			XXh
2C82h			XXh
2C83h			XXh
2C84h			XXh
2C85h			XXh
2C86h			XXh
2C87h			XXh
2C88h	DTC Control Data 9	DTCD9	XXh
2C89h			XXh
2C8Ah			XXh
2C8Bh			XXh
2C8Ch			XXh
2C8Dh			XXh
2C8Eh			XXh
2C8Fh			XXh
2C90h	DTC Control Data 10	DTCD10	XXh
2C91h			XXh
2C92h			XXh
2C93h			XXh
2C94h			XXh
2C95h			XXh
2C96h			XXh
2C97h			XXh
2C98h	DTC Control Data 11	DTCD11	XXh
2C99h			XXh
2C9Ah			XXh
2C9Bh			XXh
2C9Ch			XXh
2C9Dh			XXh
2C9Eh			XXh
2C9Fh			XXh
2CA0h	DTC Control Data 12	DTCD12	XXh
2CA1h			XXh
2CA2h			XXh
2CA3h			XXh
2CA4h			XXh
2CA5h			XXh
2CA6h			XXh
2CA7h			XXh
2CA8h	DTC Control Data 13	DTCD13	XXh
2CA9h			XXh
2CAAh			XXh
2CABh			XXh
2CACh			XXh
2CADh			XXh
2CAEh			XXh
2CAFh			XXh

X : Undefined
Note:
1. The blank areas are reserved and cannot be accessed by users.

Table 4.11 SFR Information (11) (1)

Address	Register	Symbol	After reset
2CB0h	DTC Control Data 14	DTCD14	XXh
2CB1h			XXh
2CB2h			XXh
2CB3h			XXh
2CB4h			XXh
2CB5h			XXh
2CB6h			XXh
2CB7h			XXh
2CB8h	DTC Control Data 15	DTCD15	XXh
2CB9h			XXh
2CBAh			XXh
2CBBh			XXh
2CBCh			XXh
2CBDh			XXh
2CBEh			XXh
2CBFh			XXh
2CC0h	DTC Control Data 16	DTCD16	XXh
2CC1h			XXh
2CC2h			XXh
2CC3h			XXh
2CC4h			XXh
2CC5h			XXh
2CC6h			XXh
2CC7h			XXh
2CC8h	DTC Control Data 17	DTCD17	XXh
2CC9h			XXh
2CCAh			XXh
2CCBh			XXh
2CCCh			XXh
2CCDh			XXh
2CCEh			XXh
2CCFh			XXh
2CD0h	DTC Control Data 18	DTCD18	XXh
2CD1h			XXh
2CD2h			XXh
2CD3h			XXh
2CD4h			XXh
2CD5h			XXh
2CD6h			XXh
2CD7h			XXh
2CD8h	DTC Control Data 19	DTCD19	XXh
2CD9h			XXh
2CDAh			XXh
2CDBh			XXh
2CDCh			XXh
2CDDh			XXh
2CDEh			XXh
2CDFh			XXh
2CE0h	DTC Control Data 20	DTCD20	XXh
2CE1h			XXh
2CE2h			XXh
2CE3h			XXh
2CE4h			XXh
2CE5h			XXh
2CE6h			XXh
2CE7h			XXh
2CE8h	DTC Control Data 21	DTCD21	XXh
2CE9h			XXh
2CEAh			XXh
2CEBh			XXh
2CECh			XXh
2CEDh			XXh
2CEEh			XXh
2CEFh			XXh

X : Undefined
Note:
1. The blank areas are reserved and cannot be accessed by users.

Table 4.12 SFR Information (12) (1)

Address	Register	Symbol	After reset
2CF0h	DTC Control Data 22	DTCD22	XXh
2CF1h			XXh
2CF2h			XXh
2CF3h			XXh
2CF4h			XXh
2CF5h			XXh
2CF6h			XXh
2CF7h			XXh
2CF8h	DTC Control Data 23	DTCD23	XXh
2CF9h			XXh
2CFAh			XXh
2CFBh			XXh
2CFCh			XXh
2CFDh			XXh
2CFEh			XXh
2CFFh			XXh
2D00h			
2D01h			
:			
2E00h	CAN0 Mailbox 0 : Message ID	C0MB0	XXXX XXXXh
2E01h			
2E02h			
2E03h			
2E04h			
2E05h	CAN0 Mailbox 0 : Data length		XXh
2E06h	CAN0 Mailbox 0 : Data field		XXXX XXXX
2E07h			XXXX XXXXh
2E08h			
2E09h			
2E0Ah			
2E0Bh			
2E0Ch			
2E0Dh			
2E0Eh	CAN0 Mailbox 0 : Time stamp		XXXXh
2E0Fh			
2E10h	CAN0 Mailbox 1 : Message ID	C0MB1	XXXX XXXXh
2E11h			
2E12h			
2E13h			
2E14h			
2E15h	CAN0 Mailbox 1 : Data length		XXh
2E16h	CAN0 Mailbox 1 : Data field		XXXX XXXX
2E17h			XXXX XXXXh
2E18h			
2E19h			
2E1Ah			
2E1Bh			
2E1Ch			
2E1Dh			
2E1Eh	CAN0 Mailbox 1 : Time stamp		XXXXh
2E1Fh			
2E20h	CAN0 Mailbox 2 : Message ID	C0MB2	XXXX XXXXh
2E21h			
2E22h			
2E23h			
2E24h			
2E25h	CAN0 Mailbox 2 : Data length		XXh
2E26h	CAN0 Mailbox 2 : Data field		XXXX XXXX
2E27h			XXXX XXXXh
2E28h			
2E29h			
2E2Ah			
2E2Bh			
2E2Ch			
2E2Dh			
2E2Eh	CAN0 Mailbox 2 : Time stamp		XXXXh
2E2Fh			

X : Undefined
NOTES:
1. The blank areas are reserved and cannot be accessed by users.

Table 4.13 SFR Information (13) (1)

Address	Register	Symbol	After reset
2E30h	CAN0 Mailbox 3 : Message ID	C0MB3	XXXX XXXXh
2E31h			
2E32h			
2E33h			
2E34h			
2E35h	CAN0 Mailbox 3 : Data length		XXh
2E36h	CAN0 Mailbox 3 : Data field		XXXX XXXX
2E37h			XXXX XXXXh
2E38h			
2E39h			
2E3Ah			
2E3Bh			
2E3Ch			
2E3Dh			
2E3Eh	CAN0 Mailbox3 : Time stamp		XXXXh
2E3Fh			
2E40h	CAN0 Mailbox4 : Message ID	C0MB4	XXXX XXXXh
2E41h			
2E42h			
2E43h			
2E44h			
2E45h	CAN0 Mailbox4 : Data length		XXh
2E46h	CAN0 Mailbox4 : Data field		XXXX XXXX
2E47h			XXXX XXXXh
2E48h			
2E49h			
2E4Ah			
2E4Bh			
2E4Ch			
2E4Dh			
2E4Eh	CAN0 Mailbox4 : Time stamp		XXXXh
2E4Fh			
2E50h	CAN0 Mailbox5 : Message ID	C0MB5	XXXX XXXXh
2E51h			
2E52h			
2E53h			
2E54h			
2E55h	CAN0 Mailbox5 : Data length		XXh
2E56h	CAN0 Mailbox5 : Data field		XXXX XXXX
2E57h			XXXX XXXXh
2E58h			
2E59h			
2E5Ah			
2E5Bh			
2E5Ch			
2E5Dh			
2E5Eh	CAN0 Mailbox5 : Time stamp		XXXXh
2E5Fh			
2E60h	CAN0 Mailbox6 : Message ID	C0MB6	XXXX XXXXh
2E61h			
2E62h			
2E63h			
2E64h			
2E65h	CAN0 Mailbox6 : Data length		XXh
2E66h	CAN0 Mailbox6 : Data field		XXXX XXXX
2E67h			XXXX XXXXh
2E68h			
2E69h			
2E6Ah			
2E6Bh			
2E6Ch			
2E6Dh			
2E6Eh	CAN0 Mailbox6 : Time stamp		XXXXh
2E6Fh			

X : Undefined
NOTES:
1. The blank areas are reserved and cannot be accessed by users.

Table 4.14 SFR Information (14) (1)

Address	Register	Symbol	After reset
2E70h	CAN0 Mailbox7 : Message ID	C0MB7	XXXX XXXXh
2E71h			
2E72h			
2E73h			
2E74h			
2E75h	CAN0 Mailbox7 : Data length		XXh
2E76h	CAN0 Mailbox7 : Data field		XXXX XXXX
2E77h			XXXX XXXXh
2E78h			
2E79h			
2E7Ah			
2E7Bh			
2E7Ch			
2E7Dh			
2E7Eh	CAN0 Mailbox7 : Time stamp		XXXXh
2E7Fh			
2E80h	CAN0 Mailbox8 : Message ID	C0MB8	XXXX XXXXh
2E81h			
2E82h			
2E83h			
2E84h			
2E85h	CAN0 Mailbox8 : Data length		XXh
2E86h	CAN0 Mailbox8 : Data field		XXXX XXXX
2E87h			XXXX XXXXh
2E88h			
2E89h			
2E8Ah			
2E8Bh			
2E8Ch			
2E8Dh			
2E8Eh	CAN0 Mailbox8 : Time stamp		XXXXh
2E8Fh			
2E90h	CAN0 Mailbox9 : Message ID	C0MB9	XXXX XXXXh
2E91h			
2E92h			
2E93h			
2E94h			
2E95h	CAN0 Mailbox9 : Data length		XXh
2E96h	CAN0 Mailbox9 : Data field		XXXX XXXX
2E97h			XXXX XXXXh
2E98h			
2E99h			
2E9Ah			
2E9Bh			
2E9Ch			
2E9Dh			
2E9Eh	CAN0 Mailbox9 : Time stamp		XXXXh
2E9Fh			
2EA0h	CAN0 Mailbox10 : Message ID	C0MB10	XXXX XXXXh
2EA1h			
2EA2h			
2EA3h			
2EA4h			
2EA5h	CAN0 Mailbox10 : Data length		XXh
2EA6h	CAN0 Mailbox10 : Data field		XXXX XXXX
2EA7h			XXXX XXXXh
2EA8h			
2EA9h			
2EAAh			
2EABh			
2EACh			
2EADh			
2EAEh	CAN0 Mailbox10 : Time stamp		XXXXh
2EAFh			

X : Undefined
NOTES:
1. The blank areas are reserved and cannot be accessed by users.

Table 4.15 SFR Information (15) (1)

Address	Register	Symbol	After reset
2EB0h	CAN0 Mailbox11 : Message ID	C0MB11	XXXX XXXXh
2EB1h			
2EB2h			
2EB3h			
2EB4h			
2EB5h	CAN0 Mailbox11 : Data length		XXh
2EB6h	CAN0 Mailbox11 : Data field		XXXX XXXX
2EB7h			XXXX XXXXh
2EB8h			
2EB9h			
2EBAh			
2EBBh			
2EBCh			
2EBDh			
2EBEh	CAN0 Mailbox11 : Time stamp		XXXXh
2EBFh			
2EC0h	CAN0 Mailbox12 : Message ID	C0MB12	XXXX XXXXh
2EC1h			
2EC2h			
2EC3h			
2EC4h			
2EC5h	CAN0 Mailbox12 : Data length		XXh
2EC6h	CAN0 Mailbox12 : Data field		XXXX XXXX
2EC7h			XXXX XXXXh
2EC8h			
2EC9h			
2ECAh			
2ECBh			
2ECCh			
2ECDh			
2ECEh	CAN0 Mailbox12 : Time stamp		XXXXh
2ECFh			
2ED0h	CAN0 Mailbox13 : Message ID	C0MB13	XXXX XXXXh
2ED1h			
2ED2h			
2ED3h			
2ED4h			
2ED5h	CAN0 Mailbox13 : Data length		XXh
2ED6h	CAN0 Mailbox13 : Data field		XXXX XXXX
2ED7h			XXXX XXXXh
2ED8h			
2ED9h			
2EDAh			
2EDBh			
2EDCh			
2EDDh			
2EDEh	CAN0 Mailbox13 : Time stamp		XXXXh
2EDFh			
2EE0h	CAN0 Mailbox14 : Message ID	C0MB14	XXXX XXXXh
2EE1h			
2EE2h			
2EE3h			
2EE4h			
2EE5h	CAN0 Mailbox14 : Data length		XXh
2EE6h	CAN0 Mailbox14 : Data field		XXXX XXXX
2EE7h			XXXX XXXXh
2EE8h			
2EE9h			
2EEAh			
2EEBh			
2EECh			
2EEDh			
2EEEh	CAN0 Mailbox14 : Time stamp		XXXXh
2EEFh			

X : Undefined
NOTES:
1. The blank areas are reserved and cannot be accessed by users.

Table 4.16 SFR Information (16) (1)

Address	Register	Symbol	After reset
2EF0h	CAN0 Mailbox15 : Message ID	C0MB15	XXXX XXXXh
2EF1h			
2EF2h			
2EF3h			
2EF4h			
2EF5h	CAN0 Mailbox15 : Data length		XXh
2EF6h	CAN0 Mailbox15 : Data field		XXXX XXXX
2EF7h			XXXX XXXXh
2EF8h			
2EF9h			
2EFAh			
2EFBh			
2EFCh			
2EFDh			
2EFEh	CAN0 Mailbox15 : Time stamp		XXXXh
2EFFh			
2F00h			
2F01h			
2F02h			
2F03h			
2F04h			
2F05h			
2F06h			
2F07h			
2F08h			
2F09h			
2F0Ah			
2F0Bh			
2F0Ch			
2F0Dh			
2F0Eh			
2F0Fh			
2F10h	CAN0 Mask Register 0	C0MKR0	XXXX XXXXh
2F11h			
2F12h			
2F13h			
2F14h	CAN0 Mask Register 1	C0MKR1	XXXX XXXXh
2F15h			
2F16h			
2F17h			
2F18h	CAN0 Mask Register 2	C0MKR2	XXXX XXXXh
2F19h			
2F1Ah			
2F1Bh			
2F1Ch	CAN0 Mask Register 3	C0MKR3	XXXX XXXXh
2F1Dh			
2F1Eh			
2F1Fh			
2F20h	CAN0 FIFO Received ID Compare Register 0	C0FIDCR0	XXXX XXXXh
2F21h			
2F22h			
2F23h			
2F24h	CAN0 FIFO Received ID Compare Register 1	C0FIDCR1	XXXX XXXXh
2F25h			
2F26h			
2F27h			
2F28h			
2F29h			
2F2Ah	CAN0 Mask Invalid Register	C0MKIVLR	XXXXh
2F2Bh			
2F2Ch			
2F2Dh			
2F2Eh	CAN0 Mailbox Interrupt Enable Register	C0MIER	XXXXh
2F2Fh			
2F30h	CAN0 Message Control Register 0	C0MCTL0	00h
2F31h	CAN0 Message Control Register 1	C0MCTL1	00h
2F32h	CAN0 Message Control Register 2	C0MCTL2	00h
2F33h	CAN0 Message Control Register 3	C0MCTL3	00h
2F34h	CAN0 Message Control Register 4	C0MCTL4	00h
2F35h	CAN0 Message Control Register 5	C0MCTL5	00h
2F36h	CAN0 Message Control Register 6	C0MCTL6	00h
2F37h	CAN0 Message Control Register 7	C0MCTL7	00h
2F38h	CAN0 Message Control Register 8	C0MCTL8	00h
2F39h	CAN0 Message Control Register 9	C0MCTL9	00h
2F3Ah	CAN0 Message Control Register 10	C0MCTL10	00h

X : Undefined
NOTES:
1. The blank areas are reserved and cannot be accessed by users.

Table 4.17 SFR Information (17) (1)

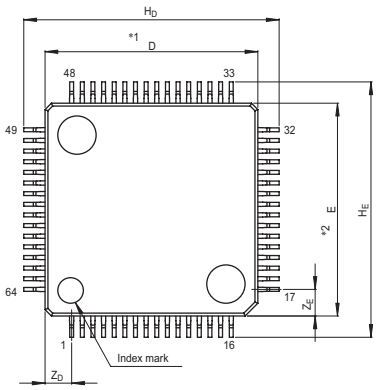
Address	Register	Symbol	After reset
2F3Bh	CAN0 Message Control Register 11	C0MCTL11	00h
2F3Ch	CAN0 Message Control Register 12	C0MCTL12	00h
2F3Dh	CAN0 Message Control Register 13	C0MCTL13	00h
2F3Eh	CAN0 Message Control Register 14	C0MCTL14	00h
2F3Fh	CAN0 Message Control Register 15	C0MCTL15	00h
2F40h	CAN0 Control Register	C0CTLR	0000 0101b
2F41h			0000 0000b
2F42h	CAN0 Status Register	C0STR	0000 0101b
2F43h			0000 0000b
2F44h	CAN0 Bit Configuration Register	C0BCR	00 0000h
2F45h			
2F46h			
2F47h			
2F48h	CAN0 Receive FIFO Control Register	C0RFCR	1000 0000b
2F49h	CAN0 Receive FIFO Pointer Control Register	C0RFPCR	XXh
2F4Ah	CAN0 Transmit FIFO Control Register	C0TFCR	1000 0000b
2F4Bh	CAN0 Transmit FIFO Pointer Control Register	C0TFPCR	XXh
2F4Ch	CAN0 Error Interrupt Enable Register	C0EIER	00h
2F4Dh	CAN0 Error Interrupt Factor Judge Register	C0EIFR	00h
2F4Eh	CAN0 Reception Error Count Register	C0RECR	00h
2F4Fh	CAN0 Transmission Error Count Register	C0TECR	00h
2F50h	CAN0 Error Code Store Register	C0ECSR	00h
2F51h	CAN0 Channel Search Support Register	C0CSSR	XXh
2F52h	CAN0 Mailbox Search Status Register	C0MSSR	1000 0000b
2F53h	CAN0 Mailbox Search Mode Register	C0MSMR	XXXX XX00b
2F54h	CAN0 Time Stamp Register	C0TSR	0000h
2F55h			
2F56h	CAN0 Acceptance Filter Support Register	C0AFSR	XXXXh
2F57h			
2F58h	CAN0 Test Control Register	C0TCR	00h
:			
FFDBh	Option Function Select Register2	OFS2	(Note 2)
:			
FFFFh	Option Function Select Register	OFS	(Note 2)

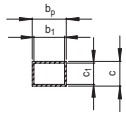
X : Undefined
NOTES:
1. The blank areas are reserved and cannot be accessed by users.
2. This register cannot be changed by a program. Use a flash programmer to write to it.

Package Dimensions

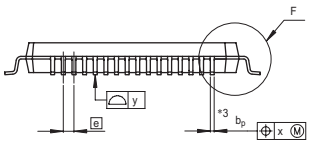
Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Technology website.

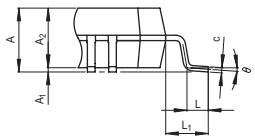
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP64-10x10-0.50	PLQP0064KB-A	64P6Q-A / FP-64K / FP-64KV	0.3g





Terminal cross section





Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

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RENESAS SALES OFFICES

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Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology (Shanghai) Co., Ltd.
Unit 204, 205, AZIACenter, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7858/7898

Renesas Technology Hong Kong Ltd.
7th Floor, North Tower, World Finance Centre, Harbour City, Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2377-3473

Renesas Technology Taiwan Co., Ltd.
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 3518-3399

Renesas Technology Singapore Pte. Ltd.
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.
Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510

Colophon .7.2