UG0557
User Guide
SmartFusion2 SoC FPGA Advanced Development Kit

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 3.0

PCIe edge card ribbon cable was removed from the kit contents. For more information, see Kit Contents, page 2.

1.2 Revision 2.0

The following is a summary of the changes in revision 2.0 of this document.

- Throughout the document, the part number was updated from M2S150-ADV-DEV-KIT-ES to M2S150-ADV-DEV-KIT (SAR 66855).
- Throughout the document, the device number was updated from M2S150T-1FCG1152ES to M2S150TS-1FCG1152 (SAR 66855).
- The MTD files link was updated. For more information, see Manufacturing Test, page 75 (SAR 60671 and 68260).
- Pin details were updated. For more information, see Validating Power Supply, page 75 (SAR 61171).
- Information about FMC connectors was updated. For more information, see FMC Connectors, page 25 (SAR 67950).

1.3 Revision 1.0

Revision 1.0 was the first publication of this document.

2 Introduction

The RoHS-compliant SmartFusion®2 SoC FPGA Advanced Development Kit (M2S150-ADV-DEV-KIT) enables you to develop the following.

- Microprocessor applications
- Embedded ARM® Cortex®-M3 processor-based systems
- Motor control applications
- Industrial automation applications
- High-speed serial I/O applications
- Universal serial bus (USB) applications (with OTG support)

2.1 Kit Contents

The following table lists the contents of the SmartFusion2 Advanced Development Kit.

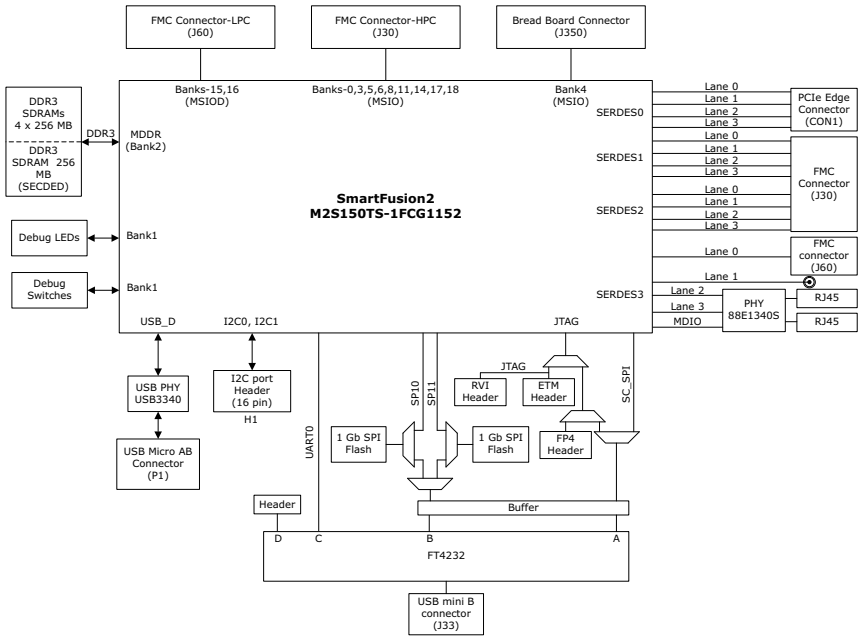
Table 1 • **Kit Contents**

Item	Quantity
SmartFusion2 Advanced Development Board with 150K LE M2S150TS-1FCG1152 device	1
USB A to Micro B cable	1
USB Micro A to A cable	1
USB A to Mini B cable	1
12 V/5 A power adapter	1

2.2 Block Diagram

The following figure is the block diagram of the SmartFusion2 Advanced Development Kit.

Figure 1 • **SmartFusion2 Advanced Development Kit Block Diagram**



2.3 Web Resources

More information about the SmartFusion2 Advanced Development Kit is available at *http://www.microsemi.com/products/fpga-soc/design-resources/dev-kits/smartfusion2/smartfusion2-advanced-development-kit#overview*.

2.4 Board Description

M2S150-ADV-DEV-KIT offers a full-featured development board for SmartFusion2 SoC FPGAs. The board integrates the following features on a single chip.

- Reliable flash-based FPGA fabric
- 166 MHz ARM Cortex-M3 processor
- Advanced security processing accelerators
- Digital signal processing (DSP) blocks
- Static random-access memory (SRAM)
- Embedded non-volatile memory (eNVM)
- High-performance communication interfaces

The SmartFusion2 Advanced Development Board has several standard interfaces including:

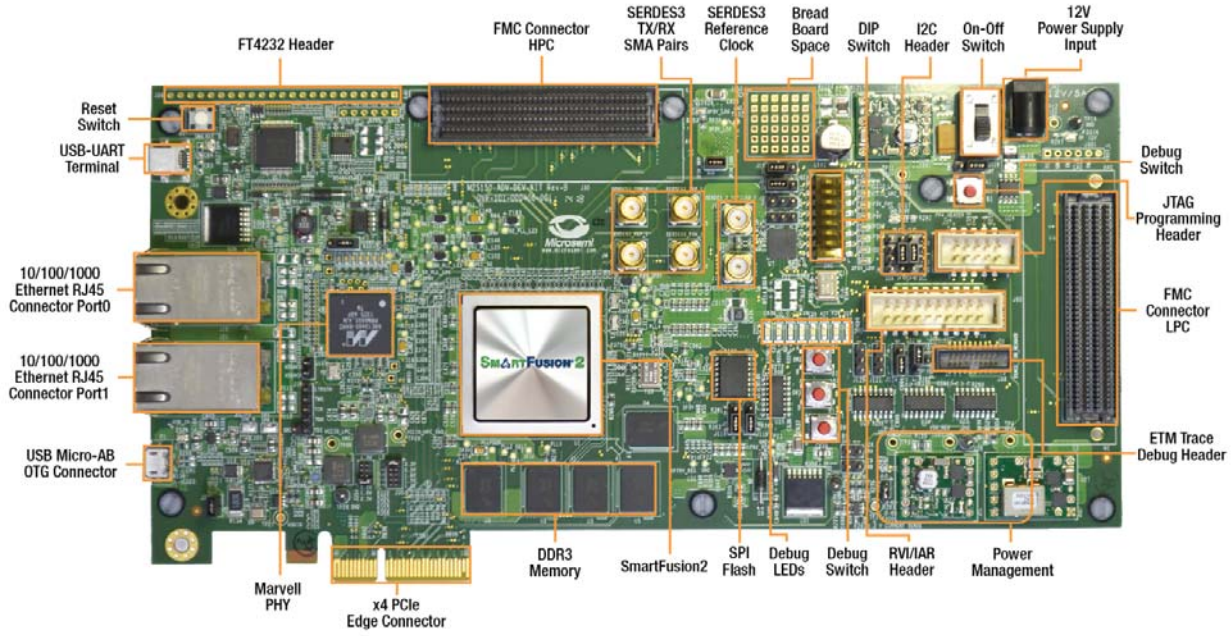
- USB
- x4 serializer and deserializer (SerDes)
- DDR3 memory
- JTAG
- Inter-integrated circuit (I2C)
- Serial peripheral interface (SPI)
- Universal asynchronous receiver/transmitter (UART)
- Dual gigabit Ethernet

The SmartFusion2 memory management system supports 1 GB (4 × 256 MB) on-board DDR3 memory for data storage, 256 MB DDR3 memory for error detection and correction (ECC-SECDED), and 2 GB (2 × 1 GB) memory for SPI flash devices. The SerDes block can be accessed using the PCIe edge connector, high-speed sub-miniature version-A (SMA) connectors, or an on-board FPGA mezzanine card (FMC) low pin count (LPC) connector (J60). Unused MSIOD signals are routed to the J60 connector from the SmartFusion2 device. Unused MSIO signals are routed to another on-board FMC connector—HPC (J30), and although the bread board connector (J350) space available for Bank 4 (MSIO) pins.

The SmartFusion2 device can be programmed through embedded FlashPro5. The Advanced Development Kit has the current measurement feature (see Current Measurement, page 11).

The following figure is a snapshot of the SmartFusion2 Advanced Development Board with its engineering silicon.

Figure 2 • **SmartFusion2 Advanced Development Board**



2.5 Board Key Components

The following table lists key components of the SmartFusion2 Advanced Development Board.

Table 2 • **SmartFusion2 Advanced Development Board Components**

Name	Description
SmartFusion2 FPGA	M2S150TS-1FCG1152 FPGA with a hard Cortex-M3 processor.
DDR3 synchronous dynamic random access memory (SDRAM)	4 × 256 MB (256 MB Micron DDR3 memories MT41K256M8DA-125 IT:K) for storing data, and 256 MB (1 × 256 MB Micron DDR3 memory MT41K256M8DA-125 IT:K) for storing ECC bits.
SPI flash	A 1-gigabit SPI flash (Micron N25Q00AA13GSF40G) connected to SPI port 0 of the SmartFusion2 microcontroller subsystem (MSS), and another 1-gigabit SPI flash (Micron N25Q00AA13GSF40G) connected to the SmartFusion2 fabric.
Ethernet	Two RJ45 connectors (Ethernet jacks with built-in magnetics) interfacing with a Marvell 10/100/1000 BASE-T physical layer (PHY) chip—88E1304S—in Serial Gigabit Media Independent Interface (SGMII) mode. The Marvell PHY device, in turn, interfaces with the Ethernet port of the SmartFusion2 MSS (on-chip MAC and external PHY).
RVI header	RVI header for application programming and debugging using Keil ULINK or IAR J-Link.
Embedded FlashPro5	Embedded FlashPro5 for programming and debugging the SmartFusion2 FPGA using Microsemi tools.
Future Technology Devices International (FTDI) programmer	FTDI programmer interface (J33) to program the external SPI flash. An FTDI chip is also used to change the JTAG_SEL signal (*high* or *low*) remotely for switching between the RVI header and JTAG mode.
Embedded Trace Macro (ETM) cell header	ETM header for debugging.

Table 2 • **SmartFusion2 Advanced Development Board Components *(continued)***

PCI Express (PCIe) edge connector	PCIe edge connector with four lanes.
Light-emitting diodes (LEDs)	Eight active-high LEDs connected to some of the user I/Os for debugging.
Push-button reset	Push-button system reset for the SmartFusion2 device.
Push-button switches	Four push-button switches for testing and navigation.
FMC HPC connector (J30)	High pin count FMC header to connect the external daughter boards. Connector array socket 400 pins (40 × 10), 1.27 mm pitch. Unused MSIO pins routed from the SmartFusion2 device to the J30 connector.
FMC LPC connector (J60)	Low pin count FMC header to connect the external daughter boards. Connector array socket 160 pins (40 × 4), 1.27 mm. Unused MSIOD pins routed from the SmartFusion2 device to the J60 connector.
USB interface	USB Micro-AB connector, interfacing with the high speed USB2.0 ULPI transceiver chip USB3320, which, in turn, interfaces with USB-D port of the SmartFusion2 MSS.
DS1818 3.3V EconoReset	A simple three-pin voltage monitor and power-on reset that holds reset for 150 ms for stabilization after power returns to tolerance.
OSC-100	100 MHz clock oscillator with differential output.
OSC-125	125 MHz clock oscillator with differential output.
OSC-50	50 MHz clock oscillator.
OSC-32	32.768 KHz low-power oscillator.
FT4232H	USB-to-quad serial ports in various configurations.
TPS3808G09DBVR	Supervisory circuit that monitors system voltage of 0.9 V, asserting an open-drain reset signal when the sense voltage drops below a preset threshold or when the manual reset (MR) pin drops to a logical low.
I2C port header	16-pin header available for I2C0 and I2C1 interfaces of the SmartFusion2 device.

3 Installation and Settings

This section provides information about the software and hardware settings for the SmartFusion Advanced Development Kit.

3.1 Software Installation

Download and install the Microsemi Libero® SoC software v11.4 or later from the Microsemi website, and register for a free Gold license to the software. The Libero SoC v11.4 or later installer has FlashPro5 drivers. For instructions on how to install Libero SoC and SoftConsole, see *Libero Software Installation and Licensing Guide*.

For instructions on how to download and install Microsemi DirectCores, SGCores, and driver firmware cores, which must be installed on the PC where Libero SoC is installed, see *Installing IP Cores and Drivers User Guide*.

The SmartFusion2 FPGA is supported by the latest IAR Embedded Workbench from IAR Systems for ARM IP. It is also supported by the latest Keil MDK-ARM Microcontroller Advanced Development Kit.

3.2 Hardware Settings

This section provides information about default jumper settings, switches, LEDs, and DIP switches for the M2S150-ADV-DEV-KIT.

3.2.1 Jumper Settings

Connect the jumpers with the default settings specified in the following table to evaluate the pre-programmed demo design.

Table 3 • **Jumper Settings**

Jumper	Description	Pin	Default Settings
Power Supply			
J123	Jumper to select a core voltage (VDD_REG) of 1.0 V or 1.2 V.	Pin 1-2 for 1.0 V.	Open
		Pin 2-3 for 1.2 V.	Close
J353	Jumper to select a core voltage (VCCIO_HPC_VADJ) of 3.3 V, 2.5 V, 1.8 V, 1.5 V, or 1.2V.	Pin 1-2 for 3.3 V.	Closed
		Pin 3-4 for 2.5 V.	Open
		Pin 5-6 for 1.8 V.	Open
		Pin 7-8 for 1.5 V.	Open
		Pin 9-10 for 1.2 V.	Open
J354	Jumper to select a core voltage (VCCIO_LPC_VADJ) of 2.5 V, 1.8 V, 1.5 V, or 1.2V.	Pin 1-2 for 2.5 V.	Closed
		Pin 3-4 for 1.8 V.	Open
		Pin 5-6 for 1.5 V.	Open
		Pin 7-8 for 1.2 V.	Open
J116	Jumpers to select either SW7 input or signal ENABLE_FT4232 from FT4232H chip.	Pin 1-2 for **SW7** switch selection.	Closed
		Pin 2–3 for Enable_FT4232 signal control.	Open

Table 3 • **Jumper Settings *(continued)***

Clocks			
J10	Jumper to select switch-side MUX inputs of A or B to the line side.	Pin 1-2 (Input A to the line side) for external clock required to source the line side through FMC connector.	Open
		Pin 2-3 (Input B to the line side) for external clock required to source the line side through SMA connectors.	Open
J9	Jumper to select the output-enable control for the line side outputs.	Pin 1-2 (line-side output enabled).	Open
		Pin 2-3 (line-side output disabled).	Open
J8	Jumper to select the output-enable control for the line side outputs.	Pin 1-2 (line-side output enabled).	Closed
		Pin 2-3 (line-side output disabled).	Open
J11	Jumper to select switch-side MUX inputs of A or B to the line side.	Pin 1-2 (Input A to the line side), that is, on-board 125 MHz differential clock oscillator output is routed to line side.	Closed
		Pin 2-3 (Input B to the line side), that is, on-board 100 MHz differential clock oscillator output is routed to line side.	Open
Marvell PHY			
J14	Jumper to select either PHY_CONFIG1 or M2S_PHY_CONFIG1 for global hardware configuration (CONFIG[1]).	Pin 1-2 CONFIG [1] connects to P2_LED[2] pin of 88E1340S.	Open
		Pin 2-3 CONFIG [1] connects to SmartFusion2 J8 pin (MSIO80NB3).	Open
J15	Jumper to short AC test points for debugging. It is recommended not to connect this jumper; refer to the Marvell PHY Datasheet.	Two-pin header.	Open
J23	Jumper to provide the VBUS supply to USB when used in host mode.	Two-pin header.	Open
Programming			
J32	JTAG selection jumper to select RVI header or FP4 header for application debug.	Pin 1-2 FP4 for SoftConsole/FlashPro.	Closed
		Pin 2-3 RVI for Keil ULINK or IAR J-Link.	Open
		Pin 2-4 for JTAG_SEL pin to DD1 signal of FT4232H chip.	Open
J121	Jumper to select FTDI JTAG or SPI slave programming.	Pin 1-2 for FTDI JTAG programming.	Closed
		Pin 2-3 for FTDI SPI slave programming.	Open
J124	Jumper to select JTAG programming via FP4 or FTDI.	Pin 1-2 for JTAG programming via FTDI.	Open
		Pin 2-3 for JTAG programming via FP4.	Closed
J125	Jumper to select FTDI SPI-0 or FTDI SPI-1 slave programming	Pin 1-2 for FTDI SPI-1 slave programming.	Open
		Pin 2-3 for FTDI SPI-0 slave programming.	Open

Table 3 • Jumper Settings *(continued)*

J118	Jumper to select programming SPI-0 flash through FTDI SPI-0 (Port-B) or SmartFusion2 SPI-0.	Pin 1-2 for programming SPI-0 flash via SmartFusion2 SPI-0.	Closed
		Pin 2-3 for programming SPI-0 flash via FTDI SPI-0 (Port-B). J125 pin 2-3 must be shorted.	Open
J119	Jumper to select programming SPI-1 flash through FTDI SPI (Port-B) or SmartFusion2 SPI-1.	Pin 1-2 for programming SPI-1 flash via SmartFusion2 SPI-1.	Closed
		Pin 2-3 for programming SPI-1 flash via FTDI SPI (Port-B). J125 pin 1-2 must be shorted.	Open

For locations of various jumpers and test points on the SmartFusion2 Advanced Development Board, see Figure 20, page 72 and Figure 21, page 73.

3.2.2 LEDs

The following table lists the power supply and Ethernet LEDs.

Table 4 • LEDs

LED	Description
DS26	Indicates USB_5V supply
DS18	Indicates 0P75V_REG supply
DS19	Indicates 1P5V_REG supply
DS20	Indicates VDD_REG supply
DS21	Indicates 2P5V_LDO supply
DS22	Indicates VCCIO_LPC_VADJ supply
DS23	Indicates VCCIO_HPC_VADJ supply
DS24	Indicates 1P0V_PHY supply
DS25	Indicates 1P8V supply
DS28	Indicates 3P3V_LDO supply
DS17	Indicates 5P0V supply
DS29	Indicates 3P3V supply
DS16	Indicates 12P0V supply
DS27	Indicates VSS_BUS supply
DS8	Indicates that DS8 is connected to parallel LED output port 0 (P0_LED[0]) of Marvell PHY
DS9	Indicates that DS9 is connected to parallel LED output port 0 (P0_LED[2]) of Marvell PHY
DS10	Indicates that DS10 is connected to parallel LED output port 0 (P0_LED[3]) of Marvell PHY
DS14	Indicates that DS14 is connected to parallel LED output port 1 (P1_LED[0]) of Marvell PHY
DS13	Indicates that DS13 is connected to parallel LED output port 1 (P1_LED[1]) of Marvell PHY
DS12	Indicates that DS12 is connected to parallel LED output port 1 (P1_LED[2]) of Marvell PHY
DS11	Indicates that DS11 is connected to parallel LED output port 1 (P1_LED[3]) of Marvell PHY

3.2.3 Test Points

The following table lists USB, ground, and other test points.

Table 5 • **Test Points**

Test Point	Description
TP20, TP33,TP16	GND
TP7	VDD_REG
TP12	12 V
TP11	5 V
TP4	3.3 V
TP29	VCCIO_HPC_VADJ
TP28	VCCIO_LPC_VADJ
TP30	3P3V_LDO
TP31	2P5V_LDO
TP9	1.5 V
TP10	0.75 V
TP14	1.8 V
TP27	VDDIO for the USB device
TP24	PHY 1.0 V

3.3 Power Sources

The following table lists the key power supplies required for normal operation of the SmartFusion2 Advanced Development Kit.

Table 6 • **I/O Voltage Rails**

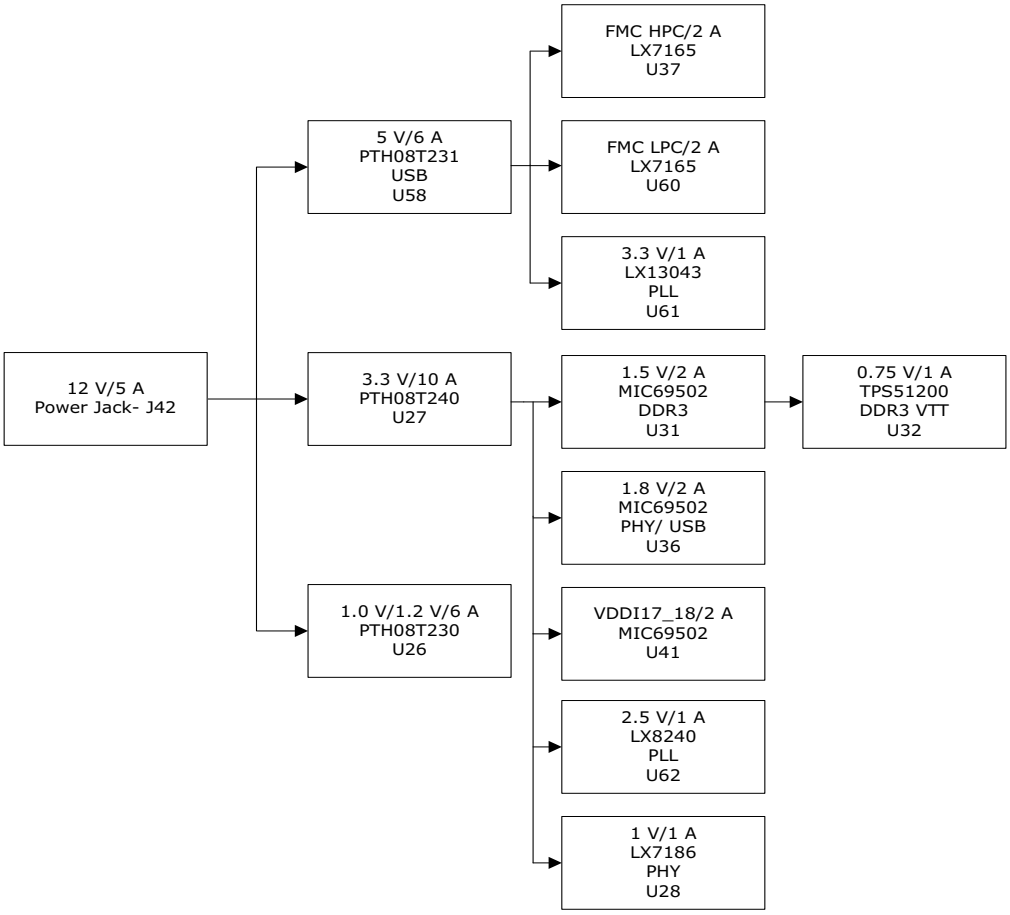
SmartFusion2 Bank	I/O Rail	Voltage
Bank0	VCCIO_HPC_VIO_B_M2S	3.3 V, 2.5 V, 1.8 V, 1.5 V, or 1.2 V
Bank1	2P5V_LDO	2.5 V
Bank2	1P5V_REG	1.5 V
Bank3	3P3V	3.3 V
Bank4	3P3V	3.3 V
Bank5	VCCIO_HPC_VIO_B_M2S	3.3 V, 2.5 V, 1.8 V, 1.5 V, or 1.2 V
Bank6	VCCIO_LPC_VADJ	2.5 V, 1.8 V, 1.5 V, or 1.2 V
Bank7	3P3V	3.3 V
Bank8	VCCIO_LPC_VADJ	2.5 V, 1.8 V, 1.5 V, or 1.2 V
Bank9	2P5V_LDO	2.5 V
Bank10	2P5V_LDO	2.5 V
Bank11	VCCIO_HPC_VADJ	3.3 V, 2.5 V, 1.8 V, 1.5 V, or 1.2 V
Bank12	2P5V_LDO	2.5 V
Bank13	2P5V_LDO	2.5 V
Bank14	VCCIO_HPC_VADJ	3.3 V, 2.5 V, 1.8 V, 1.5 V, or 1.2 V

Table 6 • **I/O Voltage Rails *(continued)***

Bank15	VCCIO_LPC_VADJ	2.5 V, 1.8 V, 1.5 V, or 1.2 V
Bank16	VCCIO_LPC_VADJ	2.5 V, 1.8 V, 1.5 V, or 1.2 V
Bank17	VCCIO_HPC_VADJ	3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V
Bank18	VCCIO_HPC_VADJ	3.3 V, 2.5 V, 1.8 V, 1.5 V, or1.2 V
VDD	VDD_REG	1.2 V or 1.0 V
VPP	3P3V_VPP	3.3 V
VREF1	VREF1	0.75 V
VREF2	0P75V_VTT_REF	0.75 V
SERDES_*x*_PLL_VDDA	PLL_SERDES*x*_VDDA	3.3 V
SERDES_*x*_L01_VDDAPLL	SERDESx_VDDPLL	2.5 V
SERDES_x_VDD	VDD_REG	1.2 V or 1.0 V

The following figure shows the voltage rails (12 V, 5 V, 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, 1.0 V, and 0.75 V) available in the SmartFusion2 Advanced Development Kit.

Figure 3 • **Voltage Rails in SmartFusion2 Advanced Development Kit**



4 Key Components Description and Operation

This section describes the key component interfaces of the SmartFusion2 Advanced Development Kit. For device datasheets, go to *http://www.microsemi.com/products/fpga-soc/design-resources/dev-kits/smartfusion2-kits*.

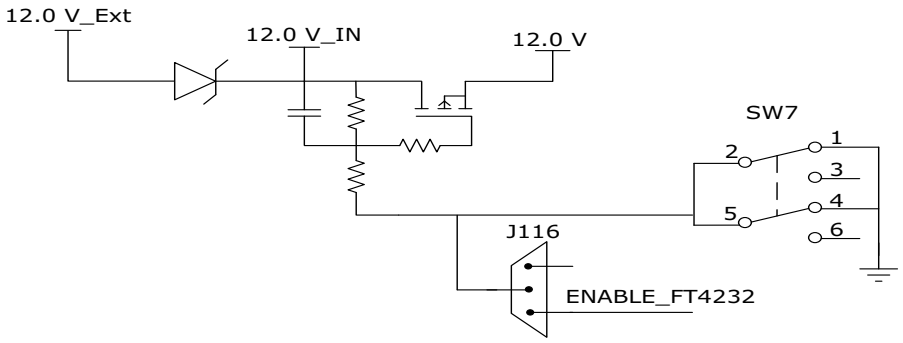
4.1 Powering Up the Board

The SmartFusion2 Advanced Development Board is powered using a 12 V external DC jack (12P0V_Ext), as shown in the following figure.

To power up the board:

1. Connect the 12 V power supply brick to the **J42** jumper to supply power to the board.
2. Switch ON the **SW7** power supply switch.

Figure 4 • **Powering Up the Board**



4.2 Current Measurement

This section provides information about current sensing in various modes.

4.2.1 1.0 V or 1.2 V Current Sensing for Normal Operation

For applications that require current measurement, high-precision operational amplifier circuitry (U59 with gain 100) is provided on the board to measure the output voltage at the **TP17** test point.

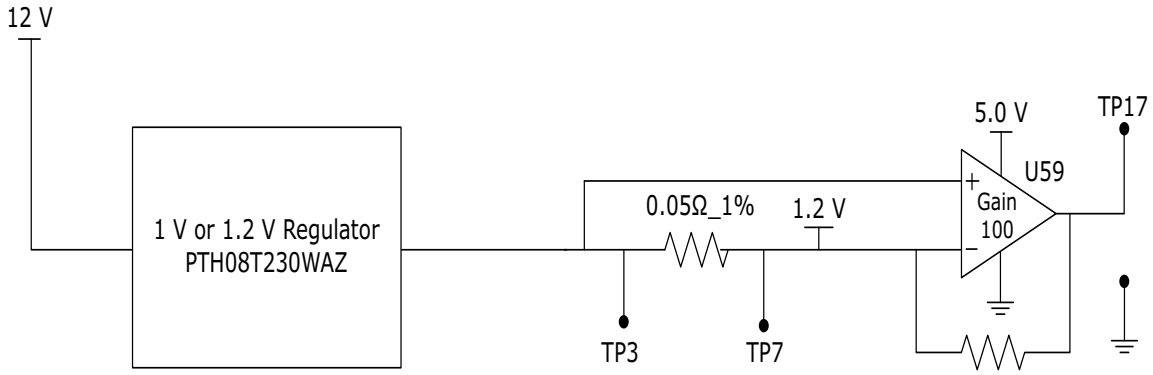
The following steps describe how to measure the core power.

1. Measure the output voltage (V_{OUT}) at TP17.
2. I = (V_{OUT}/5).
3. Core power consumed (P) = (1.2 V) × I.

For example, when the voltage measured across TP17 is 0.5 V, the core power consumed is 0.12 W.

The following figure shows the on-board core power measurement circuitry.

Figure 5 • **Core Power Measurement Circuitry**



4.2.2 1.2 V Current Sensing for Flash*Freeze Mode

The SmartFusion2 device consumes very less power in Flash*Freeze mode. The voltage across the sense resistor (0.05 Ω) must be measured directly using a precision digital multimeter that can read sub-millivolts. The **TP16** and **TP17** test points can be used to directly measure the voltage across the 1.2 V sense resistor.

To convert the voltage measured across a sense resistor to power, use the following equation.

$$\text{Power} = \left(\frac{\text{voltage\_in\_millivolts}}{0.05}\right) \times 1.2$$

Note: Accuracy is ± 10%.

4.3 Memory Interface

Dedicated I/Os for MSS DDR and fabric DDR are available in the SmartFusion2 device.

4.3.1 DDR3 SDRAM

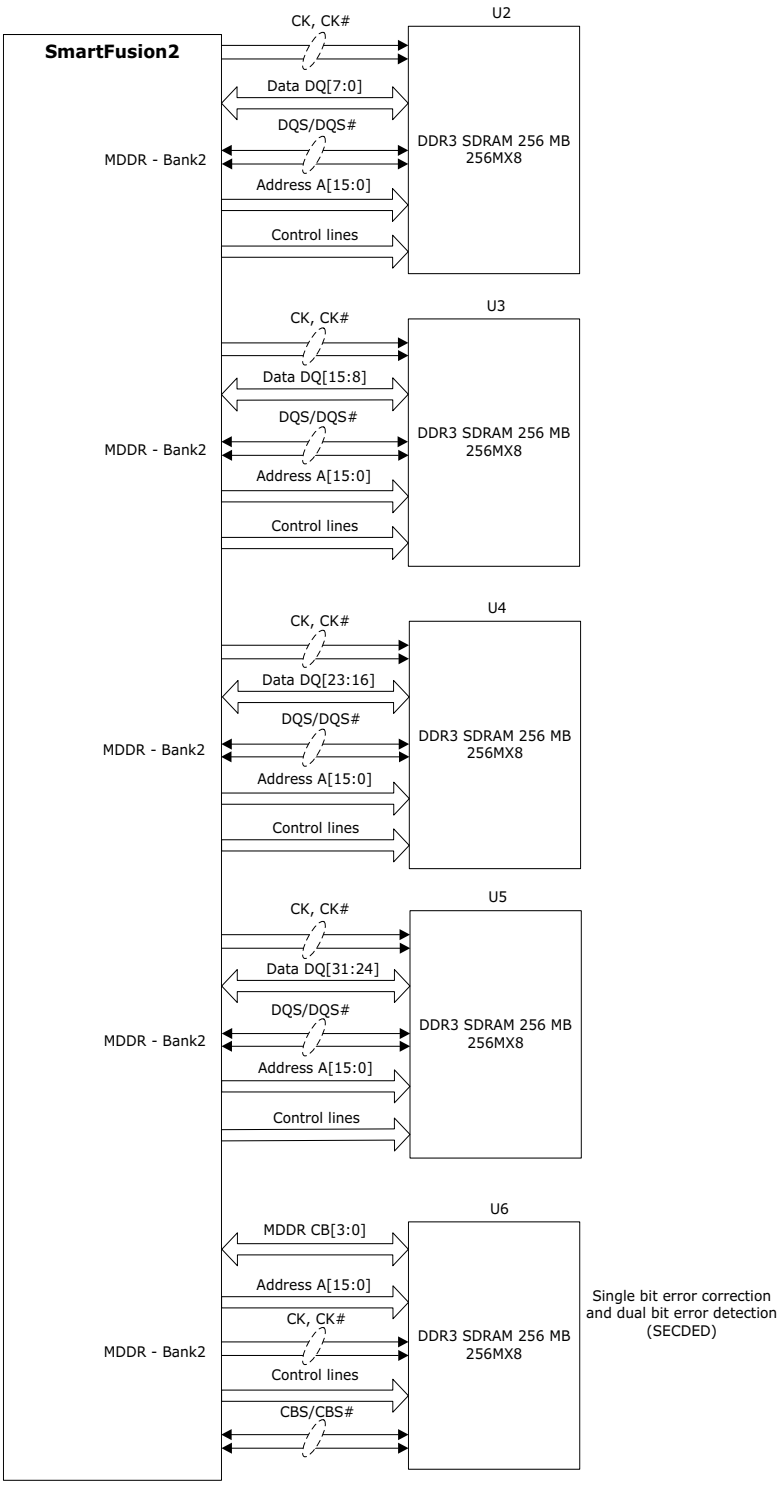
Four chips with 256 MB DDR3 memory are provided in the SmartFusion2 device as flexible volatile memory for user applications. Additionally, one chip with 256 MB DDR3 memory is provided for ECC. You can enable the SECDED feature using ECC. The DDR3 interface is implemented in Bank2.

DDR3 SDRAM specifications for the SmartFusion2 device are as follows.

- MT46H32M16LF: 32 Meg × 8 × 8 banks
- Density: 256 MB
- Clock rate: 800 MHz
- Data rate: DDR3 - 1600
- Total capacity: 1 GB across four chips

The following figure shows the SmartFusion2 memory interface.

Figure 6 • **SmartFusion2 Memory Interface**



For more information, see the Board Level Schematics document (provided separately).

4.4 SerDes Interface

The SmartFusion2 Advanced Development Kit has x4 SerDes interfaces. The SerDes block can be accessed using the PCIe edge connector, high-speed sub-miniature version-A (SMA) connectors, and/or an on-board FPGA mezzanine card (FMC) low pin count (LPC) connector (J60).

Note: All SerDes TXD pairs (SERDES0, SERDES1, SERDES2, and SERDES3) are capacitively coupled to the SmartFusion2 device. Serial AC-coupling capacitors are used to provide common-mode voltage independence.

For more information, see the Board Level Schematics document (provided separately).

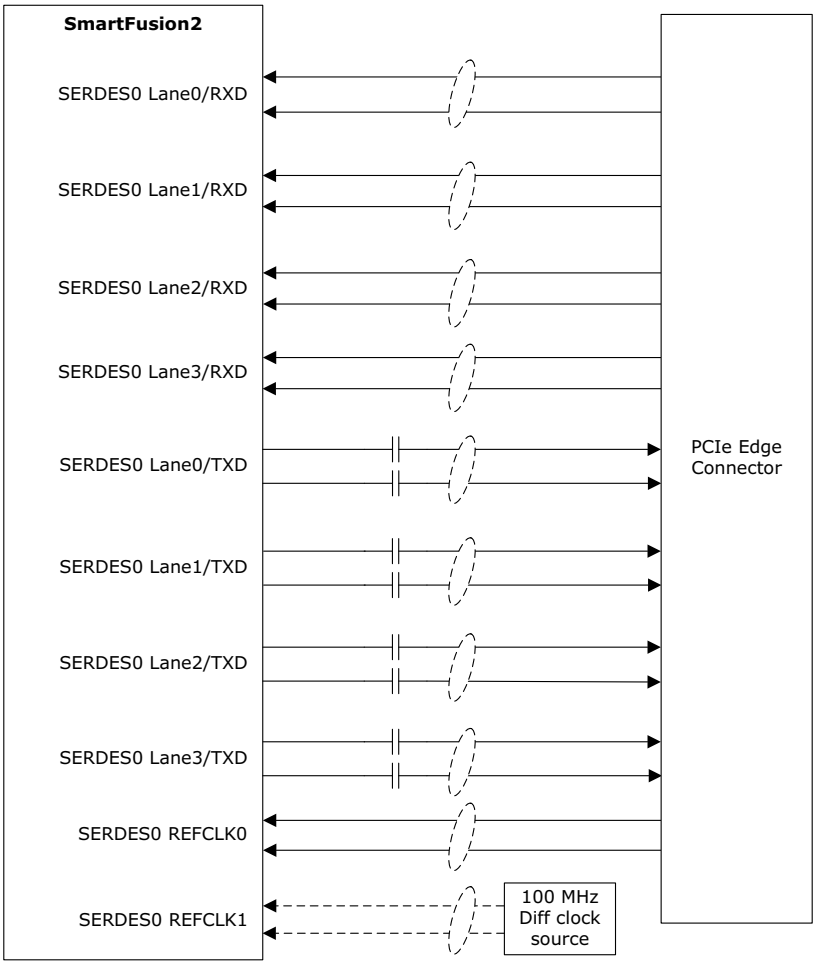
4.4.1 SERDES0 Interface

The SERDES0 interface (Lane 0,1, 2, or 3) is directly routed to the PCIe connector. The SerDes reference clocks are routed as follows.

- SERDES0 reference clock 0 is directly routed from the PCIe connector to the SmartFusion2 device.
- SERDES0 reference clock 1 is routed from the 100 MHz differential clock source (LVDS clock oscillator) through resistors.

The following figure shows the SERDES0 interface of the SmartFusion2 Advanced Development Board.

Figure 7 • **SERDES0 Interface**



Note: Mount R977 and R978 to source the clock from 100 MHz differential oscillator to the SERDES0 REFCLK1.

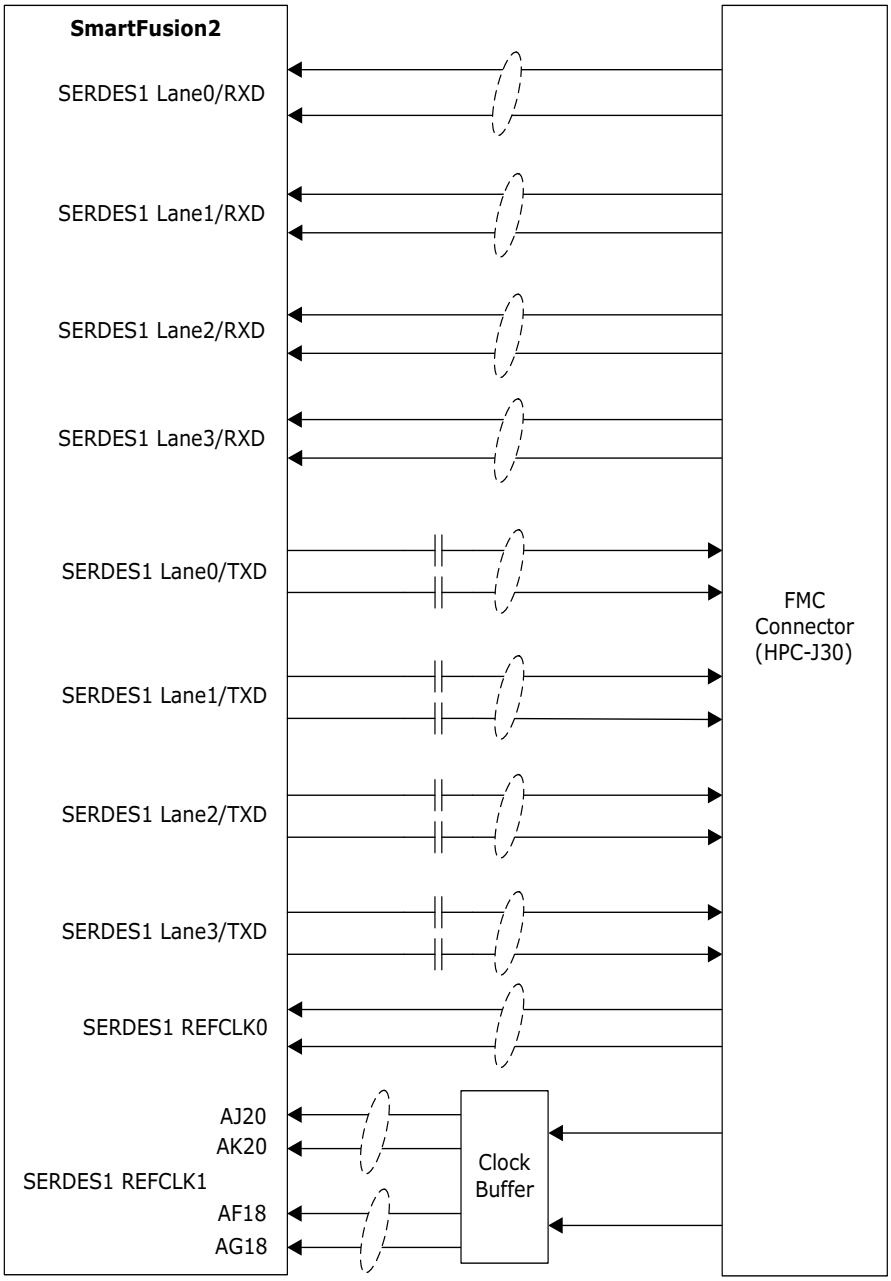
4.4.2 SERDES1 Interface

The SERDES1 interface (Lane 0, 1, 2, or 3) is routed to the FMC connector. The SerDes reference clocks are routed as follows.

- SERDES1 reference clock 0 is routed from the FMC connector.
- SERDES1 reference clock 1 is routed from the FMC connector through the clock buffer. The output of the clock buffer is additionally routed to SmartFusion2 Advanced Development Kit board pins AF18 and AG18.

The following figure shows the SERDES1 interface of the SmartFusion2 Advanced Development Board.

Figure 8 • **SERDES1 Interface**



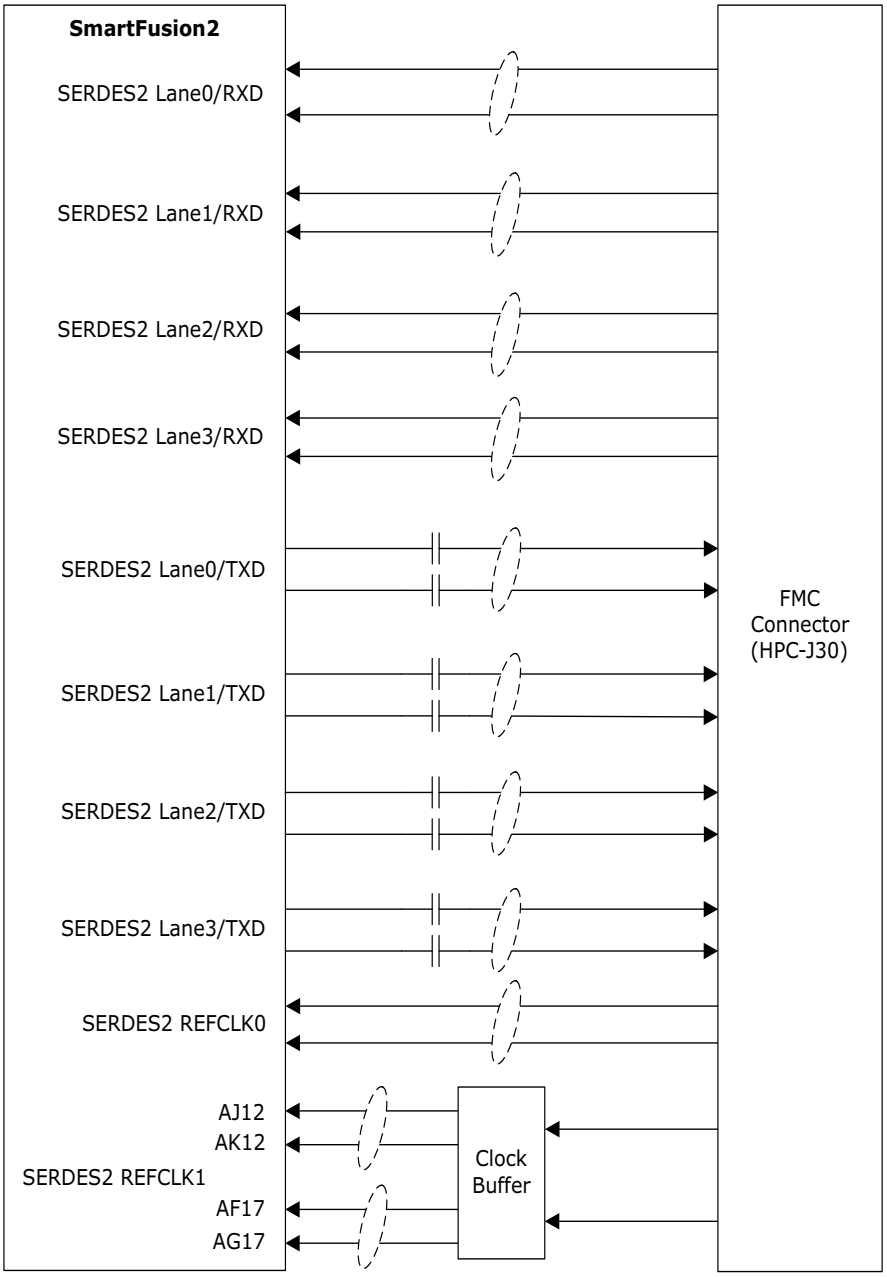
4.4.3 SERDES2 Interface

The SERDES2 interface (Lane 0, 1, 2, or 3) is routed to the FMC connector. The SerDes reference clocks are routed as follows.

- SERDES2 reference clock 0 is routed from the FMC connector.
- SERDES2 reference clock 1 is routed from the FMC connector through the clock buffer. The output of the clock buffer is additionally routed to SmartFusion2 Advanced Development Kit board pins AE17 and AF17.

The following figure shows the SERDES2 interface of the SmartFusion2 Advanced Development Board.

Figure 9 • **SERDES2 Interface**



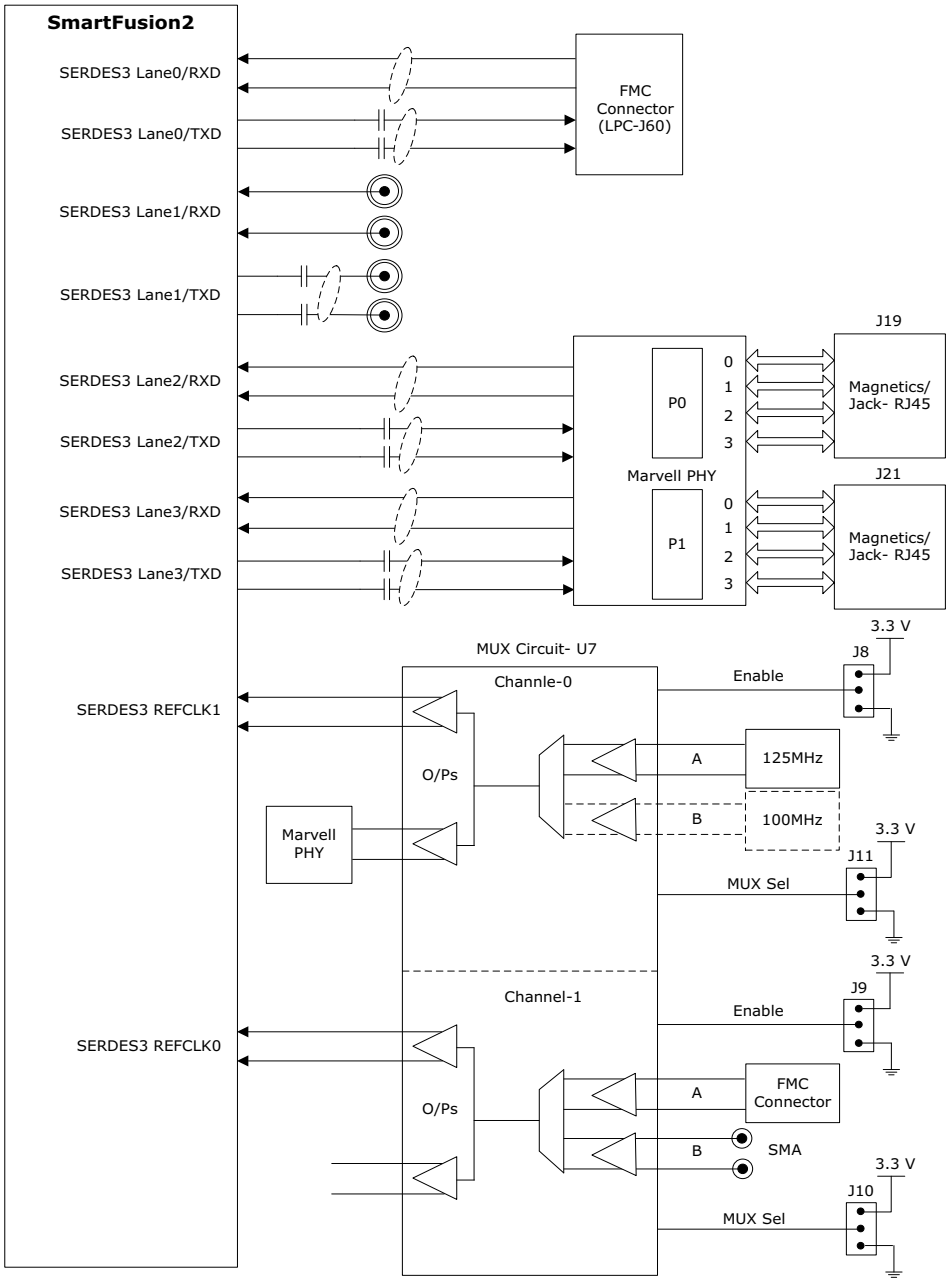
4.4.4 SERDES3 Interface

The SERDES3 lanes are connected as follows.

- Lane 0 is connected to the FMC connector.
- Lane 1 is connected to the SMA connectors.
- Lanes 2 and 3 are connected to the Marvell PHY device ports 0 and 1, respectively.
- SERDES3 reference clock 0 is connected from FMC connector or SMA connector through MUX.
- SERDES3 reference clock 1 is connected from 125 MHz or 100 MHz through MUX.

The following figure shows the SERDES3 interface of the SmartFusion2 Advanced Development Board.

Figure 10 • **SERDES3 Interface**

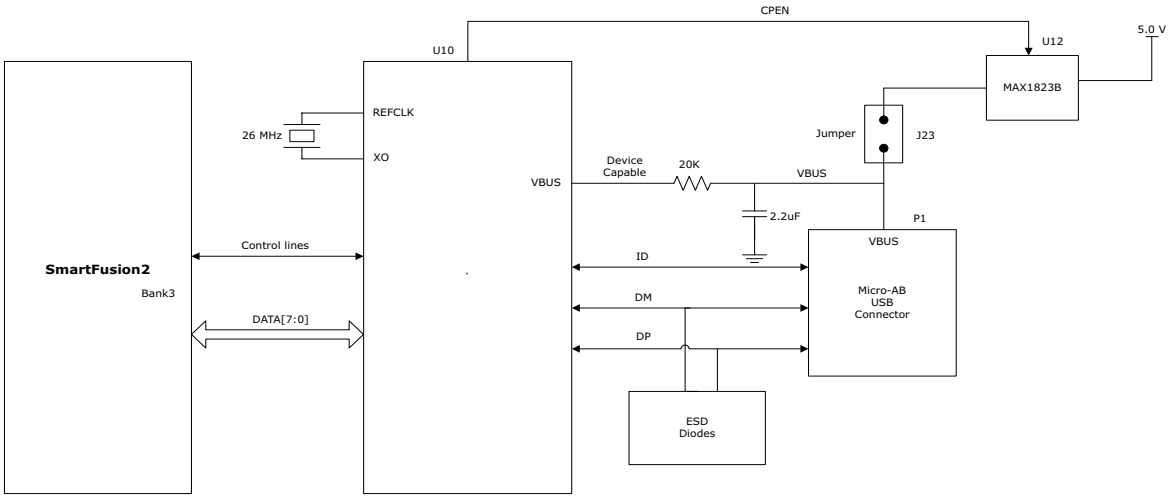


4.5 USB Interface

The following figure shows the USB interface of the SmartFusion2 Advanced Development Board. The SMSC USB3320 shown in the following figure is a high-speed USB 2.0 ULPI transceiver that provides the industry standard UTMI+ low pin interface to connect the USB transceiver to the link. CPEN (shown in the figure) is the external 5 V supply enable pin that controls the external VBUS power switch.

In the SmartFusion2 Advanced Development Kit, the USB interface can operate in host, device, and OTG modes. To use device mode, J23 can either be in open or shorted. To use host or OTG mode, pins 1 and 2 of the **J23** jumper must be closed.

Figure 11 • **USB Interface**



For more information, see the Board Level Schematics document (provided separately).

4.6 Marvell PHY (88E1340S)

The SmartFusion2 Advanced Development Kit uses the on-board Marvell Alaska PHY device 88E1340S for Ethernet communications at 10 or 1000 Mbps. The device has four independent gigabit Ethernet transceivers; however, the board uses only two of these transceivers. Each transceiver performs all the PHY functions for 100BASE-TX and 1000BASE-T full-duplex or half-duplex Ethernet on a CAT5 twisted-pair cable. The PHY device is connected to a user-provided Ethernet cable through an RJ45 connector with built-in magnetics.

Device 88E1340S supports Quad SGMII for direct connection to a SmartFusion2 chip. It is configured through the CONFIG [3:0] and CLK_SEL [1:0] pins.

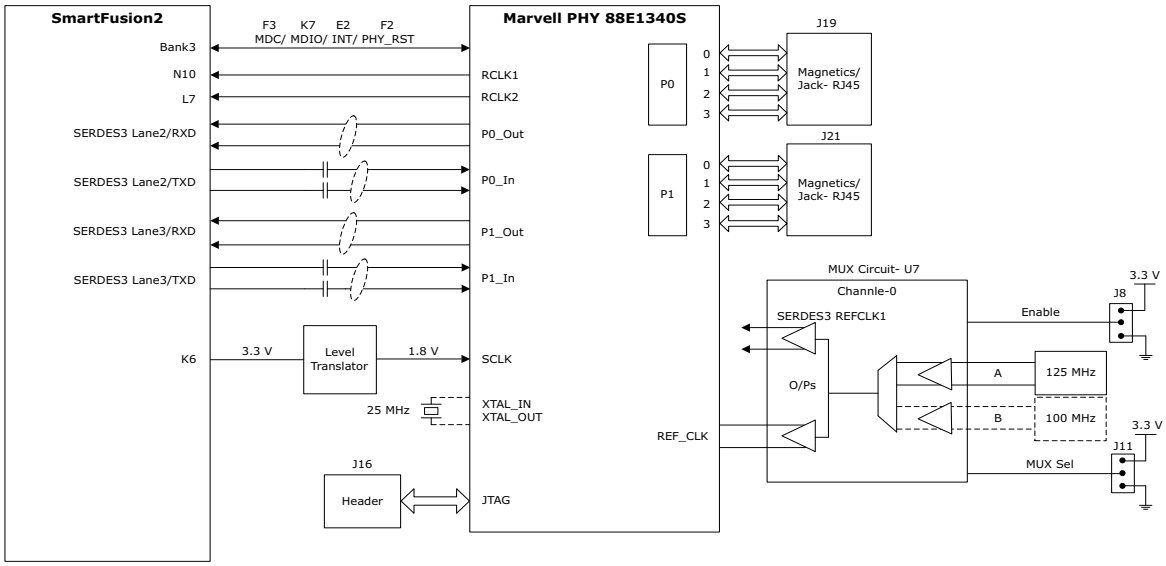
The CLK_SEL [1:0] pin is used to select the reference clock input. On the board, the status of the CLK_SEL0 pin is *high* and the status of the CLK_SEL1 pin is *low*. REF_CLK is a 125 MHz reference differential clock input (Y11). It consists of LVDS differential inputs with a 100 Ω differential internal termination resistor.

Key features of Marvell PHY 88E1340S are as follows.

- RCLK: Gigabit recovered clock
- SCLK: 25 MHz synchronous input reference clock
- Expected reference clock (REF_CLK) specifications:
  - Voltage level: 3.3 (± 0.3) V
  - Differential LVDS
    - Symmetry: 50% (± 10%)
    - Rise/fall time: Maximum 1 ns @ 20% to 80% of supply (3.3 V)
    - Output voltage levels: 0 = 0.90 minimum, 1.10 typical; 1 = 1.43 typical, 1.60 maximum
    - Differential output voltage: 247 mV minimum, 454 mV maximum

The following figure shows the SmartFusion2 Marvell PHY interface.

Figure 12 • **Marvell PHY Interface**



For more information, see the Board Level Schematics document (provided separately).

4.7 Programming

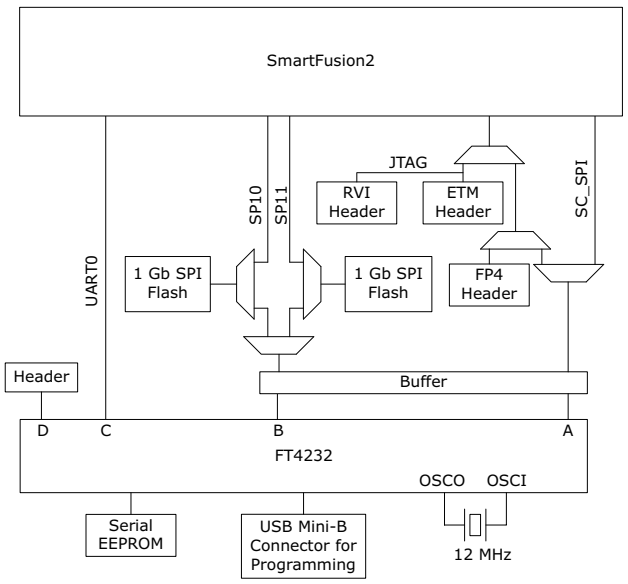
SmartFusion2 SoC FPGAs support multiple programming interfaces and can address a wide range of platform requirements. A SmartFusion2 device can be programmed through the JTAG and SPI interfaces.

The dedicated programming SPI port can operate in SPI slave or SPI master modes.

For more information, see *SmartFusion2 and IGLOO2 Programming User Guide*.

The following figure shows the programming interface of the SmartFusion2 Advanced Development Board.

Figure 13 • **Programming Interface**



JTAG_SEL: The JTAG state machine is multiplexed with the CM3 debug port. JTAG_SEL is used to switch between JTAG programming (high) and CM3 debug (low). When using the CM3 debug port, an option is available to switch to serial wire debug port.

FLASH_GOLDEN_N: This signal is always tied high to the 3.3V VCCIO_HPC_VADJ supply. It indicates that the SPI is in slave mode.

RVI Header: A 10 × 2 RVI header is provided on the board for debugging. This header allows plugging in the Keil ULINK debugger or IAR J-Link debugger to easily debug or configure the Cortex-M3 processor during board power-up.

FlashPro4 Programming Header: The SmartFusion2 device on this Advanced Development Kit can be programmed using a FlashPro4 programmer. In addition, SoftConsole uses FlashPro4 for software debugging.

The following table lists jumpers to be selected for various types of programming.

Table 7 • **Programming Jumper Selection**

J121	J124	J125	J32	Function
X	X	X	L	IAR debugging
X	L	X	H	FP4 JTAG programming
H	H	X	H	FTDI JTAG programming (embedded FlashPro5 programming)
L	X	X	H	FTDI SPI slave programming
X	X	L	X	FTDI SPI-0 programming
X	X	H	X	FTDI SPI-1 programming

For more information, see the Board Level Schematics document (provided separately).

4.8 FTDI Interface

The FT4232H chip is a USB 2.0 high-speed (480 Mbps) to UART/MPSSE interface with the following key features.

- Single-chip USB-to-quad serial ports in various configurations
- Entire USB protocol handled on the chip without requiring USB-specific firmware programming
- USB 2.0 high-speed (480 Mbps) and full-speed (12 Mbps) compatibility
- Two MPSSEs on channel A and channel B to simplify synchronous serial protocol (USB to JTAG, I2C, SPI, or bit-bang) design
- Fully assisted hardware handshaking and X-On/X-Off software handshaking
- +1.8 V (chip core) and +3.3 V I/O interfacing with +5 V tolerance

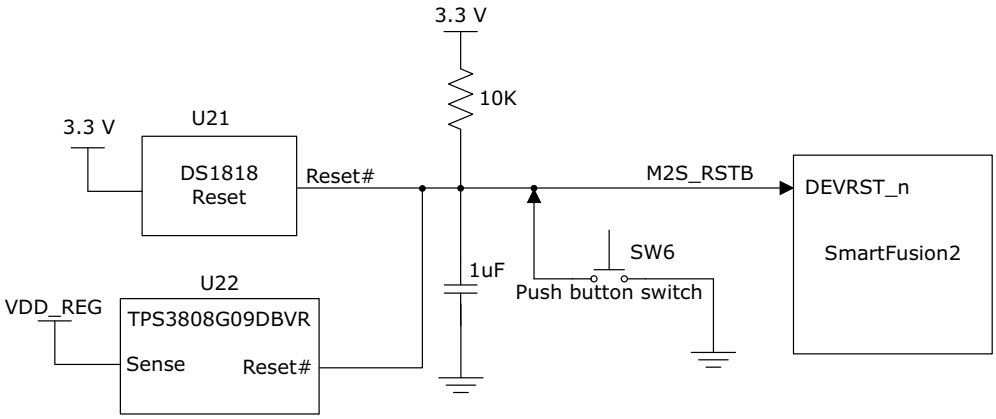
4.9 System Reset

The M2S_RSTB signal (active-low) is generated by the **SW6** push-button switch, or by the U21 (DS1818) or U22 (TPS3808G09) chips. DEVRST_N is an input-only reset pad that allows assertion of a full reset to the chip at any time.

DS1818 maintains reset till 150 milliseconds after the 3.3 V supply returns to intolerance. The TPS3808G09DBVR device monitors the voltage at the VDD_REG terminal. If the voltage at this terminal sense-drops below the threshold voltage of 0.9 V, the M2S_RSTB signal is asserted.

The following figure shows the system reset interface of the SmartFusion2 Advanced Development Board.

Figure 14 • **System Reset Interface**



For more information, see the Board Level Schematics document (provided separately).

4.10 Clock Sources

This section provides information about the clock sources available in the SmartFusion2 Advanced Development Kit.

4.10.1 50 MHz Clock Oscillator

A 50 MHz clock oscillator with an accuracy of +/-50 ppm is available on the board. This clock oscillator is connected to the FPGA fabric to provide a system reference clock.

An on-chip SmartFusion2 PLL can be configured to generate a wide range of high-precision clock frequencies.

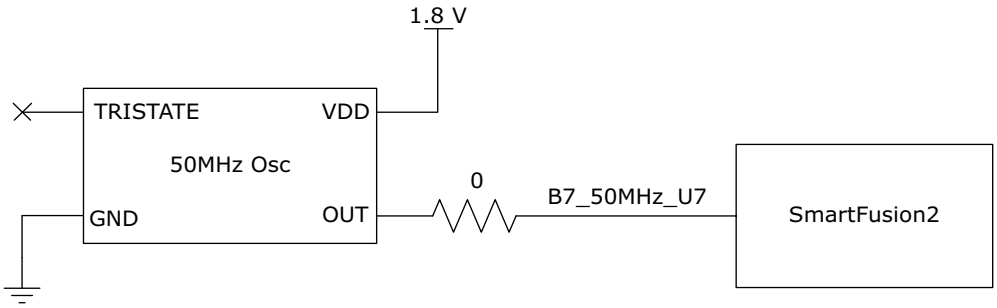
The following table provides package and pin details of the 50 MHz oscillator.

Table 8 • **50 MHz Clock**

SmartFusion2 Advanced Development Kit Pin Name	SmartFusion2 Package Number	SmartFusion2 Device Pin Name
50MHZ_SECLK_B4_P1	P1	MSIO39PB4/CCC_NE0_CLKI1

The following figure shows the 50 MHz clock oscillator interface.

Figure 15 • **50 MHz Clock Oscillator Interface**



For more information, see the Board Level Schematics document (provided separately).

4.10.2 100 MHz Clock Oscillator

A 100 MHz LVDS clock oscillator operating at 3.3 V with an accuracy of +/-50 ppm is available on the board. This clock oscillator is connected to the FPGA fabric M1 and N1 pins.

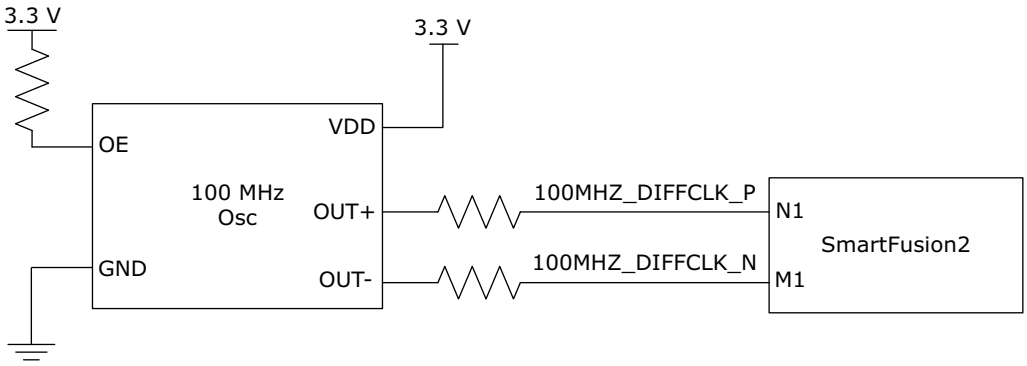
The following table provides package and pin details of the 100 MHz oscillator.

Table 9 • **100 MHz Clock**

SmartFusion2 Advanced Development Kit Pin Name	SmartFusion2 Package Pin Number	SmartFusion2 Device Pin Name
100MHZ_DIFFCLK_P	N1	MSIO40PB4/CCC_NE1_CLKI1
100MHZ_DIFFCLK_N	M1	MSIO40NB4

The following figure shows the 100 MHz clock oscillator interface.

Figure 16 • **100 MHz Clock Oscillator Interface**



For more information, see the Board Level Schematics document (provided separately).

4.11 User Interface

The SmartFusion2 Advanced Development Board UI has user LEDs as well as push-button switches.

4.11.1 User LEDs

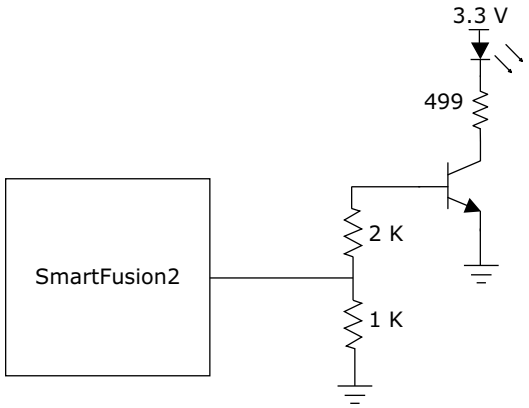
The board has eight active-high LEDs connected to the SmartFusion2 device that can be used to debug applications. The following table lists the on-board user LEDs.

Table 10 • **LEDs**

SmartFusion2 Advanced Development Board Pin	SmartFusion2 Package Pin Number	SmartFusion2 Device Pin Name
DS0	D26	DDRIO149PB1/FDDR_DQS2
DS1	F26	DDRIO150PB1/FDDR_DQ18
DS2	A27	DDRIO148PB1/FDDR_DM_RDQS2
DS3	C26	DDRIO149NB1/FDDR_DQS2_N
DS4	C28	DDRIO151PB1/FDDR_DQ16
DS5	B27	DDRIO148NB1/FDDR_DQ20
DS6	C27	DDRIO151NB1/FDDR_DQ17
DS7	E26	DDRIO150NB1/FDDR_DQ19

The following figure shows the LED interface of the SmartFusion2 Advanced Development Board.

Figure 17 • **LED Interface**



For more information, see the Board Level Schematics document (provided separately).

4.11.2 Push-Button Switches

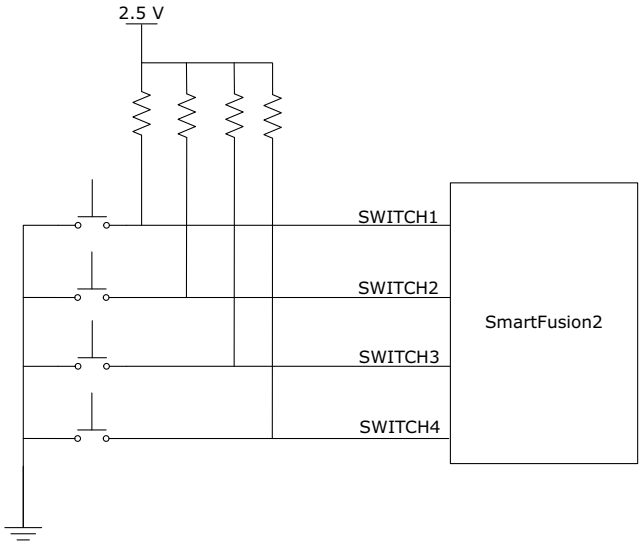
The SmartFusion2 Advanced Development Kit comes with five push-button tactile switches that are connected to the SmartFusion2 device. The following table lists the on-board push-button switches.

Table 11 • **Push-Button Switches**

SmartFusion2 Advanced Development Board Pin	SmartFusion2 Package Pin Number	SmartFusion2 Device Pin Name
SWITCH1	J25	DDRIO156PB1/FDDR_DQ10
SWITCH2	H25	DDRIO156NB1/FDDR_DQ11
SWITCH3	J24	DDRIO157PB1/FDDR_DQ8
SWITCH4	H23	DDRIO157NB1/FDDR_DQ9
SW6	AE5	System Reset

The following figure shows the switches interface of the SmartFusion2 Advanced Development Board.

Figure 18 • **Switches Interface**



For more information, see the Board Level Schematics document (provided separately).

4.11.3 Slide Switches - DPDT

The **SW7** switch powers the device ON or OFF switch from the +12 V external DC jack (J42).

4.11.4 DIP Switch - SPST

The **SW5** DIP switch has eight connections to the SmartFusion2 device.

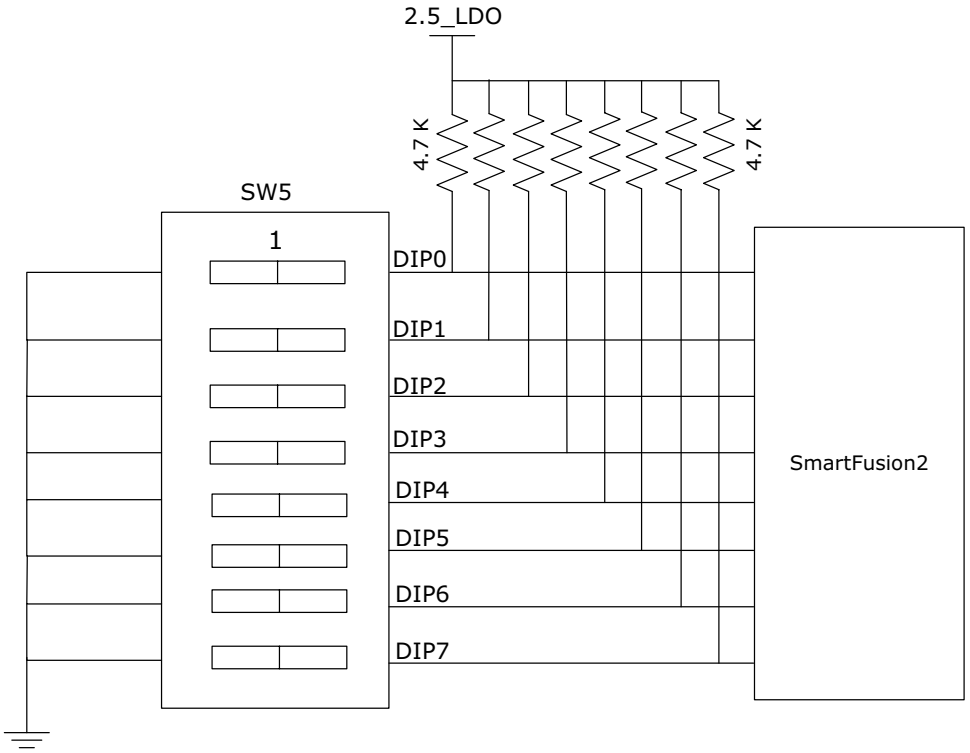
The following table lists the on-board DIP switches.

Table 12 • **DIP Switches**

SmartFusion2 Advanced Development Board Pin	SmartFusion2 Package Pin Number	SmartFusion2 Device Pin Name
DIP0	F25	DDRIO152PB1/FDDR_DQ14
DIP1	G25	DDRIO152NB1/FDDR_DQ15
DIP2	J23	DDRIO153PB1/FDDR_DQ12
DIP3	J22	DDRIO153NB1/FDDR_DQ13
DIP4	G27	DDRIO154PB1/FDDR_TMATCH_0_IN
DIP5	H27	DDRIO154NB1/FDDR_DM_RDQS1
DIP6	F23	DDRIO155PB1/FDDR_DQS1
DIP7	G23	DDRIO155NB1/FDDR_DQS1_N

The following figure shows the SPST interface of the SmartFusion2 Advanced Development Board.

Figure 19 • **SPST Interface**



For more information, see the Board Level Schematics document (provided separately).

4.11.5 FMC Connectors

SmartFusion2 Advanced Development Kit has HPC (J30) and LPC (J60) FMC connectors on the board for connecting the daughter cards to enable future expansion of interfaces.

4.11.5.1 FMC HPC Connector (J30)

The SmartFusion2 MSIOs from banks 0, 3, 5, 6, 8, 11, 14, 17, and 18, and the SERDES1 and SERDES2 signals are routed to the FMC connector for the application to be developed.

If the FMC daughter board is designed according to VITA standards, Bank0 and Bank5 I/Os draw power from the FMC daughter board. If it is not designed according to VITA standards, these I/Os can be powered from the on-board U37 regulator, by mounting an R1216 resistor.

The following table provides the FMC HPC header pinout details.

Table 13 • **FMC HPC Connector (J30) Pinout**

FMC Pin Number-J30	FMC Net Name	SmartFusion2 Pin Number	SmartFusion2 Pin name
A1	GND		
A2	FMC_HPC_SERDES2_RXD2_P	AM13	SERDES_2_RXD2_P
A3	FMC_HPC_SERDES2_RXD2_N	AL13	SERDES_2_RXD2_N
A4	GND		
A5	GND		
A6	FMC_HPC_SERDES2_RXD1_P	AM15	SERDES_2_RXD1_P
A7	FMC_HPC_SERDES2_RXD1_N	AL15	SERDES_2_RXD1_N
A8	GND		
A9	GND		
A10	FMC_HPC_SERDES2_RXD0_P	AM17	SERDES_2_RXD0_P
A11	FMC_HPC_SERDES2_RXD0_N	AL17	SERDES_2_RXD0_N
A12	GND		
A13	GND		
A14	FMC_HPC_SERDES1_RXD3_P	AL19	SERDES_1_RXD3_P
A15	FMC_HPC_SERDES1_RXD3_N	AM19	SERDES_1_RXD3_N
A16	GND		
A17	GND		
A18	FMC_HPC_SERDES1_RXD2_P	AL21	SERDES_1_RXD2_P
A19	FMC_HPC_SERDES1_RXD2_N	AM21	SERDES_1_RXD2_N
A20	GND		
A21	GND		
A22	FMC_HPC_SERDES2_TXD2_P	AN12	SERDES_2_TXD2_P
A23	FMC_HPC_SERDES2_TXD2_N	AP12	SERDES_2_TXD2_N
A24	GND		
A25	GND		
A26	FMC_HPC_SERDES2_TXD1_P	AN14	SERDES_2_TXD1_P
A27	FMC_HPC_SERDES2_TXD1_N	AP14	SERDES_2_TXD1_N

Table 13 • **FMC HPC Connector (J30) Pinout *(continued)***

A28	GND		
A29	GND		
A30	FMC_HPC_SERDES2_TXD0_P	AN16	SERDES_2_TXD0_P
A31	FMC_HPC_SERDES2_TXD0_N	AP16	SERDES_2_TXD0_N
A32	GND		
A33	GND		
A34	FMC_HPC_SERDES1_TXD3_P	AP18	SERDES_1_TXD3_P
A35	FMC_HPC_SERDES1_TXD3_N	AN18	SERDES_1_TXD3_N
A36	GND		
A37	GND		
A38	FMC_HPC_SERDES1_TXD2_P	AP20	SERDES_1_TXD2_P
A39	FMC_HPC_SERDES1_TXD2_N	AN20	SERDES_1_TXD2_N
A40	GND		
B1	NC		
B2	GND		
B3	GND		
B4	NC		
B5	NC		
B6	GND		
B7	GND		
B8	NC		
B9	NC		
B10	GND		
B11	GND		
B12	FMC_HPC_SERDES1_RXD0_P	AL25	SERDES_1_RXD0_P
B13	FMC_HPC_SERDES1_RXD0_N	AM25	SERDES_1_RXD0_N
B14	GND		
B15	GND		
B16	FMC_HPC_SERDES1_RXD1_P	AL23	SERDES_1_RXD1_P
B17	FMC_HPC_SERDES1_RXD1_N	AM23	SERDES_1_RXD1_N
B18	GND		
B19	GND		
B20	FMC_HPC_SERDES1_REFCLK0_P	AJ22	MSIOD271PB12/SERDES_1_REFCLK0_P
B21	FMC_HPC_SERDES1_REFCLK0_N	AK22	MSIOD271NB12/SERDES_1_REFCLK0_N
B22	GND		
B23	GND		
B24	NC		
B25	NC		
B26	GND		

Table 13 • **FMC HPC Connector (J30) Pinout *(continued)***

B27	GND		
B28	NC		
B29	NC		
B30	GND		
B31	GND		
B32	FMC_HPC_SERDES1_TXD0_P	AP24	SERDES_1_TXD0_P
B33	FMC_HPC_SERDES1_TXD0_N	AN24	SERDES_1_TXD0_N
B34	GND		
B35	GND		
B36	FMC_HPC_SERDES1_TXD1_P	AP22	SERDES_1_TXD1_P
B37	FMC_HPC_SERDES1_TXD1_N	AN22	SERDES_1_TXD1_N
B38	GND		
B39	GND		
B40	NC		
C1	GND		
C2	FMC_HPC_SERDES2_TXD3_P	AN10	SERDES_2_TXD3_P
C3	FMC_HPC_SERDES2_TXD3_N	AP10	SERDES_2_TXD3_N
C4	GND		
C5	GND		
C6	FMC_HPC_SERDES2_RXD3_P	AM11	SERDES_2_RXD3_P
C7	FMC_HPC_SERDES2_RXD3_N	AL11	SERDES_2_RXD3_N
C8	GND		
C9	GND		
C10	HPC_LA06_M32_191P_B18	M32	MSIO191PB18
C11	HPC_LA06_M31_191N_B18	M31	MSIO191NB18
C12	GND		
C13	GND		
C14	HPC_LA10_T23_206P_B17	T23	MSIO206PB17
C15	HPC_LA10_T24_206N_B17	T24	MSIO206NB17
C16	GND		
C17	GND		
C18	HPC_LA14_P29_198P_B17	P29	MSIO198PB17
C19	HPC_LA14_P28_198N_B17	P28	MSIO198NB17
C20	GND		
C21	GND		
C22	HPC_LA18_CC_U29_215P_B17	U29	MSIO215PB17/CCC_NW1_CLKI0
C23	HPC_LA18_CC_U30_215N_B17	U30	MSIO215NB17
C24	GND		
C25	GND		

Table 13 • **FMC HPC Connector (J30) Pinout *(continued)***

C26	HPC_LA27_P34_208P_B17	P34	MSIO208PB17
C27	HPC_LA27_N34_208N_B17	N34	MSIO208NB17
C28	GND		
C29	GND		
C30	I2C0_SCL	K10	MSIO81NB3/I2C_0_SCL/GPIO_31_B/USB_DATA1_C
C31	I2C0_SDA	K9	MSIO81PB3/I2C_0_SDA/GPIO_30_B/USB_DATA0_C
C32	GND		
C33	GND		
C34	GND		
C35	12P0V		
C36	GND		
C37	12P0V		
C38	GND		
C39	3P3V		
C40	GND		
D1	HPC_PG_C2M_H6_77N_B3	H6	MSIO77NB3/MMUART_0_DSR/GPIO_20_B
D2	GND		
D3	GND		
D4	FMC_HPC_SERDES2_REFCLK0_P	AK14	MSIOD277PB10/SERDES_2_REFCLK0_P
D5	FMC_HPC_SERDES2_REFCLK0_N	AJ14	MSIOD277NB10/SERDES_2_REFCLK0_N
D6	GND		
D7	GND		
D8	HPC_LA01_CC_U27_216P_B17	U27	MSIO216PB17/CCC_NW0_CLKI0
D9	HPC_LA01_CC_U26_216N_B17	U26	MSIO216NB17
D10	GND		
D11	HPC_LA05_N23_186P_B18	N23	MSIO186PB18
D12	HPC_LA05_N24_186N_B18	N24	MSIO186NB18
D13	GND		
D14	HPC_LA09_R23_200P_B17	R23	MSIO200PB17
D15	HPC_LA09_R24_200N_B17	R24	MSIO200NB17
D16	GND		
D17	HPC_LA13_R26_202P_B17	R26	MSIO202PB17
D18	HPC_LA13_R25_202N_B17	R25	MSIO202NB17
D19	GND		
D20	HPC_LA17_CC_U31_213P_B17	U31	MSIO213PB17/GB6/CCC_NW1_CLKI1
D21	HPC_LA17_CC_U32_213N_B17	U32	MSIO213NB17
D22	GND		
D23	HPC_LA23_T33_212P_B17	T33	MSIO212PB17

Table 13 • **FMC HPC Connector (J30) Pinout *(continued)***

D24	HPC_LA23_T32_212N_B17	T32	MSIO212NB17
D25	GND		
D26	HPC_LA26_L33_190P_B18	L33	MSIO190PB18
D27	HPC_LA26_L32_190N_B18	L32	MSIO190NB18
D28	GND		
D29	HPC_TCK		
D30	HPC_TDI		
D31	HPC_TDO		
D32	3P3V		
D33	HPC_TMS		
D34	HPC_TRST_L		
D35	GND		
D36	3P3V		
D37	GND		
D38	3P3V		
D39	GND		
D40	3P3V		
E1	GND		
E2	HPC_HA01_CC_AF16_276P_B11	AF16	MSIO276PB11/GB11/VCCC_SE0_CLKI
E3	HPC_HA01_CC_AG16_276N_B11	AG16	MSIO276NB11
E4	GND		
E5	GND		
E6	HPC_HA05_AA3_17P_B6	AA3	MSIO17PB6
E7	HPC_HA05_AA2_17N_B6	AA2	MSIO17NB6
E8	GND		
E9	HPC_HA09_AJ2_285P_B8	AJ2	MSIO285PB8
E10	HPC_HA09_AH3_285N_B8	AH3	MSIO285NB8
E11	GND		
E12	HPC_HA13_AH6_283P_B8	AH6	MSIO283PB8
E13	HPC_HA13_AH5_283N_B8	AH5	MSIO283NB8
E14	GND		
E15	HPC_HA16_AG7_284P_B8	AG7	MSIO284PB8
E16	HPC_HA16_AF7_284N_B8	AF7	MSIO284NB8
E17	GND		
E18	HPC_HA20_AB8_8P_B6	AB8	MSIO8PB6
E19	HPC_HA20_AB7_8N_B6	AB7	MSIO8NB6
E20	GND		
E21	HPC_HB03_W1_20P_B5	W1	MSIO20PB5
E22	HPC_HB03_W2_20N_B5	W2	MSIO20NB5

Table 13 • **FMC HPC Connector (J30) Pinout *(continued)***

E23	GND		
E24	HPC_HB05_Y2_19P_B5	Y2	MSIO19PB5
E25	HPC_HB05_Y1_19N_B5	Y1	MSIO19NB5
E26	GND		
E27	HPC_HB09_V4_30P_B5	V4	MSIO30PB5/USB_DATA0_B
E28	HPC_HB09_V5_30N_B5	V5	MSIO30NB5/USB_DATA1_B
E29	GND		
E30	HPC_HB13_U2_29P_B5	U2	MSIO29PB5/USB_STP_B
E31	HPC_HB13_U3_29N_B5	U3	MSIO29NB5/USB_NXT_B
E32	GND		
E33	HPC_HB19_H31_175P_B0	H31	MSIO175PB0
E34	HPC_HB19_G31_175N_B0	G31	MSIO175NB0
E35	GND		
E36	HPC_HB21_L25_174P_B0	L25	MSIO174PB0
E37	HPC_HB21_L26_174N_B0	L26	MSIO174NB0
E38	GND		
E39	VCCIO_HPC_VADJ		
E40	GND		
F1	HPC_PG_M2C_J6_78P_B3	J6	MSIO78PB3/MMUART_0_RI/GPIO_21_B
F2	GND		
F3	GND		
F4	HPC_HA00_CC_AJ4_282P_B8	AJ4	MSIO282PB8/VCCC_SE1_CLKI
F5	HPC_HA00_CC_AJ3_282N_B8	AJ3	MSIO282NB8
F6	GND		
F7	HPC_HA04_AG3_287P_B8	AG3	MSIO287PB8
F8	HPC_HA04_AG4_287N_B8	AG4	MSIO287NB8
F9	GND		
F10	HPC_HA08_AD1_9P_B6	AD1	MSIO9PB6
F11	HPC_HA08_AC1_9N_B6	AC1	MSIO9NB6
F12	GND		
F13	HPC_HA12_AE4_4P_B6	AE4	MSIO4PB6
F14	HPC_HA12_AD4_4N_B6	AD4	MSIO4NB6
F15	GND		
F16	HPC_HA15_AA7_15P_B6	AA7	MSIO15PB6
F17	HPC_HA15_Y7_15N_B6	Y7	MSIO15NB6
F18	GND		
F19	HPC_HA19_AB10_11P_B6	AB10	MSIO11PB6
F20	HPC_HA19_AA10_11N_B6	AA10	MSIO11NB6
F21	GND		

Table 13 • **FMC HPC Connector (J30) Pinout *(continued)***

F22	HPC_HB02_V1_26P_B5	V1	MSIO26PB5/GPIO_27_A
F23	HPC_HB02_U1_26N_B5	U1	MSIO26NB5/GPIO_28_A
F24	GND		
F25	HPC_HB04_W3_25P_B5	W3	MSIO25PB5
F26	HPC_HB04_V3_25N_B5	V3	MSIO25NB5
F27	GND		
F28	HPC_HB08_Y6_18P_B5	Y6	MSIO18PB5
F29	HPC_HB08_Y5_18N_B5	Y5	MSIO18NB5
F30	GND		
F31	HPC_HB12_W8_27P_B5	W8	MSIO27PB5
F32	HPC_HB12_W9_27N_B5	W9	MSIO27NB5/USB_DATA7_B
F33	GND		
F34	HPC_HB16_Y12_21P_B5	Y12	MSIO21PB5
F35	HPC_HB16_Y11_21N_B5	Y11	MSIO21NB5
F36	GND		
F37	HPC_HB20_W12_28P_B5	W12	MSIO28PB5/USB_XCLK_B
F38	HPC_HB20_W11_28N_B5	W11	MSIO28NB5/USB_DIR_B
F39	GND		
F40	VCCIO_HPC_VADJ		
G1	GND		
G2	HPC_CLK1_M2C_AH28_267P_B14	AH28	MSIO267PB14/CCC_SW0_CLKI2
G3	HPC_CLK1_M2C_AG27_267N_B14	AG27	MSIO267NB14
G4	GND		
G5	GND		
G6	HPC_LA00_CC_U23_214P_B17	U23	MSIO214PB17/GB2/CCC_NW0_CLKI1
G7	HPC_LA00_CC_U24_214N_B17	U24	MSIO214NB17
G8	GND		
G9	HPC_LA03_N32_201P_B17	N32	MSIO201PB17
G10	HPC_LA03_N31_201N_B17	N31	MSIO201NB17
G11	GND		
G12	HPC_LA08_M25_181P_B18	M25	MSIO181PB18
G13	HPC_LA08_M24_181N_B18	M24	MSIO181NB18
G14	GND		
G15	HPC_LA12_M27_183P_B18	M27	MSIO183PB18
G16	HPC_LA12_M26_183N_B18	M26	MSIO183NB18
G17	GND		
G18	HPC_LA16_T28_209P_B17	T28	MSIO209PB17
G19	HPC_LA16_T27_209N_B17	T27	MSIO209NB17
G20	GND		

Table 13 • **FMC HPC Connector (J30) Pinout *(continued)***

G21	HPC_LA20_R31_205P_B17	R31	MSIO205PB17
G22	HPC_LA20_R30_205N_B17	R30	MSIO205NB17
G23	GND		
G24	HPC_LA22_R33_207P_B17	R33	MSIO207PB17
G25	HPC_LA22_R32_207N_B17	R32	MSIO207NB17
G26	GND		
G27	HPC_LA25_M34_197P_B17	M34	MSIO197PB17
G28	HPC_LA25_L34_197N_B17	L34	MSIO197NB17
G29	GND		
G30	HPC_LA29_J34_194P_B18	J34	MSIO194PB18
G31	HPC_LA29_J33_194N_B18	J33	MSIO194NB18
G32	GND		
G33	HPC_LA31_H34_196P_B18	H34	MSIO196PB18
G34	HPC_LA31_G34_196N_B18	G34	MSIO196NB18
G35	GND		
G36	HPC_LA33_E33_176P_B18	E33	MSIO176PB18
G37	HPC_LA33_D33_176N_B18	D33	MSIO176NB18
G38	GND		
G39	VCCIO_HPC_VADJ		
G40	GND		
H1	N36608719		
H2	HPC_PRSNT_M2CL_J7_78N_B3	J7	MSIO78NB3/MMUART_0_DCD/GPIO_22_B
H3	GND		
H4	HPC_CLK0_M2C_AJ6_281P_B8	AJ6	MSIO281PB8/GB15/VCCC_SE1_CLKI
H5	HPC_CLK0_M2C_AJ5_281N_B8	AJ5	MSIO281NB8
H6	GND		
H7	HPC_LA02_K31_179P_B18	K31	MSIO179PB18
H8	HPC_LA02_K30_179N_B18	K30	MSIO179NB18
H9	GND		
H10	HPC_LA04_L30_182P_B18	L30	MSIO182PB18
H11	HPC_LA04_L29_182N_B18	L29	MSIO182NB18
H12	GND		
H13	HPC_LA07_P23_192P_B18	P23	MSIO192PB18
H14	HPC_LA07_P24_192N_B18	P24	MSIO192NB18
H15	GND		
H16	HPC_LA11_T30_210P_B17	T30	MSIO210PB17
H17	HPC_LA11_T29_210N_B17	T29	MSIO210NB17
H18	GND		
H19	HPC_LA15_M30_188P_B18	M30	MSIO188PB18

Table 13 • **FMC HPC Connector (J30) Pinout *(continued)***

H20	HPC_LA15_M29_188N_B18	M29	MSIO188NB18
H21	GND		
H22	HPC_LA19_P31_199P_B17	P31	MSIO199PB17
H23	HPC_LA19_P30_199N_B17	P30	MSIO199NB17
H24	GND		
H25	HPC_LA21_P33_203P_B17	P33	MSIO203PB17
H26	HPC_LA21_N33_203N_B17	N33	MSIO203NB17
H27	GND		
H28	HPC_LA24_K33_187P_B18	K33	MSIO187PB18
H29	HPC_LA24_K32_187N_B18	K32	MSIO187NB18
H30	GND		
H31	HPC_LA28_H33_184P_B18	H33	MSIO184PB18
H32	HPC_LA28_H32_184N_B18	H32	MSIO184NB18
H33	GND		
H34	HPC_LA30_F34_185P_B18	F34	MSIO185PB18
H35	HPC_LA30_F33_185N_B18	F33	MSIO185NB18
H36	GND		
H37	HPC_LA32_D34_180P_B18	D34	MSIO180PB18
H38	HPC_LA32_C34_180N_B18	C34	MSIO180NB18
H39	GND		
H40	VCCIO_HPC_VADJ		
J1	GND		
J2	HPC_CLK3_M2C_P	AK12	MSIOD278PB10/SERDES_2_REFCLK1_P
J2	HPC_CLK3_M2C_P	AE17	MSIO275PB11/VCCC_SE0_CLKI
J3	HPC_CLK3_M2C_N	AJ12	MSIOD278NB10/SERDES_2_REFCLK1_N
J3	HPC_CLK3_M2C_N	AF17	MSIO275NB11
J4	GND		
J5	GND		
J6	HPC_HA03_AA4_12P_B6	AA4	MSIO12PB6
J7	HPC_HA03_AA5_12N_B6	AA5	MSIO12NB6
J8	GND		
J9	HPC_HA07_AC3_10P_B6	AC3	MSIO10PB6
J10	HPC_HA07_AB3_10N_B6	AB3	MSIO10NB6
J11	GND		
J12	HPC_HA11_AD3_5P_B6	AD3	MSIO5PB6
J13	HPC_HA11_AD2_5N_B6	AD2	MSIO5NB6
J14	GND		
J15	HPC_HA14_AG6_286P_B8	AG6	MSIO286PB8
J16	HPC_HA14_AG5_286N_B8	AG5	MSIO286NB8

Table 13 • **FMC HPC Connector (J30) Pinout *(continued)***

J17	GND		
J18	HPC_HA18_AC9_3P_B6	AC9	MSIO3PB6
J19	HPC_HA18_AC8_3N_B6	AC8	MSIO3NB6
J20	GND		
J21	HPC_HA22_AA8_13P_B6	AA8	MSIO13PB6
J22	HPC_HA22_AA9_13N_B6	AA9	MSIO13NB6
J23	GND		
J24	HPC_HB01_R1_32P_B5	R1	MSIO32PB5/USB_DATA4_B
J25	HPC_HB01_R2_32N_B5	R2	MSIO32NB5/USB_DATA5_B
J26	GND		
J27	HPC_HB07_Y4_24P_B5	Y4	MSIO24PB5
J28	HPC_HB07_W4_24N_B5	W4	MSIO24NB5
J29	GND		
J30	HPC_HB11_W6_23P_B5	W6	MSIO23PB5
J31	HPC_HB11_W7_23N_B5	W7	MSIO23NB5
J32	GND		
J33	HPC_HB15_V9_34P_B5	V9	MSIO34PB5
J34	HPC_HB15_V10_34N_B5	V10	MSIO34NB5
J35	GND		
J36	HPC_HB18_T2_31P_B5	T2	MSIO31PB5/USB_DATA2_B
J37	HPC_HB18_T3_31N_B5	T3	MSIO31NB5/USB_DATA3_B
J38	GND		
J39	VCCIO_HPC_VIO_B_M2C_FMC		
J40	GND		
K1	N36626276		
K2	GND		
K3	GND		
K4	HPC_CLK2_M2C_P	AJ20	MSIOD272PB12/SERDES_1_REFCLK1_P
K4	HPC_CLK2_M2C_P	AF18	MSIO274PB11/CCC_SW1_CLKI2
K5	HPC_CLK2_M2C_N	AK20	MSIOD272NB12/SERDES_1_REFCLK1_N
K5	HPC_CLK2_M2C_N	AG18	MSIO274NB11/CCC_SW1_CLKI3
K6	GND		
K7	HPC_HA02_AB2_16P_B6	AB2	MSIO16PB6
K8	HPC_HA02_AB1_16N_B6	AB1	MSIO16NB6
K9	GND		
K10	HPC_HA06_AC5_6P_B6	AC5	MSIO6PB6
K11	HPC_HA06_AC4_6N_B6	AC4	MSIO6NB6
K12	GND		
K13	HPC_HA10_AE6_288P_B8	AE6	MSIO288PB8

Table 13 • **FMC HPC Connector (J30) Pinout *(continued)***

K14	HPC_HA10_AF5_288N_B8	AF5	MSIO288NB8
K15	GND		
K16	HPC_HA17_CC_AJ29_268P_B14	AJ29	MSIO268PB14/GB3/CCC_SW0_CLKI3
K17	HPC_HA17_CC_AJ28_268N_B14	AJ28	MSIO268NB14
K18	GND		
K19	HPC_HA21_AA12_14P_B6	AA12	MSIO14PB6
K20	HPC_HA21_AA11_14N_B6	AA11	MSIO14NB6
K21	GND		
K22	HPC_HA23_AB5_7P_B6	AB5	MSIO7PB6
K23	HPC_HA23_AB6_7N_B6	AB6	MSIO7NB6
K24	GND		
K25	HPC_HB00_CC_F32_172P_B0	F32	MSIO172PB0/GB0/CCC_NW0_CLKI3
K26	HPC_HB00_CC_E32_172N_B0	E32	MSIO172NB0
K27	GND		
K28	HPC_HB06_CC_J29_170P_B0	J29	MSIO170PB0/CCC_NW1_CLKI3
K29	HPC_HB06_CC_J28_170N_B0	J28	MSIO170NB0
K30	GND		
K31	HPC_HB10_Y10_22P_B5	Y10	MSIO22PB5
K32	HPC_HB10_Y9_22N_B5	Y9	MSIO22NB5
K33	GND		
K34	HPC_HB14_V6_33P_B5	V6	MSIO33PB5/USB_DATA6_B
K35	HPC_HB14_U6_33N_B5	U6	MSIO33NB5
K36	GND		
K37	HPC_HB17_CC_U5_37P_B5	U5	MSIO37PB5/GB9/VCCC_SE0_CLKI
K38	HPC_HB17_CC_T5_37N_B5	T5	MSIO37NB5
K39	GND		
K40	VCCIO_HPC_VIO_B_M2C_FMC		

4.11.5.2 FMC LPC Connector (J60)

The SmartFusion2 MSIODs from banks 15 and 16 and the SERFDES3 lane 0 signals are routed to the FMC connector for the application to be developed.

The following table provides the FMC LPC header pinout details.

Table 14 • **FMC LPC Connector (J60) Pinout**

FMC Pin Number - J60	FMC Net Name	SmartFusion2 Pin Number	SmartFusion2 Pin Name
C1	GND		
C2	FMC_LPC_SERDES3_TXD0_P	AN8	SERDES_3_TXD0_P
C3	FMC_LPC_SERDES3_TXD0_N	AP8	SERDES_3_TXD0_N
C4	GND		
C5	GND		
C6	FMC_LPC_SERDES3_RXD0_P	AM9	SERDES_3_RXD0_P
C7	FMC_LPC_SERDES3_RXD0_N	AL9	SERDES_3_RXD0_N
C8	GND		
C9	GND		
C10	LPC_LA06_AF33_248P_B15	AF33	MSIOD248PB15
C11	LPC_LA06_AE33_248N_B15	AE33	MSIOD248NB15
C12	GND		
C13	GND		
C14	LPC_LA10_AE30_250P_B15	AE30	MSIOD250PB15
C15	LPC_LA10_AD30_250N_B15	AD30	MSIOD250NB15
C16	GND		
C17	GND		
C18	LPC_LA14_W23_227P_B16	W23	MSIOD227PB16
C19	LPC_LA14_W24_227N_B16	W24	MSIOD227NB16
C20	GND		
C21	GND		
C22	LPC_LA18_CC_AA32_228P_B16	AA32	MSIOD228PB16
C23	LPC_LA18_CC_Y32_228N_B16	Y32	MSIOD228NB16
C24	GND		
C25	GND		
C26	LPC_LA27_V29_223P_B16	V29	MSIOD223PB16
C27	LPC_LA27_V28_223N_B16	V28	MSIOD223NB16
C28	GND		
C29	GND		
C30	I2C1_SCL	T8	MSIO45NB4/I2C_1_SCL/GPIO_1_A/USB_DATA4_A
C31	I2C1_SDA	T9	MSIO45PB4/I2C_1_SDA/GPIO_0_A/USB_DATA3_A
C32	GND		
C33	GND		

Table 14 • **FMC LPC Connector (J60) Pinout *(continued)***

C34	GND		
C35	12P0V		
C36	GND		
C37	12P0V		
C38	GND		
C39	3P3V		
C40	GND		
D1	LPC_PGC2M_N12_71P_B3	N12	MSIO71PB3/MMUART_1_RTS/GPIO_11_B
D2	GND		
D3	GND		
D4	FMC_LPC_SERDES3_REFCLK0_P	AJ10	MSIOD279PB9/SERDES_3_REFCLK0_P
D5	FMC_LPC_SERDES3_REFCLK0_N	AK10	MSIOD279NB9/SERDES_3_REFCLK0_N
D6	GND		
D7	GND		
D8	LPC_LA01_CC_W34_219P_B16	W34	MSIOD219PB16/CCC_SW1_CLKI0
D9	LPC_LA01_CC_V34_219N_B16	V34	MSIOD219NB16
D10	GND		
D11	LPC_LA05_W29_226P_B16	W29	MSIOD226PB16
D12	LPC_LA05_W30_226N_B16	W30	MSIOD226NB16
D13	GND		
D14	LPC_LA09_Y28_231P_B16	Y28	MSIOD231PB16
D15	LPC_LA09_W28_231N_B16	W28	MSIOD231NB16
D16	GND		
D17	LPC_LA13_AC24_258P_B15	AC24	MSIOD258PB15
D18	LPC_LA13_AC23_258N_B15	AC23	MSIOD258NB15
D19	GND		
D20	LPC_LA17_CC_V23_220P_B16	V23	MSIOD220PB16/CCC_SW0_CLKI0
D21	LPC_LA17_CC_V24_220N_B16	V24	MSIOD220NB16
D22	GND		
D23	LPC_LA23_AG32_252P_B15	AG32	MSIOD252PB15
D24	LPC_LA23_AF32_252N_B15	AF32	MSIOD252NB15
D25	GND		
D26	LPC_LA26_V27_222P_B16	V27	MSIOD222PB16
D27	LPC_LA26_V26_222N_B16	V26	MSIOD222NB16
D28	GND		
D29	LPC_TCK		
D30	LPC_TDI		
D31	LPC_TDO		
D32	3P3V		

Table 14 • **FMC LPC Connector (J60) Pinout *(continued)***

D33	LPC_TMS		
D34	LPC_TRST_L		
D35	GND		
D36	3P3V		
D37	GND		
D38	3P3V		
D39	GND		
D40	3P3V		
G1	GND		
G2	LPC_CLK1_M2C_U34_217P_B16	U34	MSIOD217PB16/GB5/CCC_SW1_CLKI1
G3	LPC_CLK1_M2C_T34_217N_B16	T34	MSIOD217NB16
G4	GND		
G5	GND		
G6	LPC_LA00_CC_Y33_224P_B16	Y33	MSIOD224PB16
G7	LPC_LA00_CC_W33_224N_B16	W33	MSIOD224NB16
G8	GND		
G9	LPC_LA03_AC34_232P_B16	AC34	MSIOD232PB16
G10	LPC_LA03_AB34_232N_B16	AB34	MSIOD232NB16
G11	GND		
G12	LPC_LA08_AC32_233P_B16	AC32	MSIOD233PB16
G13	LPC_LA08_AC33_233N_B16	AC33	MSIOD233NB16
G14	GND		
G15	LPC_LA12_W26_229P_B16	W26	MSIOD229PB16
G16	LPC_LA12_W25_229N_B16	W25	MSIOD229NB16
G17	GND		
G18	LPC_LA16_Y23_234P_B16	Y23	MSIOD234PB16
G19	LPC_LA16_Y24_234N_B16	Y24	MSIOD234NB16
G20	GND		
G21	LPC_LA20_AF27_257P_B15	AF27	MSIOD257PB15
G22	LPC_LA20_AE27_257N_B15	AE27	MSIOD257NB15
G23	GND		
G24	LPC_LA22_AG34_244P_B15	AG34	MSIOD244PB15
G25	LPC_LA22_AF34_244N_B15	AF34	MSIOD244NB15
G26	GND		
G27	LPC_LA25_AH33_255P_B15	AH33	MSIOD255PB15
G28	LPC_LA25_AH34_255N_B15	AH34	MSIOD255NB15
G29	GND		
G30	LPC_LA29_AC27_245P_B15	AC27	MSIOD245PB15
G31	LPC_LA29_AB27_245N_B15	AB27	MSIOD245NB15
G32	GND		
G33	LPC_LA31_AB24_251P_B15	AB24	MSIOD251PB15

Table 14 • **FMC LPC Connector (J60) Pinout *(continued)***

G34	LPC_LA31_AB23_251N_B15	AB23	MSIOD251NB15
G35	GND		
G36	LPC_LA33_AD24_261P_B15	AD24	MSIOD261PB15
G37	LPC_LA33_AD25_261N_B15	AD25	MSIOD261NB15
G38	GND		
G39	VCCIO_LPC_VADJ		
G40	GND		
H1	N36478604		
H2	LPC_PRSNTM2CL_N11_71N_B3	N11	MSIO71NB3/MMUART_1_DTR/GPIO_12_B
H3	GND		
H4	LPC_CLK0_M2C_V32_218P_B16	V32	MSIOD218PB16/GB1/CCC_SW0_CLKI1
H5	LPC_CLK0_M2C_V33_218N_B16	V33	MSIOD218NB16
H6	GND		
H7	LPC_LA02_AA33_225P_B16	AA33	MSIOD225PB16
H8	LPC_LA02_AA34_225N_B16	AA34	MSIOD225NB16
H9	GND		
H10	LPC_LA04_AD33_239P_B16	AD33	MSIOD239PB16
H11	LPC_LA04_AD34_239N_B16	AD34	MSIOD239NB16
H12	GND		
H13	LPC_LA07_AE31_247P_B15	AE31	MSIOD247PB15
H14	LPC_LA07_AE32_247N_B15	AE32	MSIOD247NB15
H15	GND		
H16	LPC_LA11_AF30_254P_B15	AF30	MSIOD254PB15
H17	LPC_LA11_AG31_254N_B15	AG31	MSIOD254NB15
H18	GND		
H19	LPC_LA15_AF28_256P_B15	AF28	MSIOD256PB15
H20	LPC_LA15_AE28_256N_B15	AE28	MSIOD256NB15
H21	GND		
H22	LPC_LA19_AG30_260P_B15	AG30	MSIOD260PB15
H23	LPC_LA19_AF29_260N_B15	AF29	MSIOD260NB15
H24	GND		
H25	LPC_LA21_W31_221P_B16	W31	MSIOD221PB16
H26	LPC_LA21_V31_221N_B16	V31	MSIOD221NB16
H27	GND		
H28	LPC_LA24_AD28_249P_B15	AD28	MSIOD249PB15
H29	LPC_LA24_AD29_249N_B15	AD29	MSIOD249NB15
H30	GND		
H31	LPC_LA28_AB25_246P_B15	AB25	MSIOD246PB15
H32	LPC_LA28_AB26_246N_B15	AB26	MSIOD246NB15
H33	GND		

Table 14 • **FMC LPC Connector (J60) Pinout *(continued)***

H34	LPC_LA30_AC25_253P_B15	AC25	MSIOD253PB15
H35	LPC_LA30_AC26_253N_B15	AC26	MSIOD253NB15
H36	GND		
H37	LPC_LA32_AE26_259P_B15	AE26	MSIOD259PB15
H38	LPC_LA32_AD26_259N_B15	AD26	MSIOD259NB15
H39	GND		
H40	VCCIO_LPC_VADJ		

5 Pin List

The following table lists all the package pins in the SmartFusion2 M2S150TS-1FCG1152 device.

Table 15 • **Pin List**

Package Pin	Device Pin Name
A2	DDRIO82PB2/MDDR_ADDR14
A3	DDRIO86NB2/MDDR_ADDR7
A4	VSS
A5	DDRIO88NB2/MDDR_ADDR4
A6	DDRIO87PB2/MDDR_ADDR5
A7	VSS
A8	DDRIO97PB2/MDDR_DQ28
A9	VSS
A10	DDRIO101PB2/MDDR_DQ24
A11	VSS
A12	DDRIO112PB2/MDDR_DQ10
A13	VSS
A14	DDRIO115PB2/MDDR_DQ5
A15	VSS
A16	DDRIO119PB2/MDDR_DQ0
A17	VSS
A18	DDRIO126NB1/FDDR_ADDR15
A19	DDRIO130PB1/FDDR_ODT
A20	VSS
A21	DDRIO140PB1/FDDR_DQ30
A22	VSS
A23	DDRIO141PB1/FDDR_DQ28
A24	VSS
A25	DDRIO147PB1/FDDR_DQ21
A26	VSS
A27	DDRIO148PB1/FDDR_DM_RDQS2
A28	VSS
A29	DDRIO162PB1/FDDR_DQ2
A30	VSS
A31	DDRIO164PB1/FDDR_DQ_ECC1
A32	VSS
A33	DDRIO165PB1/FDDR_DQ_ECC3
AA1	VSS
AA2	MSIO17NB6

Table 15 • **Pin List**

AA3	MSIO17PB6
AA4	MSIO12PB6
AA5	MSIO12NB6
AA6	VDDI6
AA7	MSIO15PB6
AA8	MSIO13PB6
AA9	MSIO13NB6
AA10	MSIO11NB6
AA11	MSIO14NB6
AA12	MSIO14PB6
AA13	VDDI6
AA14	VSS
AA15	VPP
AA16	VSS
AA17	VPP
AA18	VSS
AA19	VPP
AA20	VSS
AA21	CCC_SW1_PLL_VSSA
AA22	CCC_SW0_PLL_VSSA
AA23	CCC_SW0_PLL_VDDA
AA24	VSS
AA25	MSIOD241PB16
AA26	VDDI16
AA27	MSIOD238PB16
AA28	MSIOD238NB16
AA29	MSIOD237PB16
AA30	MSIOD237NB16
AA31	VSS
AA32	MSIOD228PB16
AA33	MSIOD225PB16
AA34	MSIOD225NB16
AB1	MSIO16NB6
AB2	MSIO16PB6
AB3	MSIO10NB6
AB4	VSS
AB5	MSIO7PB6
AB6	MSIO7NB6
AB7	MSIO8NB6
AB8	MSIO8PB6

Table 15 • **Pin List**

AB9	VDDI6
AB10	MSIO11PB6
AB11	CCC_SE1_PLL_VDDA
AB12	CCC_SE0_PLL_VDDA
AB13	CCC_SE0_PLL_VSSA
AB14	SERDES_3_VDD
AB15	VSS
AB16	SERDES_2_VDD
AB17	VSS
AB18	SERDES_1_VDD
AB19	VSS
AB20	SERDES_0_VDD
AB21	VSS
AB22	VDDI15
AB23	MSIOD251NB15
AB24	MSIOD251PB15
AB25	MSIOD246PB15
AB26	MSIOD246NB15
AB27	MSIOD245NB15
AB28	VSS
AB29	MSIOD242PB16
AB30	MSIOD242NB16
AB31	MSIOD236PB16
AB32	MSIOD236NB16
AB33	VDDI16
AB34	MSIOD232NB16
AC1	MSIO9NB6
AC2	VDDI6
AC3	MSIO10PB6
AC4	MSIO6NB6
AC5	MSIO6PB6
AC6	FLASH_GOLDEN_N
AC7	VSS
AC8	MSIO3NB6
AC9	MSIO3PB6
AC10	SC_SPI_SS
AC11	SC_SPI_SDO
AC12	CCC_SE1_PLL_VSSA
AC13	SERDES_3_VDD
AC14	VSS

Table 15 • **Pin List**

AC15	SERDES_2_VDD
AC16	VSS
AC17	VDD
AC18	VSS
AC19	SERDES_1_VDD
AC20	VSS
AC21	SERDES_0_VDD
AC22	VSS
AC23	MSIOD258NB15
AC24	MSIOD258PB15
AC25	MSIOD253PB15
AC26	MSIOD253NB15
AC27	MSIOD245PB15
AC28	MSIOD243PB16
AC29	MSIOD243NB16
AC30	VDDI16
AC31	MSIOD240NB16
AC32	MSIOD233PB16
AC33	MSIOD233NB16
AC34	MSIOD232PB16
AD1	MSIO9PB6
AD2	MSIO5NB6
AD3	MSIO5PB6
AD4	MSIO4NB6
AD5	VDDI6
AD6	VDDI8
AD7	MSIO289NB8
AD8	SC_SPI_SDI
AD9	SC_SPI_CLK
AD10	VSS
AD11	VSS
AD12	SERDES_3_L23_VDDAIO
AD13	VSS
AD14	SERDES_2_L23_VDDAIO
AD15	VSS
AD16	SERDES_2_L01_VDDAIO
AD17	VSS
AD18	SERDES_1_L23_VDDAIO
AD19	VSS
AD20	SERDES_1_L01_VDDAIO

Table 15 • **Pin List**

AD21	VSS
AD22	SERDES_0_L01_VDDAIO
AD23	VSS
AD24	MSIOD261PB15
AD25	MSIOD261NB15
AD26	MSIOD259NB15
AD27	VDDI15
AD28	MSIOD249PB15
AD29	MSIOD249NB15
AD30	MSIOD250NB15
AD31	MSIOD240PB16
AD32	VSS
AD33	MSIOD239PB16
AD34	MSIOD239NB16
AE1	JTAG_TDI/M3_TDI
AE2	JTAG_TMS/M3_TMS/M3_SWDIO
AE3	VSS
AE4	MSIO4PB6
AE5	DEVRST_N
AE6	MSIO288PB8
AE7	MSIO289PB8
AE8	VSS
AE9	VSS
AE10	VSS
AE11	SERDES_3_L23_VDDAIO
AE12	VSS
AE13	SERDES_3_L01_VDDAIO
AE14	VSS
AE15	SERDES_2_L01_VDDAIO
AE16	VSS
AE17	MSIO275PB11/CCC_SE0_CLKI2
AE18	VSS
AE19	SERDES_1_L23_VDDAIO
AE20	VSS
AE21	SERDES_0_L23_VDDAIO
AE22	VSS
AE23	SERDES_0_L01_VDDAIO
AE24	VSS
AE25	VSS
AE26	MSIOD259PB15

Table 15 • **Pin List**

AE27	MSIOD257NB15
AE28	MSIOD256NB15
AE29	VSS
AE30	MSIOD250PB15
AE31	MSIOD247PB15
AE32	MSIOD247NB15
AE33	MSIOD248NB15
AE34	VDDI15
AF1	VDDI7
AF2	JTAG_TDO/M3_TDO/M3_SWO
AF3	JTAG_TCK/M3_TCK
AF4	VSS
AF5	MSIO288NB8
AF6	VSS
AF7	MSIO284NB8
AF8	VSS
AF9	SERDES_3_PLL_VSSA
AF10	SERDES_3_PLL_VDDA
AF11	VSS
AF12	SERDES_3_L01_VDDAIO
AF13	VSS
AF14	SERDES_2_L23_VDDAIO
AF15	VSS
AF16	MSIO276PB11/GB11/CCC_SE0_CLKI3
AF17	MSIO275NB11
AF18	MSIO274PB11/GB7/CCC_SW1_CLKI2
AF19	VSS
AF20	SERDES_1_L01_VDDAIO
AF21	VSS
AF22	SERDES_0_L23_VDDAIO
AF23	VSS
AF24	SERDES_0_L01_VDDAPLL
AF25	SERDES_0_L01_REFRET
AF26	VSS
AF27	MSIOD257PB15
AF28	MSIOD256PB15
AF29	MSIOD260NB15
AF30	MSIOD254PB15
AF31	VDDI15
AF32	MSIOD252NB15

Table 15 • **Pin List**

AF33	MSIOD248PB15
AF34	MSIOD244NB15
AG1	JTAG_TRSTB/M3_TRSTB
AG2	JTAGSEL
AG3	MSIO287PB8
AG4	MSIO287NB8
AG5	MSIO286NB8
AG6	MSIO286PB8
AG7	MSIO284PB8
AG8	VSS
AG9	SERDES_3_L23_REXT
AG10	SERDES_3_L23_VDDAPLL
AG11	SERDES_3_L01_VDDAPLL
AG12	VSS
AG13	SERDES_2_PLL_VSSA
AG14	VSS
AG15	SERDES_2_L23_VDDAPLL
AG16	MSIO276NB11
AG17	VDDI11
AG18	MSIO274NB11/CCC_SW1_CLKI3
AG19	SERDES_1_L23_VDDAPLL
AG20	VSS
AG21	SERDES_1_L01_VDDAPLL
AG22	VSS
AG23	SERDES_0_L23_VDDAPLL
AG24	SERDES_0_L23_REFRET
AG25	SERDES_0_L01_REXT
AG26	VSS
AG27	MSIO267NB14
AG28	MSIO263NB14
AG29	MSIO263PB14
AG30	MSIOD260PB15
AG31	MSIOD254NB15
AG32	MSIOD252PB15
AG33	VSS
AG34	MSIOD244PB15
AH1	XTLOSC_AUX_EXTAL
AH2	VSS
AH3	MSIO285NB8
AH4	VDDI8

Table 15 • **Pin List**

AH5	MSIO283NB8
AH6	MSIO283PB8
AH7	VDDI8
AH8	VSS
AH9	SERDES_3_L23_REFRET
AH10	SERDES_3_L01_REXT
AH11	SERDES_3_L01_REFRET
AH12	SERDES_2_PLL_VDDA
AH13	SERDES_2_L23_REXT
AH14	SERDES_2_L23_REFRET
AH15	SERDES_2_L01_VDDAPLL
AH16	SERDES_2_L01_REXT
AH17	MSIO273PB11/PROBE_A
AH18	SERDES_1_PLL_VSSA
AH19	SERDES_1_L23_REXT
AH20	SERDES_1_L23_REFRET
AH21	SERDES_1_L01_REFRET
AH22	SERDES_1_L01_REXT
AH23	SERDES_0_PLL_VSSA
AH24	SERDES_0_PLL_VDDA
AH25	SERDES_0_L23_REXT
AH26	VSS
AH27	VDDI14
AH28	MSIO267PB14/CCC_SW0_CLKI2
AH29	MSIO266PB14
AH30	MSIO265NB14
AH31	MSIO265PB14
AH32	MSIO264PB14
AH33	MSIOD255PB15
AH34	MSIOD255NB15
AJ1	XTLOSC_AUX_XTAL
AJ2	MSIO285PB8
AJ3	MSIO282NB8
AJ4	MSIO282PB8/CCC_SE1_CLKI3
AJ5	MSIO281NB8
AJ6	MSIO281PB8/GB15/CCC_SE1_CLKI2
AJ7	VSS
AJ8	MSIOD280PB9/SERDES_3_REFCLK1_P
AJ9	VDDI9
AJ10	MSIOD279PB9/SERDES_3_REFCLK0_P

Table 15 • **Pin List**

AJ11	VSS
AJ12	MSIOD278NB10/SERDES_2_REFCLK1_N
AJ13	VDDI10
AJ14	MSIOD277NB10/SERDES_2_REFCLK0_N
AJ15	VSS
AJ16	SERDES_2_L01_REFRET
AJ17	MSIO273NB11/PROBE_B
AJ18	SERDES_1_PLL_VDDA
AJ19	VSS
AJ20	MSIOD272PB12/SERDES_1_REFCLK1_P
AJ21	VDDI12
AJ22	MSIOD271PB12/SERDES_1_REFCLK0_P
AJ23	VSS
AJ24	MSIOD270PB13/SERDES_0_REFCLK1_P
AJ25	VDDI13
AJ26	MSIOD269PB13/SERDES_0_REFCLK0_P
AJ27	VSS
AJ28	MSIO268NB14
AJ29	MSIO268PB14/GB3/CCC_SW0_CLKI3
AJ30	MSIO266NB14
AJ31	VDDI14
AJ32	MSIO264NB14
AJ33	MSIO262NB14
AJ34	MSIO262PB14
AK1	XTLOSC_MAIN_EXTAL
AK2	VSS
AK3	VSS
AK4	VSS
AK5	VSS
AK6	VSS
AK7	VSS
AK8	MSIOD280NB9/SERDES_3_REFCLK1_N
AK9	VSS
AK10	MSIOD279NB9/SERDES_3_REFCLK0_N
AK11	VSS
AK12	MSIOD278PB10/SERDES_2_REFCLK1_P
AK13	VSS
AK14	MSIOD277PB10/SERDES_2_REFCLK0_P
AK15	VSS
AK16	VSS

Table 15 • **Pin List**

AK17	VSS
AK18	VSS
AK19	VSS
AK20	MSIOD272NB12/SERDES_1_REFCLK1_N
AK21	VSS
AK22	MSIOD271NB12/SERDES_1_REFCLK0_N
AK23	VSS
AK24	MSIOD270NB13/SERDES_0_REFCLK1_N
AK25	VSS
AK26	MSIOD269NB13/SERDES_0_REFCLK0_N
AK27	VSS
AK28	VSS
AK29	VSS
AK30	VSS
AK31	VSS
AK32	VSS
AK33	VSS
AK34	VSS
AL1	XTLOSC_MAIN_XTAL
AL2	VSS
AL3	SERDES_3_RXD3_N
AL4	VSS
AL5	SERDES_3_RXD2_N
AL6	VSS
AL7	SERDES_3_RXD1_N
AL8	VSS
AL9	SERDES_3_RXD0_N
AL10	VSS
AL11	SERDES_2_RXD3_N
AL12	VSS
AL13	SERDES_2_RXD2_N
AL14	VSS
AL15	SERDES_2_RXD1_N
AL16	VSS
AL17	SERDES_2_RXD0_N
AL18	VSS
AL19	SERDES_1_RXD3_P
AL20	VSS
AL21	SERDES_1_RXD2_P
AL22	VSS

Table 15 • **Pin List**

AL23	SERDES_1_RXD1_P
AL24	VSS
AL25	SERDES_1_RXD0_P
AL26	VSS
AL27	SERDES_0_RXD3_P
AL28	VSS
AL29	SERDES_0_RXD2_P
AL30	VSS
AL31	SERDES_0_RXD1_P
AL32	VSS
AL33	SERDES_0_RXD0_P
AL34	VSS
AM1	VSS
AM2	VSS
AM3	SERDES_3_RXD3_P
AM4	VSS
AM5	SERDES_3_RXD2_P
AM6	VSS
AM7	SERDES_3_RXD1_P
AM8	VSS
AM9	SERDES_3_RXD0_P
AM10	VSS
AM11	SERDES_2_RXD3_P
AM12	VSS
AM13	SERDES_2_RXD2_P
AM14	VSS
AM15	SERDES_2_RXD1_P
AM16	VSS
AM17	SERDES_2_RXD0_P
AM18	VSS
AM19	SERDES_1_RXD3_N
AM20	VSS
AM21	SERDES_1_RXD2_N
AM22	VSS
AM23	SERDES_1_RXD1_N
AM24	VSS
AM25	SERDES_1_RXD0_N
AM26	VSS
AM27	SERDES_0_RXD3_N
AM28	VSS

Table 15 • **Pin List**

AM29	SERDES_0_RXD2_N
AM30	VSS
AM31	SERDES_0_RXD1_N
AM32	VSS
AM33	SERDES_0_RXD0_N
AM34	VSS
AN1	VSS
AN2	SERDES_3_TXD3_P
AN3	VSS
AN4	SERDES_3_TXD2_P
AN5	VSS
AN6	SERDES_3_TXD1_P
AN7	VSS
AN8	SERDES_3_TXD0_P
AN9	VSS
AN10	SERDES_2_TXD3_P
AN11	VSS
AN12	SERDES_2_TXD2_P
AN13	VSS
AN14	SERDES_2_TXD1_P
AN15	VSS
AN16	SERDES_2_TXD0_P
AN17	VSS
AN18	SERDES_1_TXD3_N
AN19	VSS
AN20	SERDES_1_TXD2_N
AN21	VSS
AN22	SERDES_1_TXD1_N
AN23	VSS
AN24	SERDES_1_TXD0_N
AN25	VSS
AN26	SERDES_0_TXD3_N
AN27	VSS
AN28	SERDES_0_TXD2_N
AN29	VSS
AN30	SERDES_0_TXD1_N
AN31	VSS
AN32	SERDES_0_TXD0_N
AN33	VSS
AN34	VSS

Table 15 • **Pin List**

AP2	SERDES_3_TXD3_N
AP3	VSS
AP4	SERDES_3_TXD2_N
AP5	VSS
AP6	SERDES_3_TXD1_N
AP7	VSS
AP8	SERDES_3_TXD0_N
AP9	VSS
AP10	SERDES_2_TXD3_N
AP11	VSS
AP12	SERDES_2_TXD2_N
AP13	VSS
AP14	SERDES_2_TXD1_N
AP15	VSS
AP16	SERDES_2_TXD0_N
AP17	VSS
AP18	SERDES_1_TXD3_P
AP19	VSS
AP20	SERDES_1_TXD2_P
AP21	VSS
AP22	SERDES_1_TXD1_P
AP23	VSS
AP24	SERDES_1_TXD0_P
AP25	VSS
AP26	SERDES_0_TXD3_P
AP27	VSS
AP28	SERDES_0_TXD2_P
AP29	VSS
AP30	SERDES_0_TXD1_P
AP31	VSS
AP32	SERDES_0_TXD0_P
AP33	VSS
B1	VSS
B2	DDRIO82NB2/MDDR_ADDR15
B3	DDRIO86PB2/MDDR_ODT
B4	DDRIO88PB2/MDDR_ADDR3
B5	DDRIO87NB2/MDDR_ADDR6
B6	DDRIO89PB2/MDDR_ADDR1
B7	VDDI2
B8	DDRIO97NB2/MDDR_DQ29

Table 15 • **Pin List**

B9	VDDI2
B10	DDRIO101NB2/MDDR_DQ25
B11	VDDI2
B12	DDRIO112NB2/MDDR_DQ11
B13	VDDI2
B14	DDRIO115NB2/MDDR_DQ6
B15	VDDI2
B16	DDRIO119NB2/MDDR_DQ1
B17	VDDI2
B18	DDRIO126PB1/FDDR_ADDR14
B19	DDRIO130NB1/FDDR_ADDR7
B20	VDDI1
B21	DDRIO140NB1/FDDR_DQ31
B22	VDDI1
B23	DDRIO141NB1/FDDR_DQ29
B24	VDDI1
B25	DDRIO147NB1/FDDR_DQ22
B26	VDDI1
B27	DDRIO148NB1/FDDR_DQ20
B28	VDDI1
B29	DDRIO162NB1/FDDR_DQ3
B30	VDDI1
B31	DDRIO164NB1/FDDR_DQ_ECC0
B32	VDDI1
B33	DDRIO165NB1/FDDR_DQ_ECC2
B34	VSS
C1	DDRIO84NB2/MDDR_ADDR11
C2	DDRIO84PB2/MDDR_ADDR10
C3	VDDI2
C4	DDRIO83NB2/MDDR_ADDR13
C5	DDRIO92PB2/MDDR_CLK
C6	DDRIO89NB2/MDDR_ADDR2
C7	DDRIO96PB2/MDDR_DQ30
C8	DDRIO99NB2/MDDR_DQS3_N
C9	DDRIO99PB2/MDDR_DQS3
C10	DDRIO100PB2/MDDR_DQ26
C11	DDRIO111NB2/MDDR_DQS1_N
C12	DDRIO111PB2/MDDR_DQS1
C13	DDRIO113PB2/MDDR_DQ8
C14	DDRIO117NB2/MDDR_DQS0_N

Table 15 • **Pin List**

C15	DDRIO117PB2/MDDR_DQS0
C16	DDRIO118PB2/MDDR_DQ2
C17	DDRIO121PB2/MDDR_DQ_ECC3
C18	VDDI1
C19	DDRIO131NB1/FDDR_ADDR6
C20	DDRIO134NB1/FDDR_ADDR0
C21	DDRIO143NB1/FDDR_DQS3_N
C22	DDRIO143PB1/FDDR_DQS3
C23	DDRIO144NB1/FDDR_DQ27
C24	DDRIO144PB1/FDDR_DQ26
C25	DDRIO146PB1/FDDR_DQ23
C26	DDRIO149NB1/FDDR_DQS2_N
C27	DDRIO151NB1/FDDR_DQ17
C28	DDRIO151PB1/FDDR_DQ16
C29	DDRIO161NB1/FDDR_DQS0_N
C30	DDRIO161PB1/FDDR_DQS0
C31	DDRIO167NB1/FDDR_DQS_ECC_N
C32	DDRIO167PB1/FDDR_DQS_ECC
C33	FDDR_IMP_CALIB
C34	MSIO180NB18
D1	MSIO62NB3/USB_NXT_D
D2	DDRIO85NB2/MDDR_ADDR9
D3	DDRIO85PB2/MDDR_ADDR8
D4	DDRIO83PB2/MDDR_ADDR12
D5	DDRIO92NB2/MDDR_CLK_N
D6	VSS
D7	DDRIO96NB2/MDDR_DQ31
D8	VSS
D9	DDRIO100NB2/MDDR_DQ27
D10	VSS
D11	DDRIO109PB2/MDDR_DQ12
D12	VSS
D13	DDRIO113NB2/MDDR_DQ9
D14	VSS
D15	DDRIO118NB2/MDDR_DQ3
D16	VSS
D17	DDRIO121NB2/MDDR_DQ_ECC2
D18	DDRIO127PB1/FDDR_ADDR12
D19	DDRIO131PB1/FDDR_ADDR5
D20	DDRIO134PB1/FDDR_BA2

Table 15 • **Pin List**

D21	VSS
D22	DDRIO145PB1/FDDR_DQ24
D23	VSS
D24	DDRIO146NB1/FDDR_TMATCH_1_OUT
D25	VSS
D26	DDRIO149PB1/FDDR_DQS2
D27	VSS
D28	DDRIO159PB1/FDDR_DQ5
D29	VSS
D30	DDRIO163NB1/FDDR_DQ1
D31	VSS
D32	DDRIO169NB1
D33	MSIO176NB18
D34	MSIO180PB18
E1	MSIO62PB3/USB_STP_D
E2	MSIO74PB3/USB_XCLK_C
E3	MSIO74NB3/MMUART_1_TXD/GPIO_24_B/USB_DATA2_C
E4	VSS
E5	DDRIO91PB2/MDDR_BA0
E6	DDRIO90NB2/MDDR_ADDR0
E7	DDRIO95PB2/MDDR_RAS_N
E8	VDDI2
E9	DDRIO98PB2/MDDR_TMATCH_1_IN
E10	VDDI2
E11	DDRIO109NB2/MDDR_DQ13
E12	VDDI2
E13	DDRIO114NB2/MDDR_TMATCH_0_OUT
E14	VDDI2
E15	DDRIO116NB2/MDDR_DQ4
E16	VDDI2
E17	DDRIO123NB2/MDDR_DQS_ECC_N
E18	DDRIO127NB1/FDDR_ADDR13
E19	VSS
E20	DDRIO136PB1/FDDR_CLK
E21	VDDI1
E22	DDRIO145NB1/FDDR_DQ25
E23	VDDI1
E24	DDRIO142PB1/FDDR_TMATCH_1_IN
E25	VDDI1

Table 15 • **Pin List**

E26	DDRIO150NB1/FDDR_DQ19
E27	VDDI1
E28	DDRIO159NB1/FDDR_DQ6
E29	VDDI1
E30	DDRIO163PB1/FDDR_DQ0
E31	DDRIO169PB1/FDDR_TMATCH_ECC_OUT
E32	MSIO172NB0
E33	MSIO176PB18
E34	VDDI18
F1	VDDI3
F2	MSIO73PB3/MMUART_1_RI/GPIO_15_B
F3	MSIO73NB3/MMUART_1_DCD/GPIO_16_B
F4	MSIO79PB3
F5	DDRIO91NB2/MDDR_BA1
F6	DDRIO90PB2/MDDR_BA2
F7	DDRIO95NB2/MDDR_WE_N
F8	DDRIO98NB2/MDDR_DM_RDQS3
F9	DDRIO102NB2/MDDR_TMATCH_1_OUT
F10	DDRIO108NB2/MDDR_DQ15
F11	DDRIO108PB2/MDDR_DQ14
F12	DDRIO110NB2/MDDR_DM_RDQS1
F13	DDRIO110PB2/MDDR_TMATCH_0_IN
F14	DDRIO114PB2/MDDR_DQ7
F15	DDRIO116PB2/MDDR_DM_RDQS0
F16	DDRIO120PB2/MDDR_DQ_ECC1/GB12/CCC_NE1_CLKI2
F17	DDRIO123PB2/MDDR_DQS_ECC
F18	DDRIO128NB1/FDDR_ADDR11
F19	DDRIO132NB1/FDDR_ADDR4
F20	DDRIO136NB1/FDDR_CLK_N
F21	DDRIO137NB1/FDDR_CAS_N
F22	DDRIO137PB1/FDDR_RESET_N
F23	DDRIO155PB1/FDDR_DQS1
F24	DDRIO142NB1/FDDR_DM_RDQS3
F25	DDRIO152PB1/FDDR_DQ14
F26	DDRIO150PB1/FDDR_DQ18
F27	DDRIO158NB1/FDDR_TMATCH_0_OUT
F28	DDRIO158PB1/FDDR_DQ7
F29	DDRIO160NB1/FDDR_DQ4
F30	DDRIO166NB1/FDDR_DM_RDQS_ECC

Table 15 • **Pin List**

F31	DDRIO166PB1/FDDR_TMATCH_ECC_IN
F32	MSIO172PB0/GB0/CCC_NW0_CLKI3
F33	MSIO185NB18
F34	MSIO185PB18
G1	MSIO61NB3/USB_DIR_D
G2	MSIO69PB3/GPIO_7_B
G3	MSIO69NB3/GPIO_8_B
G4	VDDI3
G5	MSIO79NB3/MMUART_0_TXD/GPIO_27_B/USB_DIR_C
G6	VDDI2
G7	DDRIO93NB2/MDDR_CAS_N
G8	DDRIO93PB2/MDDR_RESET_N
G9	VSS
G10	DDRIO102PB2/MDDR_DQ23
G11	VSS
G12	DDRIO105PB2/MDDR_DQS2
G13	VSS
G14	DDRIO107PB2/MDDR_DQ16
G15	VSS
G16	DDRIO120NB2/MDDR_DQ_ECC0/CCC_NE1_CLKI3
G17	VSS
G18	DDRIO129NB1/FDDR_ADDR9
G19	DDRIO128PB1/FDDR_ADDR10
G20	DDRIO132PB1/FDDR_ADDR3
G21	DDRIO135PB1/FDDR_BA0
G22	VSS
G23	DDRIO155NB1/FDDR_DQS1_N
G24	VSS
G25	DDRIO152NB1/FDDR_DQ15
G26	VSS
G27	DDRIO154PB1/FDDR_TMATCH_0_IN
G28	VSS
G29	DDRIO160PB1/FDDR_DM_RDQS0
G30	MSIO171PB0/GB4/CCC_NW1_CLKI2
G31	MSIO175NB0
G32	VDDI0
G33	VSS
G34	MSIO196NB18
H1	MSIO61PB3/USB_XCLK_D
H2	VSS

Table 15 • **Pin List**

H3	MSIO70PB3/GPIO_9_B
H4	MSIO70NB3/GPIO_10_B
H5	MSIO77PB3/MMUART_0_CTS/GPIO_19_B/USB_DATA7_C
H6	MSIO77NB3/MMUART_0_DSR/GPIO_20_B
H7	MSIO80PB3/MMUART_0_RXD/GPIO_28_B/USB_STP_C
H8	DDRIO94PB2/MDDR_CKE
H9	VDDI2
H10	DDRIO103PB2/MDDR_DQ21
H11	VDDI2
H12	DDRIO105NB2/MDDR_DQS2_N
H13	VDDI2
H14	DDRIO107NB2/MDDR_DQ17
H15	VDDI2
H16	DDRIO122PB2/MDDR_TMATCH_ECC_IN
H17	VDDI2
H18	DDRIO129PB1/FDDR_ADDR8
H19	VSS
H20	DDRIO135NB1/FDDR_BA1
H21	DDRIO138NB1/FDDR_CS_N
H22	VDDI1
H23	DDRIO157NB1/FDDR_DQ9
H24	VDDI1
H25	DDRIO156NB1/FDDR_DQ11
H26	VDDI1
H27	DDRIO154NB1/FDDR_DM_RDQS1
H28	VDDI1
H29	MSIO171NB0
H30	VSS
H31	MSIO175PB0
H32	MSIO184NB18
H33	MSIO184PB18
H34	MSIO196PB18
J1	MSIO56PB4/SPI_0_SS3/GPIO_10_A/USB_DATA7_A
J2	MSIO56NB4/SPI_1_SS1/GPIO_14_A
J3	MSIO65PB3/USB_DATA4_D
J4	MSIO65NB3/USB_DATA5_D
J5	VSS
J6	MSIO78PB3/MMUART_0_RI/GPIO_21_B
J7	MSIO78NB3/MMUART_0_DCD/GPIO_22_B

Table 15 • **Pin List**

J8	MSIO80NB3/MMUART_0_CLK/GPIO_29_B/USB_NXT_C
J9	DDRIO94NB2/MDDR_CS_N
J10	DDRIO103NB2/MDDR_DQ22
J11	DDRIO104NB2/MDDR_DQ20
J12	DDRIO104PB2/MDDR_DM_RDQS2
J13	DDRIO106NB2/MDDR_DQ19
J14	DDRIO106PB2/MDDR_DQ18
J15	DDRIO122NB2/MDDR_DM_RDQS_ECC
J16	DDRIO125PB2/MDDR_TMATCH_ECC_OUT
J17	DDRIO124NB2/GB8/CCC_NE0_CLKI3
J18	DDRIO124PB2/CCC_NE0_CLKI2
J19	DDRIO133NB1/FDDR_ADDR2
J20	DDRIO139PB1/FDDR_RAS_N
J21	DDRIO138PB1/FDDR_CKE
J22	DDRIO153NB1/FDDR_DQ13
J23	DDRIO153PB1/FDDR_DQ12
J24	DDRIO157PB1/FDDR_DQ8
J25	DDRIO156PB1/FDDR_DQ10
J26	DDRIO168NB1
J27	DDRIO168PB1
J28	MSIO170NB0
J29	MSIO170PB0/CCC_NW1_CLKI3
J30	MSIO177NB18
J31	MSIO177PB18
J32	VDDI18
J33	MSIO194NB18
J34	MSIO194PB18
K1	MSIO47PB4/SPI_0_SDO/GPIO_6_A/USB_STP_A
K2	MSIO47NB4/SPI_0_SS0/GPIO_7_A/USB_NXT_A
K3	VDDI4
K4	MSIO66PB3/USB_DATA6_D
K5	MSIO66NB3/USB_DATA7_D/GPIO_23_B
K6	MSIO72PB3/GPIO_13_B/MMUART_1_CTS
K7	MSIO72NB3/MMUART_1_DSR/GPIO_14_B
K8	VSS
K9	MSIO81PB3/I2C_0_SDA/GPIO_30_B/USB_DATA0_C
K10	MSIO81NB3/I2C_0_SCL/GPIO_31_B/USB_DATA1_C
K11	MSS_MDDR_PLL_VSSA
K12	MSS_MDDR_PLL_VDDA
K13	VSS

Table 15 • **Pin List**

K14	VDDI2
K15	MDDR_IMP_CALIB
K16	VSS
K17	DDRIO125NB2
K18	VSS
K19	DDRIO133PB1/FDDR_ADDR1
K20	DDRIO139NB1/FDDR_WE_N
K21	VSS
K22	VDDI1
K23	FDDR_PLL_VDDA
K24	FDDR_PLL_VSSA
K25	VSS
K26	VDDI0
K27	MSIO173PB0/CCC_NW0_CLKI2
K28	MSIO173NB0
K29	VDDI18
K30	MSIO179NB18
K31	MSIO179PB18
K32	MSIO187NB18
K33	MSIO187PB18
K34	VSS
L1	VSS
L2	MSIO51PB4/SPI_1_SDO/GPIO_12_A
L3	MSIO51NB4/SPI_1_SS0/GPIO_13_A
L4	MSIO59PB4/GPIO_31_A
L5	MSIO59NB4/GPIO_0_B
L6	VDDI3
L7	MSIO68PB3/GPIO_5_B
L8	MSIO68NB3/GPIO_6_B
L9	MSIO75PB3/MMUART_1_CLK/GPIO_25_B/USB_DATA4_C
L10	MSIO75NB3/MMUART_1_RXD/GPIO_26_B/USB_DATA3_C
L11	VSS
L12	CCC_NE0_PLL_VSSA
L13	CCC_NE0_PLL_VDDA
L14	VSS
L15	VDDI2
L16	VSS
L17	VDDI2

Table 15 • **Pin List**

L18	VSS
L19	VDDI1
L20	VSS
L21	VDDI1
L22	VSS
L23	CCC_NW0_PLL_VSSA
L24	CCC_NW0_PLL_VDDA
L25	MSIO174PB0
L26	MSIO174NB0
L27	MSIO178NB18
L28	MSIO178PB18
L29	MSIO182NB18
L30	MSIO182PB18
L31	VSS
L32	MSIO190NB18
L33	MSIO190PB18
L34	MSIO197NB17
M1	MSIO40NB4
M2	MSIO48PB4/SPI_0_SS4/GPIO_19_A
M3	MSIO48NB4/SPI_0_SS5/GPIO_20_A
M4	VSS
M5	MSIO55NB4/SPI_0_SS2/GPIO_9_A/USB_DATA6_A
M6	MSIO60PB4/GPIO_1_B
M7	MSIO60NB4/GPIO_2_B
M8	MSIO63NB3/USB_DATA1_D
M9	VDDI3
M10	MSIO76PB3/MMUART_0_RTS/GPIO_17_B/USB_DATA5_C
M11	MSIO76NB3/MMUART_0_DTR/GPIO_18_B/USB_DATA6_C
M12	CCC_NE1_PLL_VSSA
M13	CCC_NE1_PLL_VDDA
M14	VDDI2
M15	VSS
M16	VDDI2
M17	VSS
M18	VDDI1
M19	VSS
M20	VDDI1
M21	VSS

Table 15 • **Pin List**

M22	CCC_NW1_PLL_VSSA
M23	CCC_NW1_PLL_VDDA
M24	MSIO181NB18
M25	MSIO181PB18
M26	MSIO183NB18
M27	MSIO183PB18
M28	VSS
M29	MSIO188NB18
M30	MSIO188PB18
M31	MSIO191NB18
M32	MSIO191PB18
M33	VDDI17
M34	MSIO197PB17
N1	MSIO40PB4/CCC_NE1_CLKI1
N2	VDDI4
N3	MSIO49NB4/SPI_0_SS7/GPIO_22_A
N4	MSIO49PB4/SPI_0_SS6/GPIO_21_A
N5	MSIO55PB4/SPI_0_SS1/GPIO_8_A/USB_DATA5_A
N6	MSIO53NB4/SPI_1_SS7/GPIO_24_A
N7	VSS
N8	MSIO63PB3/USB_DATA0_D
N9	MSIO67PB3/GPIO_3_B
N10	MSIO67NB3/GPIO_4_B
N11	MSIO71NB3/MMUART_1_DTR/GPIO_12_B
N12	MSIO71PB3/MMUART_1_RTS/GPIO_11_B
N13	VDDI3
N14	VREF2
N15	VDDI2
N16	VREF2
N17	VREF2
N18	VREF1
N19	VDDI1
N20	VREF1
N21	VDDI1
N22	VREF1
N23	MSIO186PB18
N24	MSIO186NB18
N25	VSS
N26	MSIO189NB18
N27	MSIO189PB18

Table 15 • **Pin List**

N28	MSIO193NB18
N29	MSIO193PB18
N30	VDDI18
N31	MSIO201NB17
N32	MSIO201PB17
N33	MSIO203NB17
N34	MSIO208NB17
P1	MSIO39PB4/CCC_NE0_CLKI1
P2	MSIO39NB4
P3	MSIO43PB4
P4	MSIO43NB4/CAN_TX/GPIO_2_A/USB_DATA0_A
P5	VDDI4
P6	MSIO53PB4/SPI_1_SS6/GPIO_23_A
P7	MSIO52NB4/SPI_1_SS5/GPIO_18_A
P8	MSIO58PB4/GPIO_29_A
P9	MSIO58NB4/GPIO_30_A
P10	VSS
P11	MSIO64NB3/USB_DATA3_D
P12	MSIO64PB3/USB_DATA2_D
P13	VSS
P14	VDD
P15	VSS
P16	VDD
P17	VSS
P18	VDD
P19	VSS
P20	VDD
P21	VSS
P22	VDDI18
P23	MSIO192PB18
P24	MSIO192NB18
P25	MSIO195NB18
P26	MSIO195PB18
P27	VDDI18
P28	MSIO198NB17
P29	MSIO198PB17
P30	MSIO199NB17
P31	MSIO199PB17
P32	VSS
P33	MSIO203PB17

Table 15 • **Pin List**

P34	MSIO208PB17
R1	MSIO32PB5/USB_DATA4_B
R2	MSIO32NB5/USB_DATA5_B
R3	VSS
R4	MSIO38NB5
R5	MSIO44PB4/CAN_RX/GPIO_3_A/USB_DATA1_A
R6	MSIO44NB4/CAN_TX_EN_N/GPIO_4_A/USB_DATA2_A
R7	MSIO52PB4/SPI_1_SS4/GPIO_17_A
R8	VDDI4
R9	MSIO54PB4/GPIO_25_A
R10	MSIO54NB4/GPIO_26_A
R11	MSIO57NB4/SPI_1_SS3/GPIO_16_A
R12	MSIO57PB4/SPI_1_SS2/GPIO_15_A
R13	VDDI4
R14	VSS
R15	VDD
R16	VSS
R17	VDD
R18	VSS
R19	VDD
R20	VSS
R21	VDD
R22	VSS
R23	MSIO200PB17
R24	MSIO200NB17
R25	MSIO202NB17
R26	MSIO202PB17
R27	MSIO204NB17
R28	MSIO204PB17
R29	VSS
R30	MSIO205NB17
R31	MSIO205PB17
R32	MSIO207NB17
R33	MSIO207PB17
R34	VDDI17
T1	VDDI5
T2	MSIO31PB5/USB_DATA2_B
T3	MSIO31NB5/USB_DATA3_B
T4	MSIO38PB5/GB13/CCC_SE1_CLKI0
T5	MSIO37NB5

Table 15 • **Pin List**

T6	VSS
T7	MSIO41NB4
T8	MSIO45NB4/I2C_1_SCL/GPIO_1_A/USB_DATA4_A
T9	MSIO45PB4/I2C_1_SDA/GPIO_0_A/USB_DATA3_A
T10	MSIO50NB4/SPI_1_SDI/GPIO_11_A
T11	MSIO50PB4/SPI_1_CLK
T12	MSIO46NB4/SPI_0_SDI/GPIO_5_A/USB_DIR_A
T13	VSS
T14	VPP
T15	VSS
T16	VDD
T17	VSS
T18	VDD
T19	VSS
T20	VDD
T21	VSS
T22	VDDI17
T23	MSIO206PB17
T24	MSIO206NB17
T25	MSIO211NB17
T26	VSS
T27	MSIO209NB17
T28	MSIO209PB17
T29	MSIO210NB17
T30	MSIO210PB17
T31	VDDI17
T32	MSIO212NB17
T33	MSIO212PB17
T34	MSIOD217NB16
U1	MSIO26NB5/GPIO_28_A
U2	MSIO29PB5/USB_STP_B
U3	MSIO29NB5/USB_NXT_B
U4	VDDI5
U5	MSIO37PB5/GB9/CCC_SE0_CLKI0
U6	MSIO33NB5
U7	MSIO41PB4/GB10/CCC_SE0_CLKI1
U8	MSIO36NB5
U9	VSS
U10	MSIO42PB4/GB14/CCC_SE1_CLKI1
U11	MSIO42NB4

Table 15 • **Pin List**

U12	MSIO46PB4/SPI_0_CLK/USB_XCLK_A
U13	VDDI4
U14	VSS
U15	VDD
U16	VSS
U17	VDD
U18	VSS
U19	VDD
U20	VSS
U21	VDD
U22	VSS
U23	MSIO214PB17/GB2/CCC_NW0_CLKI1
U24	MSIO214NB17
U25	MSIO211PB17
U26	MSIO216NB17
U27	MSIO216PB17/CCC_NW0_CLKI0
U28	VDDI17
U29	MSIO215PB17/CCC_NW1_CLKI0
U30	MSIO215NB17
U31	MSIO213PB17/GB6/CCC_NW1_CLKI1
U32	MSIO213NB17
U33	VSS
U34	MSIOD217PB16/GB5/CCC_SW1_CLKI1
V1	MSIO26PB5/GPIO_27_A
V2	VSS
V3	MSIO25NB5
V4	MSIO30PB5/USB_DATA0_B
V5	MSIO30NB5/USB_DATA1_B
V6	MSIO33PB5/USB_DATA6_B
V7	VDDI5
V8	MSIO36PB5/CCC_NE1_CLKI0
V9	MSIO34PB5
V10	MSIO34NB5
V11	MSIO35NB5
V12	MSIO35PB5/CCC_NE0_CLKI0
V13	VSS
V14	VPP
V15	VSS
V16	VDD
V17	VSS

Table 15 • **Pin List**

V18	VDD
V19	VSS
V20	VDD
V21	VSS
V22	VDDI16
V23	MSIOD220PB16/CCC_SW0_CLKI0
V24	MSIOD220NB16
V25	VDDI16
V26	MSIOD222NB16
V27	MSIOD222PB16
V28	MSIOD223NB16
V29	MSIOD223PB16
V30	VSS
V31	MSIOD221NB16
V32	MSIOD218PB16/GB1/CCC_SW0_CLKI1
V33	MSIOD218NB16
V34	MSIOD219NB16
W1	MSIO20PB5
W2	MSIO20NB5
W3	MSIO25PB5
W4	MSIO24NB5
W5	VSS
W6	MSIO23PB5
W7	MSIO23NB5
W8	MSIO27PB5
W9	MSIO27NB5/USB_DATA7_B
W10	VDDI5
W11	MSIO28NB5/USB_DIR_B
W12	MSIO28PB5/USB_XCLK_B
W13	VDDI5
W14	VSS
W15	VDD
W16	VSS
W17	VDD
W18	VSS
W19	VDD
W20	VSS
W21	VDD
W22	VSS
W23	MSIOD227PB16

Table 15 • **Pin List**

W24	MSIOD227NB16
W25	MSIOD229NB16
W26	MSIOD229PB16
W27	VSS
W28	MSIOD231NB16
W29	MSIOD226PB16
W30	MSIOD226NB16
W31	MSIOD221PB16
W32	VDDI16
W33	MSIOD224NB16
W34	MSIOD219PB16/CCC_SW1_CLKI0
Y1	MSIO19NB5
Y2	MSIO19PB5
Y3	VDDI5
Y4	MSIO24PB5
Y5	MSIO18NB5
Y6	MSIO18PB5
Y7	MSIO15NB6
Y8	VSS
Y9	MSIO22NB5
Y10	MSIO22PB5
Y11	MSIO21NB5
Y12	MSIO21PB5
Y13	VSS
Y14	VDD
Y15	VSS
Y16	VDD
Y17	VSS
Y18	VDD
Y19	VSS
Y20	VDD
Y21	VSS
Y22	CCC_SW1_PLL_VDDA
Y23	MSIOD234PB16
Y24	MSIOD234NB16
Y25	MSIOD241NB16
Y26	MSIOD235PB16
Y27	MSIOD235NB16
Y28	MSIOD231PB16
Y29	VDDI16

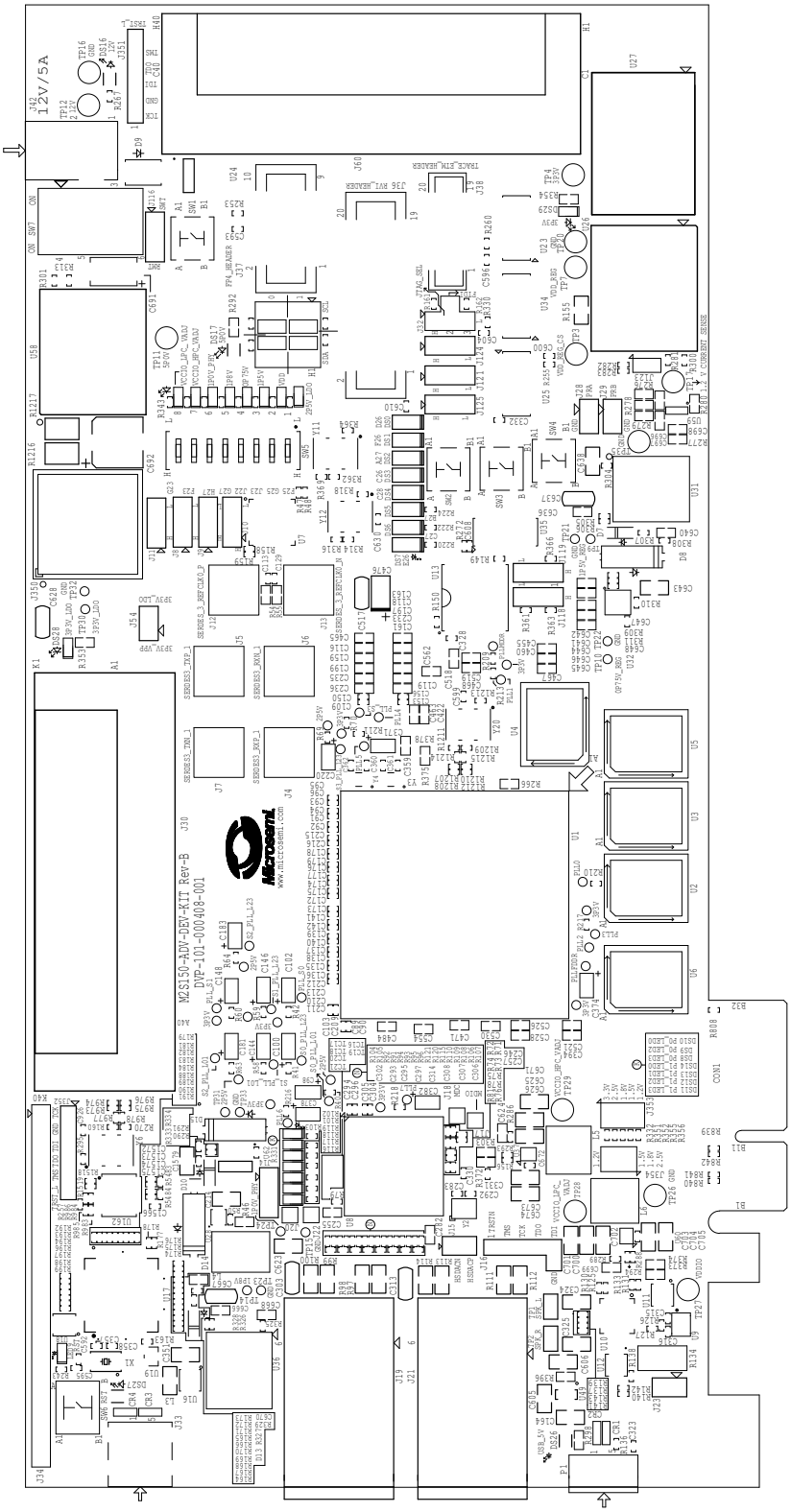
Table 15 • **Pin List**

Y30	MSIOD230PB16
Y31	MSIOD230NB16
Y32	MSIOD228NB16
Y33	MSIOD224PB16
Y34	VSS

6 Board Components Placement

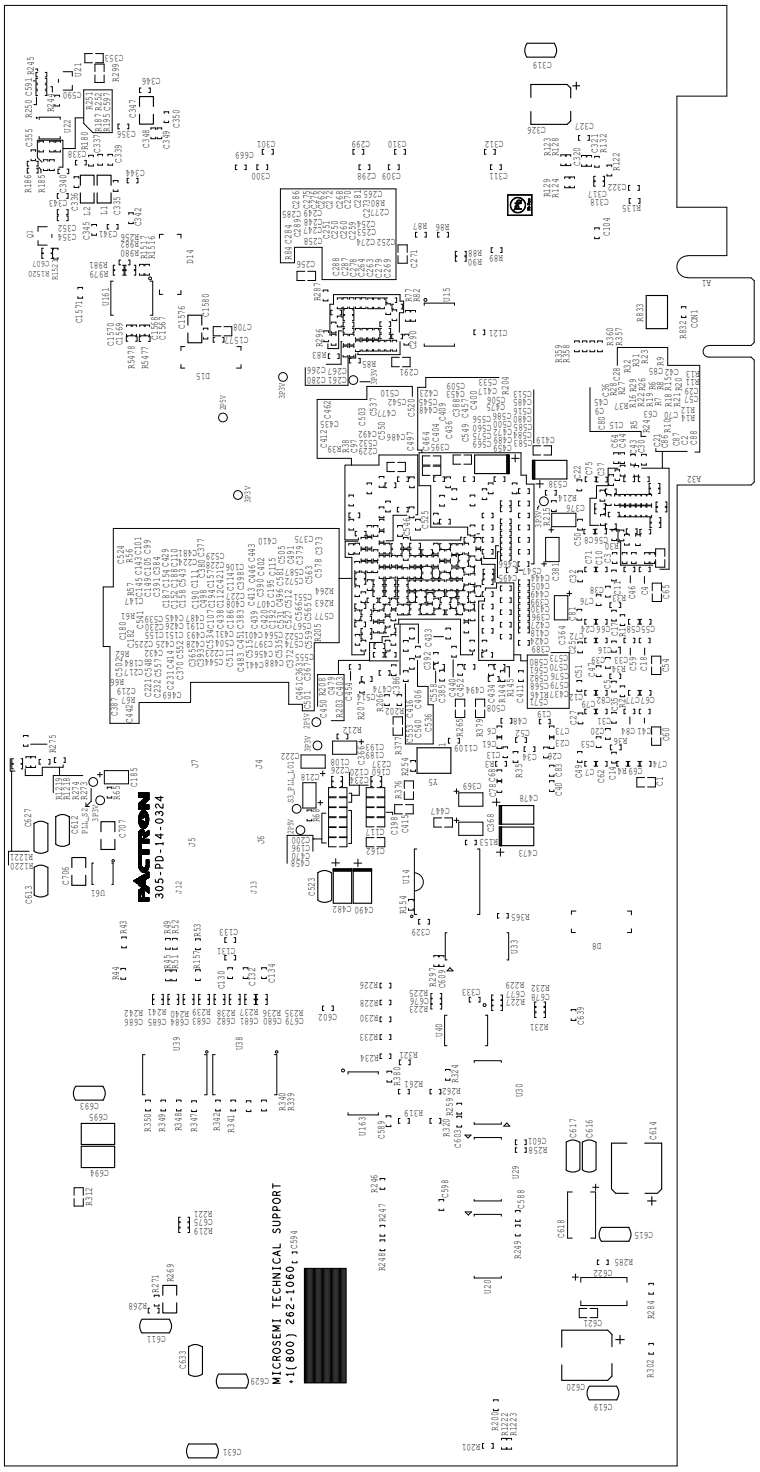
The following figure shows the placement of various components on the SmartFusion2 Advanced Development Kit silkscreen.

Figure 20 • **Silkscreen Top View**



The following figure shows the bottom view of the SmartFusion2 Advanced Development Kit silkscreen.

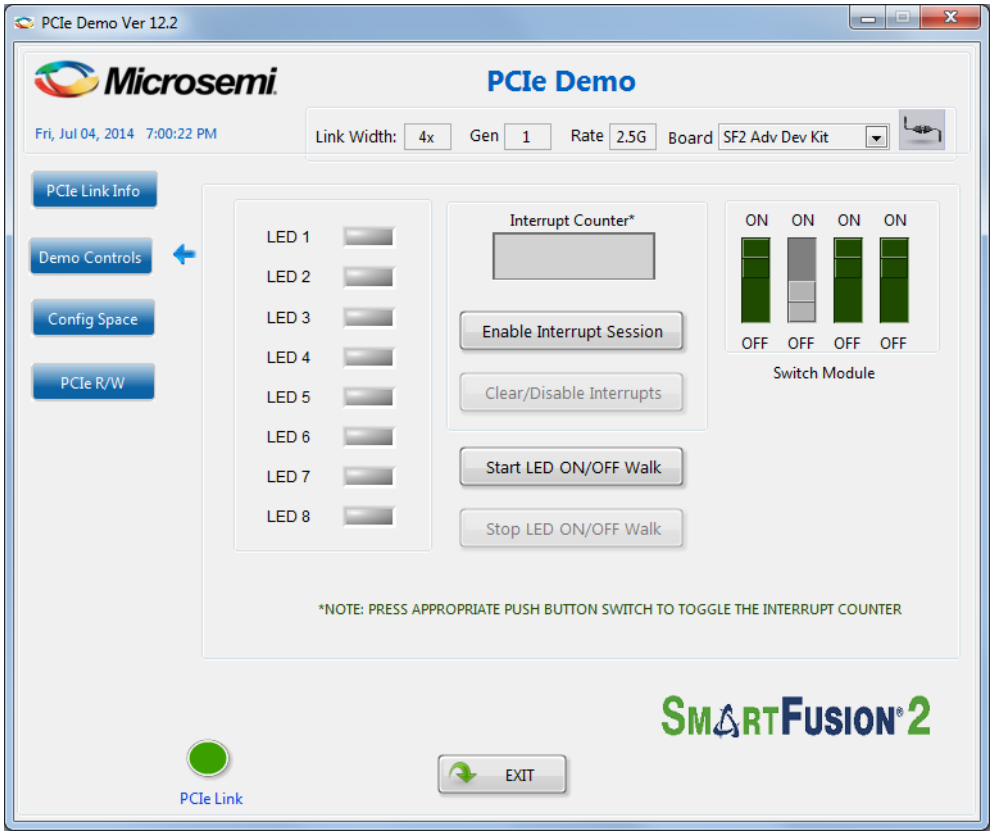
Figure 21 • **Silkscreen Bottom View**



7 Demo Design

The SmartFusion2 M2S150-ADV-DEV-KIT comes with a preloaded PCIe control plane design. to demonstrate the PCIe interface of the SmartFusion2 device. The following figure shows the PCIe demo design window.

Figure 22 • **PCIe Demo Design Window**



For more information about running the demo design, see *SmartFusion2 SoC FPGA PCIe Control Plane Demo Guide for Advanced Development Kit*.

8 Manufacturing Test

The M2S150-ADV-DEV-KIT device contains a manufacturing test program that can be run to verify the functionality of the board. This program contains a list of options that can be run as diagnostics. After Tera Term is set up and the board is powered up, various tests that can be performed on the board are displayed (see Figure 29, page 80). One or more tests can then be selected from the list of available tests.

Before testing the SmartFusion2 Advanced Development Board:

- Download `SEC_KIT_MTD_top.stp` file from *http://www.microsemi.com/document-portal/doc_download/134344-smartfusion2-advanced-development-kit-mtd*.
- Download and install the FTD drivers from *http://www.ftdichip.com/Drivers/D2XX.htm*.

8.1 Programming M2S150-ADV-DEV-KIT

This section provides information about validating the power supply and programming the M2S150-ADV-DEV-KIT for the manufacturing test.

8.1.1 Validating Power Supply

To test and validate the power supply to the board:

1. Connect the following jumpers on the SmartFusion2 Advanced Development Board.
   - Short the **J116** jumper to position 1-2.
   - Short the **J123** jumper to position 2-3.
   - Short the **J353** jumper to position 1-2.
   - Short the **J354** jumper to position 1-2.
   - Short the **J54** jumper to position 1-2.

Note: Before making the jumper connections, switch OFF the **SW7** power supply switch.

2. Connect the 12 V/5 A power supply brick to the **J42** jumper.
3. Switch ON the **SW7** power supply switch.

8.1.2 Programming the FPGA Using Embedded FlashPro5

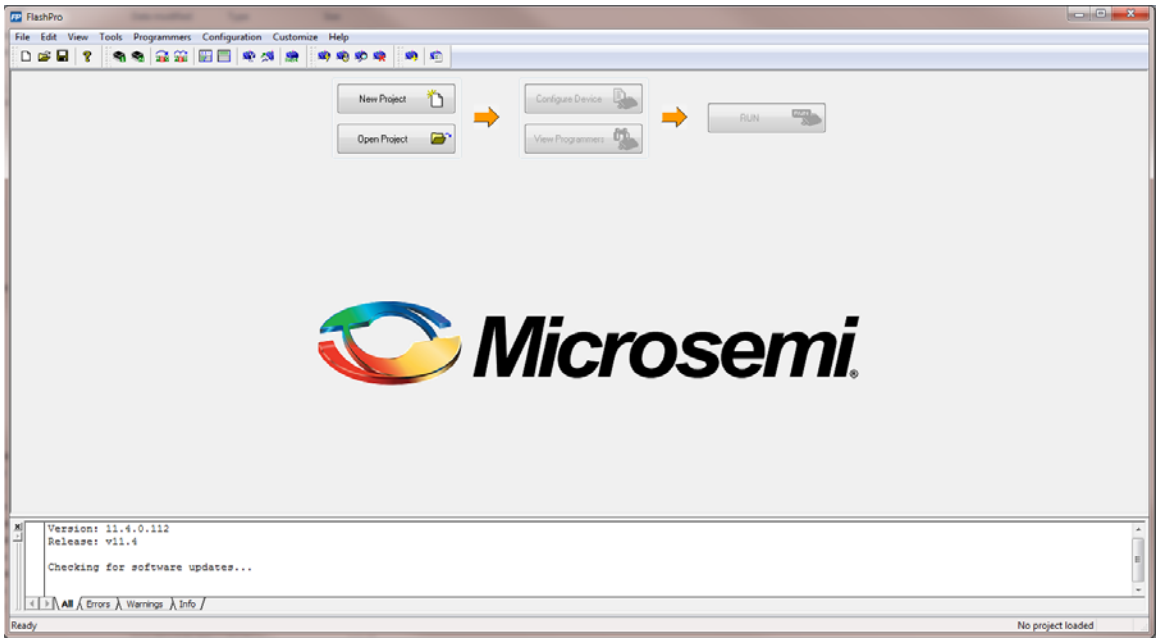
The M2S150-ADV-DEV-KIT has an embedded FlashPro5 programmer; therefore, an external programmer is not required to program the SmartFusion2 device. The device can be programmed using the embedded FlashPro5, provided the FlashPro software is installed on the host PC.

Note: The board can also be programmed using FlashPro4. To program the board using FlashPro4, connect the FlashPro4 header to the **J37** connector, and change the position of the **J124** jumper to pin 2-3.

To program the device using embedded FlashPro5:

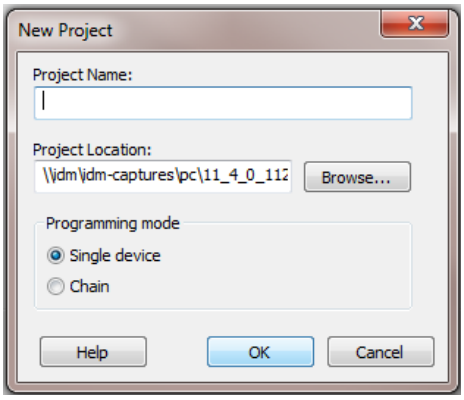
1. Connect the following jumpers on the SmartFusion2 Advanced Development Board:
   - Short the **J124** jumper to position 1-2.
   - Short the **J121** jumper to position 1-2.
   - Short the **J32** jumper to position 1-2.
2. Connect one end of the mini USB to Type A USB cable to the **J33** jumper, and other end to the USB port of the host PC.
3. Launch the FlashPro v11.4 software.

Figure 23 • **FlashPro Window**



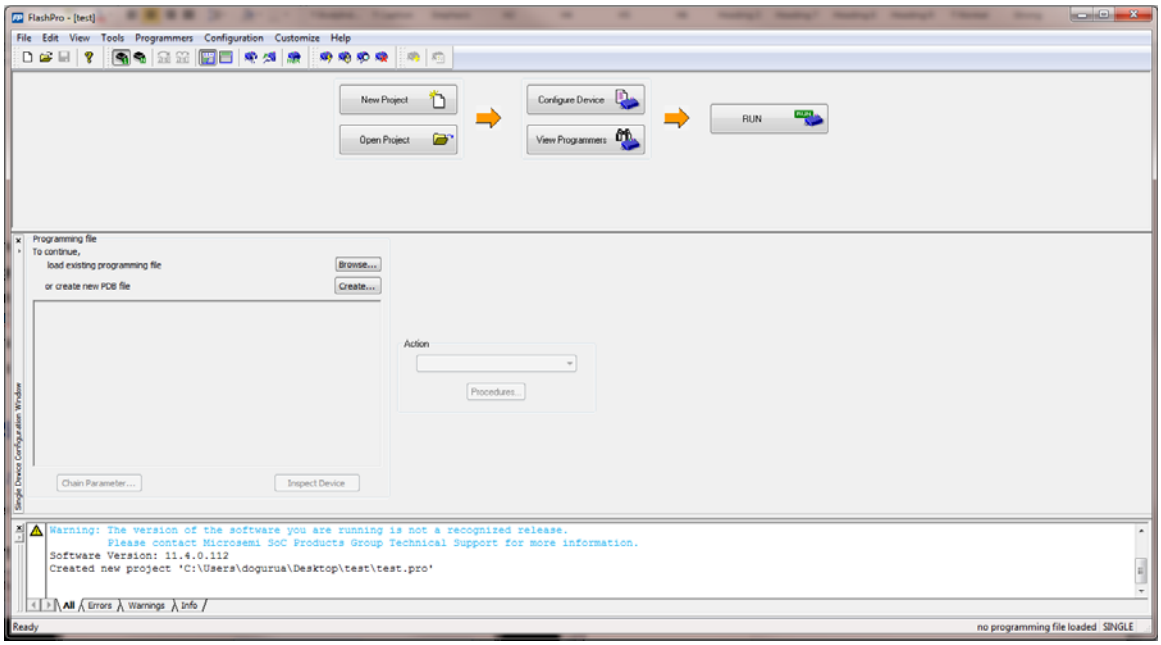
4. Click **New Project** to create a new project.
5. In the **New Project** window, do the following, and click **OK**.
   - Enter a project name.
   - Select **Single device** as the programming mode.

Figure 24 • **New Project Window**



6. Click **Configure Device**.

Figure 25 • **Configuring the Device**



7. Click **Browse,** and select the `SEC_KIT_MTD_top.stp` file from the **Load Programming File** window.
8. Click **Program** to program the device.
9. Press the **SW4** switch.
   The corresponding DS7 LED starts glowing, indicating that the device is programmed successfully.

8.2 Running the Manufacturing Test

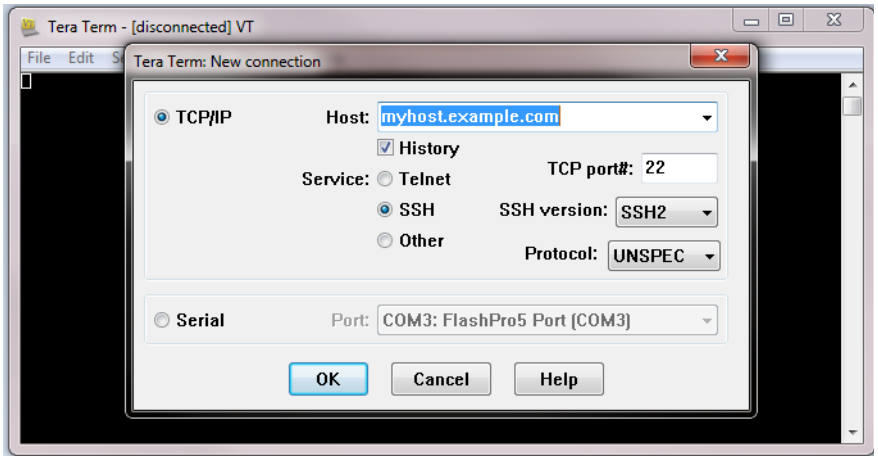
This section describes how to run the manufacturing test for the SmartFusion2 Advanced Development Board.

8.2.1 Setting Up Tera Term

To set up Tera Term for the manufacturing test:

1. Connect one end of the mini USB to Type A USB cable to **J33,** and other end to the USB port of the host PC.
2. Launch **Tera Term** from the Start menu.

Figure 26 • **Tera Term New Connection Window**

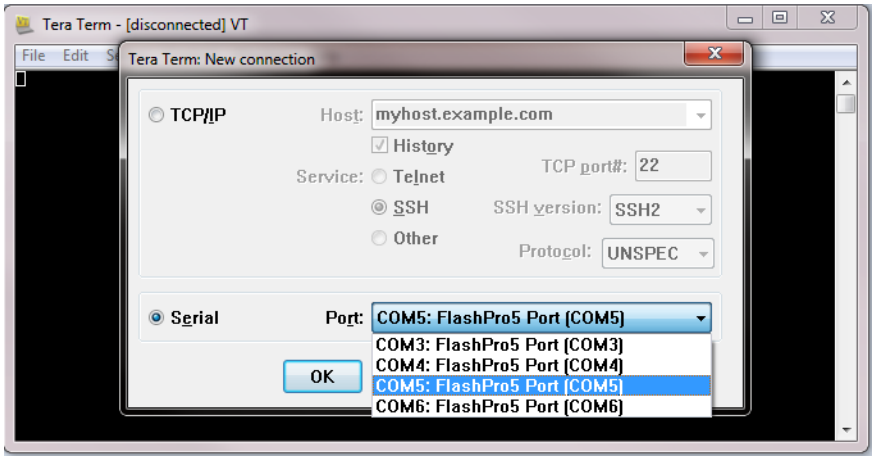


3. Select the **Serial** radio button.
4. Select a port from the **Port** drop-down list, and click **OK**.

Notes:

- When using a USB cable for Tera Term communication, four FlashPro5 COM ports are available in the **Port** drop-down list, as shown in the following figure. Select the third FlashPro5 COM port to establish the connection with the host PC.
- If FlashPro5 drivers are not installed properly, the drop-down list does not list FlashPro5 COM ports.

Figure 27 • **Tera Term New Connection Window**



5. On the **Tera Term Serial port setup** window, select the COM port to establish connection with the host PC, and enter the following Tera Term settings.
   - Baud rate = 57600
   - Data = 8 bit
   - Parity = none
   - Stop = 1 bit
   - Flow control = none

Figure 28 • **Tera Term Serial Port Setup Window**

6. Click **OK**.

8.2.2 Setting Up Jumpers

The following table specifies the jumper settings required to perform various tests on the SmartFusion2 Advanced Development Board.

Table 16 • **Jumper Settings for Manufacturing Test**

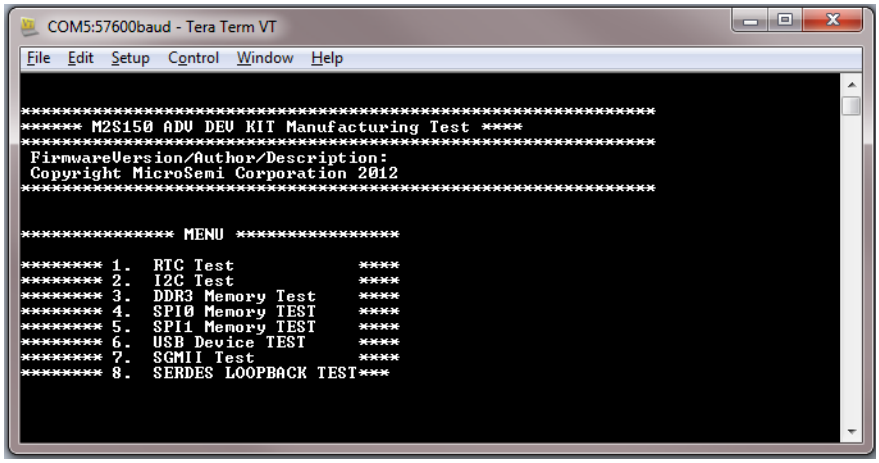
Interface	Jumper Settings
RTC test	–
I2C test	On header (H1), short 10-6 and 11-7.
DDR3 memory test	–
SPI0 memory test	Short J118 pin 1-2.
SPI1 memory test	Short J119 pin 1-2.
USB device test	Connect Micro B to P1, and connect the other end of the cable to the host PC (type A). This cable is required for testing on board USB device interface.
	Short J23 pin 1-2.
SGMII test	Connect an Ethernet cable to J19, and connect other end of the cable to the 1 Gbps Ethernet switch or network.
	Short J11 pin 1-2.
	Short J8 pin 1-2.
	Short J14 pin 1-2.
SerDes loopback test	Connect J4 to J5 and J6 to J7 using an SMA-to-SMA cable.
	Loopback cable (5 Gbps data rate).
	Short J11 pin 1-2.
	Short J8 pin 1-2.

8.2.3 Running the Test

After the device is programmed and the jumper settings are applied, follow these steps to run the manufacturing test.

1. Press the **SW6** reset switch on the M2S150-ADV-DEV-KIT board to reset the board and begin the tests.
   When the setup is completed, all tests are listed in the HyperTerminal window, as shown in the following figure.

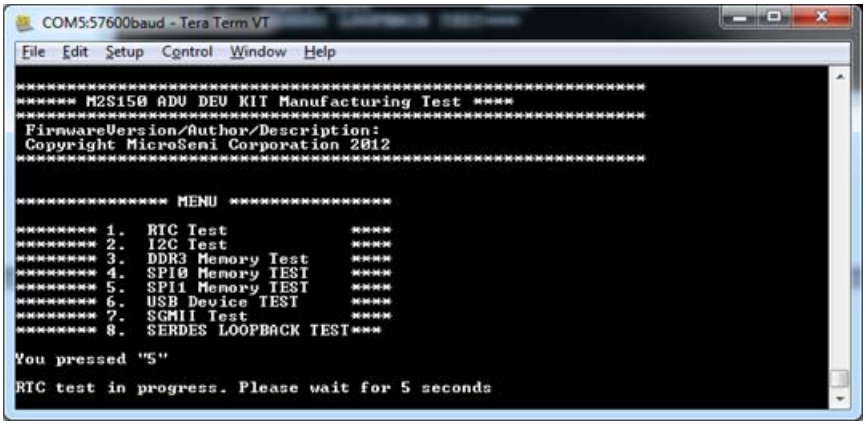
Figure 29 • **Test Menu**



If the list of tests does not appear, press the **SW6** reset switch again. If the list still does not appear, then check all the jumpers and Tera Term settings.

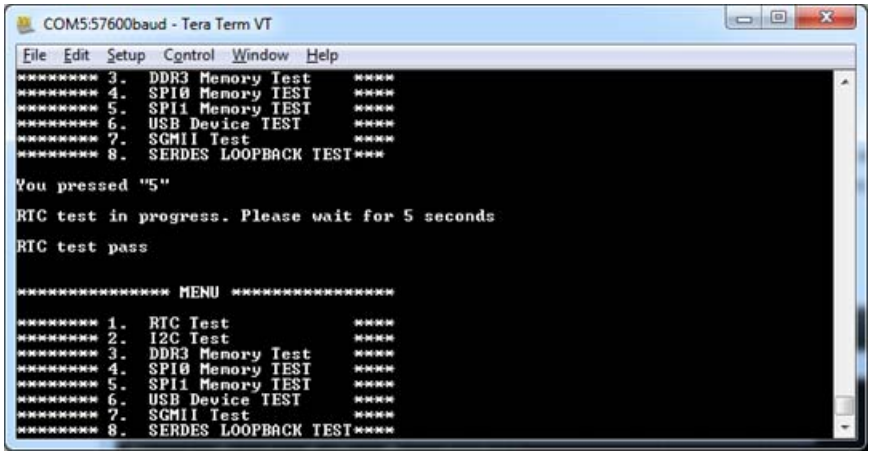
2. Press **1** to run the RTC test.
   The following message appears.

Figure 30 • **Running RTC Test**



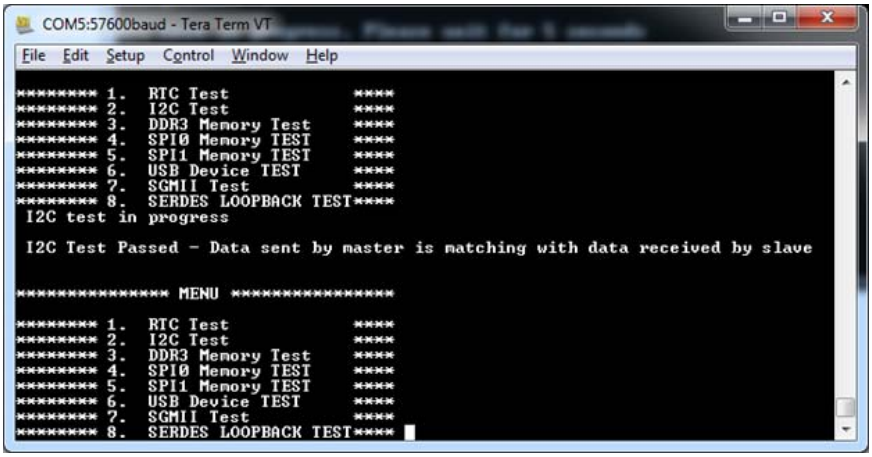
When the test is passed, the following message appears.

Figure 31 • **RTC Test Passed**



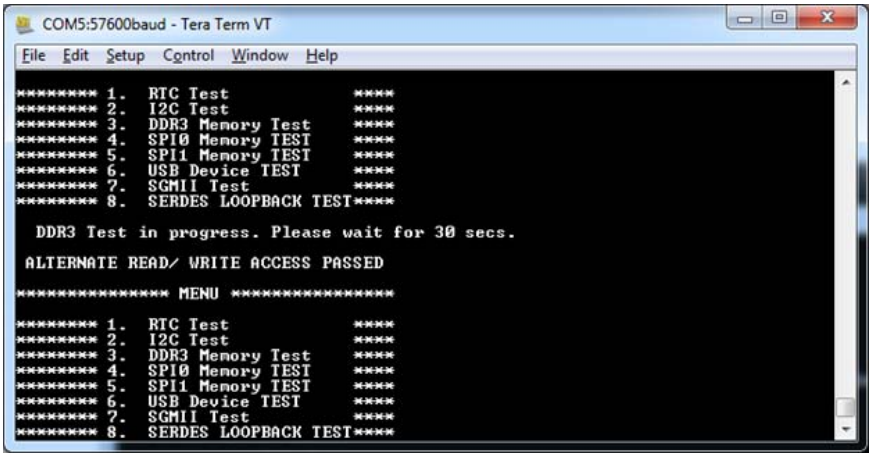
3. Press **2** to run the I2C loopback test. Wait for five seconds for the test to be run. When the test is passed, the following message appears.

Figure 32 • **I2C Test Passed**



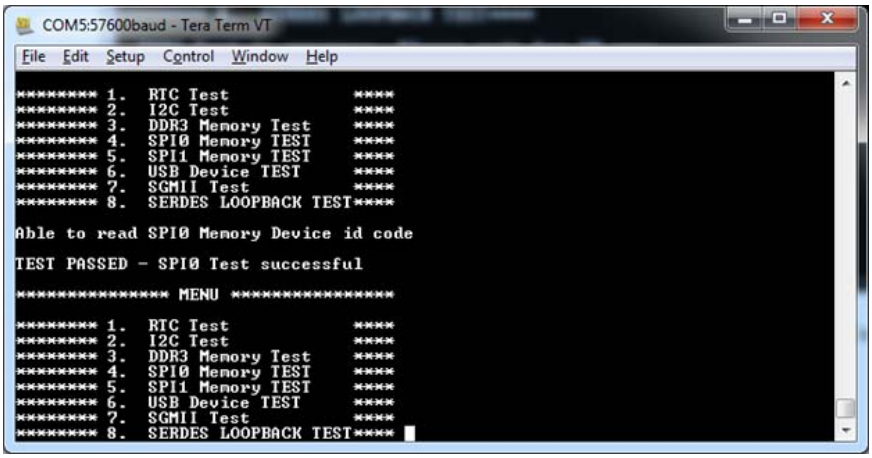
4. Press **3** to run the DDR3 memory test. Wait for 30 seconds for the test to be run. When the test is passed, the following message appears.

Figure 33 • **DDR3 Memory Test Passed**



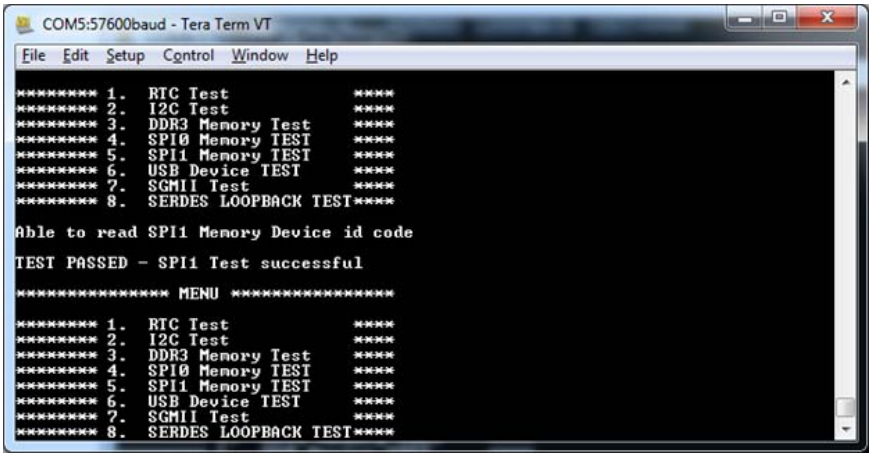
5. Press **4** to run the SPI0 memory test.
   When the test is passed, the following message appears.

Figure 34 • **SPI0 Memory Test Passed**



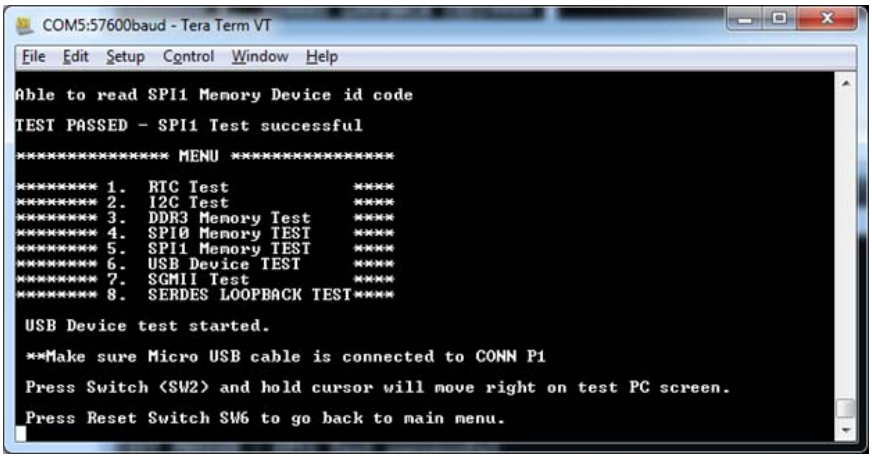
6. Press **5** to run the SPI1 memory test.
   When the test is passed, the following message is appears.

Figure 35 • **SPI1 Memory Test Passed**



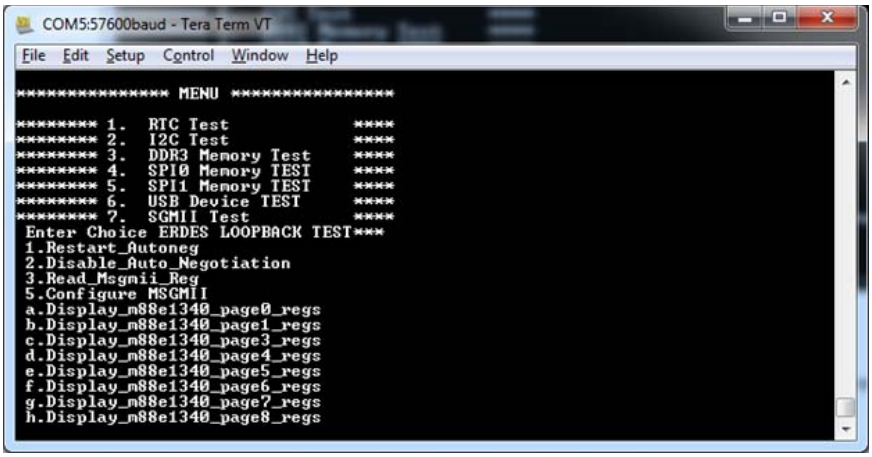
7. Press **6** to run the USB device test.
   When the test begins, the following message appears.

Figure 36 • **USB Device Test Passed**



8. Press and hold the **SW2** switch on the board, and observe the mouse cursor moving to the right side.
9. Press **SW6** reset switch go back to the main menu.
10. Press **7** to run the SGMII test.
    When the test begins, the DS1 LED is OFF. The DS10 LED starts glowing, and the DS8 LED starts blinking. The following message appears.

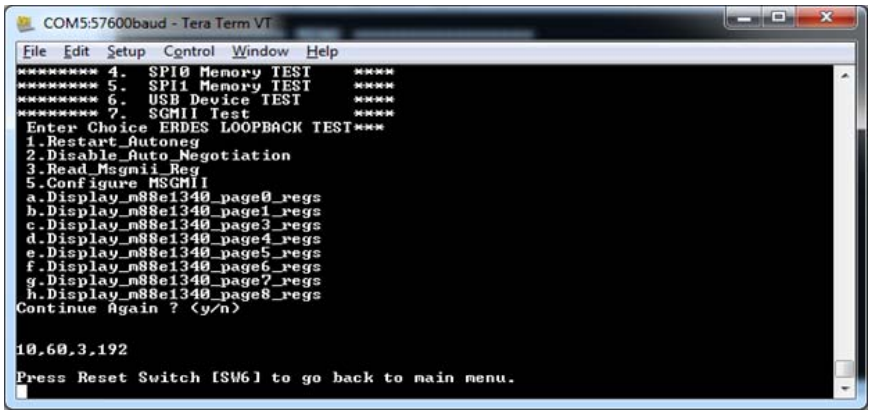
Figure 37 • **SGMII Test**



Note: If this message is not displayed, or if DS10 and DS8 LEDs do not blink, switch ON and OFF the **SW7** power supply switch on the board, and run the DDR3 test by pressing 3.

11. Press **7** to repeat the SGMII test.
    A confirmation message is displayed,
12. Press **n** twice.
    When the test is passed, the IP address of the host PC is displayed, as shown in the following figure.

Figure 38 • **SGMII Test Passed**

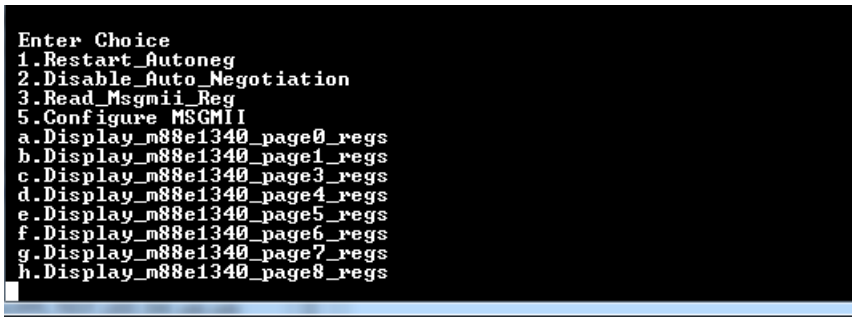


Note: IP address may vary from one PC to the other PC.

13. Press the **SW6** reset switch on the board to go back to the main menu.

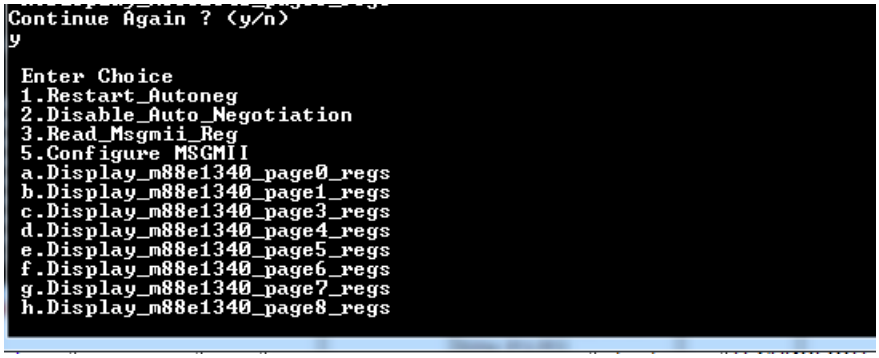
14. If the IP address is not displayed, perform the following steps to get the IP address.
    i. Press **7** to run the SGMII test.

Figure 39 • **SGMII Debug Test**



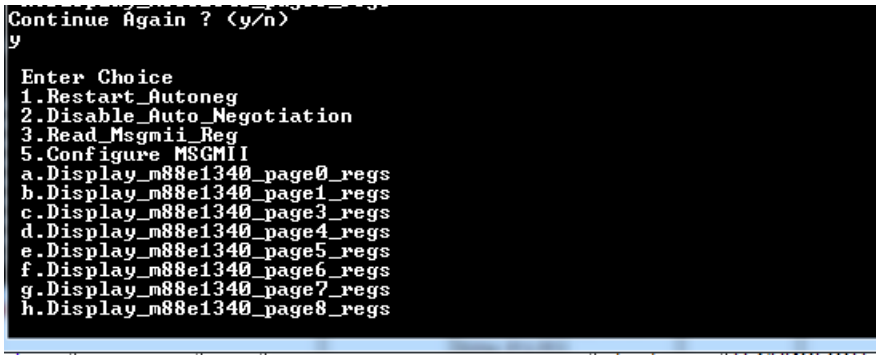
    ii. Press **1** to restart auto-negotiation, and press **y** to continue.

Figure 40 • **SGMII Debug Test**



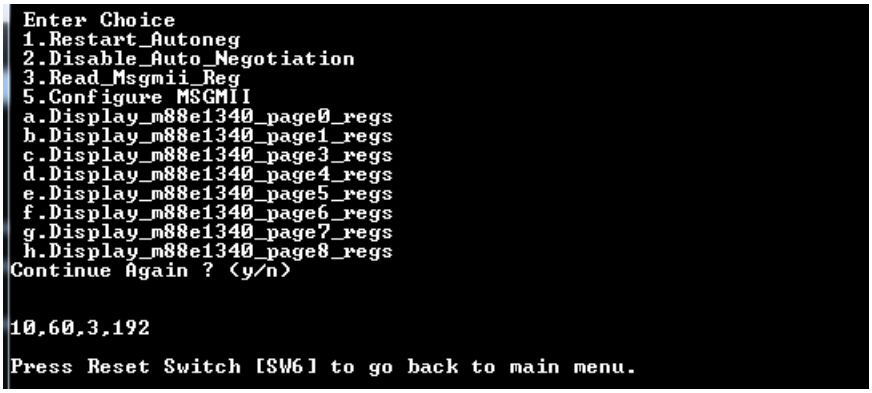
    iii. Press **2** to disable auto-negotiation, and press **y** to continue.

Figure 41 • **SGMII Debug Test**



iv. Press **n** twice to not repeat the action and to get the IP address, as shown in the following figure.

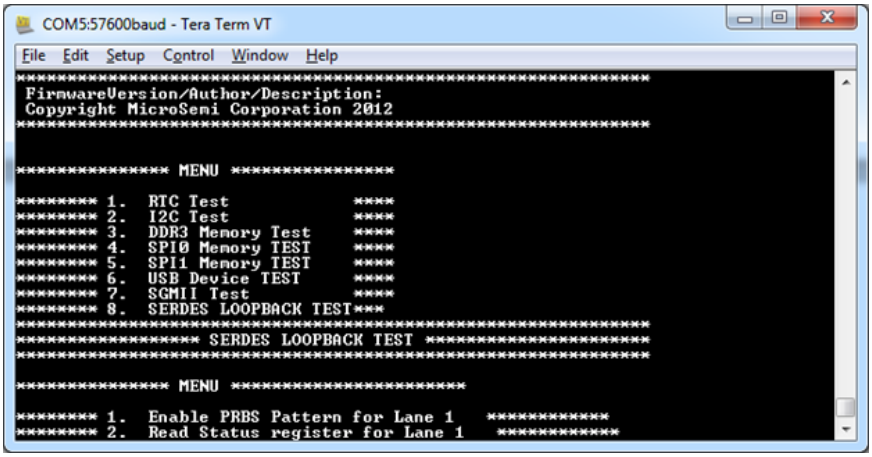
Figure 42 • **SGMII Debug Test Passed**



15. Press **SW6** to go back to the main menu.
16. Press **8** to run the SerDes loopback test.

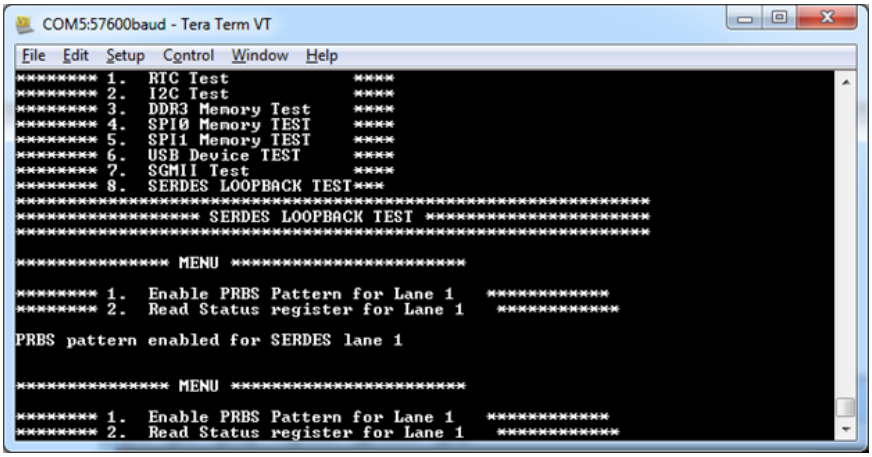
Note: Ensure that the loopback cable is connected. (See Setting Up Jumpers, page 79.)

Figure 43 • **SerDes Loopback Test**



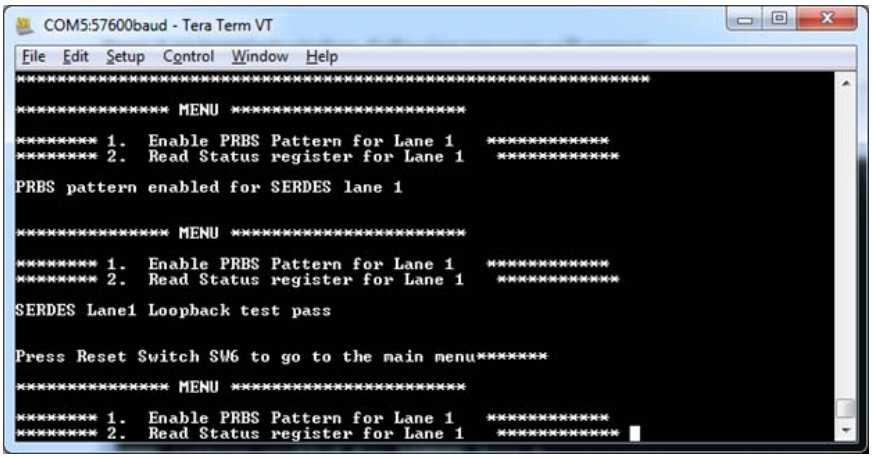
17. Press 1 to enable PRBS pattern for Lane 1.

Figure 44 • **SerDes Loopback Test - Enabling PRBS Pattern for Lane 1**



18. Press **2** to read the status register for Lane 1.
    When the test is passed, the following message appears.

Figure 45 • **SerDes Loopback Passed**



19. Press the **SW6** reset switch to go back to the main menu.