32-Channel High Voltage Amplifier Array

Features

- 32 independent high voltage amplifiers
- 300V operating voltage
- 295V output voltage
- 2.2V/µs typical output slew rate
- Adjustable output current source limit
- Adjustable output current sink limit
- Internal closed loop gain of 72V/V
- 12MΩ feedback impedance
- Layout ideal for die applications

Applications

- MEMS (microelectromechanical systems) driver
- Piezoelectric transducer driver
- Optical crosspoint switches (using MEMS technology)

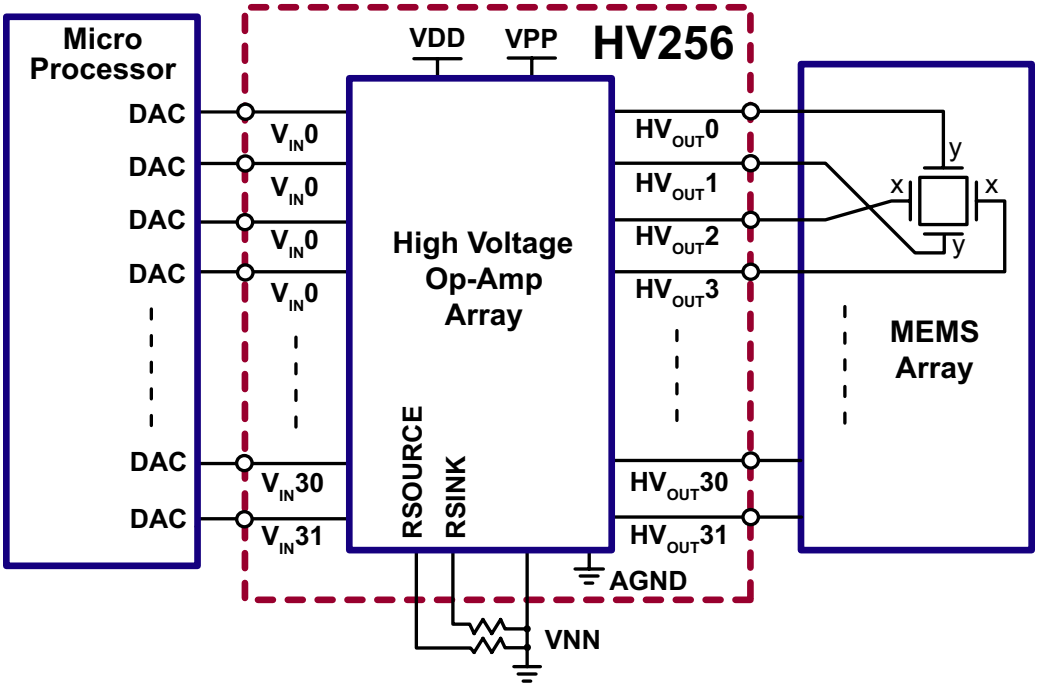
General Description

The Supertex HV256 is a 32-channel, high voltage, amplifier array integrated circuit. It operates on a single high voltage supply, up to 300V, and two low voltage supplies, V_{DD} and V_{NN}.

The input voltage range is from 0 to 4.096V. The internal closed loop gain is 72V/V, giving an output voltage of 295V when 4.096V is applied. Input voltages of up to 5.0V can be applied, but will cause the output to saturate. The maximum output voltage swing is 5.0V below the V_{PP} high voltage supply. The outputs can drive capacitive loads of up to 3000pF.

The maximum output source and sink current can be adjusted by using two external resistors. An external R_{SOURCE} resistor controls the maximum sourcing current and an external R_{SINK} resistor controls the maximum sinking current. The current limit is approximately 12.5V divided by the external resistor value. The setting is common for all 32 outputs. A low voltage silicon junction diode is made available to help monitor the die temperature.

Typical Application Circuit



Ordering Information

Part Number	Package Option	Packing
HV256FG-G	100-Lead MQFP	66/Tray

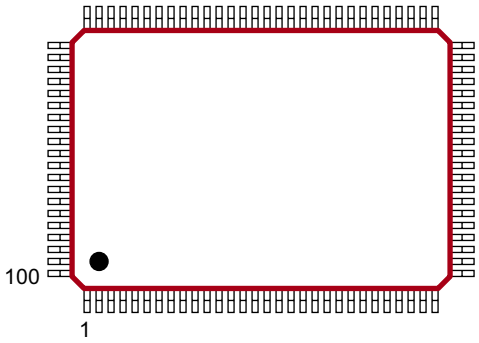
-G denotes a lead (Pb)-free / RoHS compliant package

Absolute Maximum Ratings

Parameter	Value
V_{PP}, High voltage supply	310V
AV_{DD}, Analog low voltage positive supply	8.0V
DV_{DD}, Digital low voltage positive supply	8.0V
AV_{NN}, Analog low voltage negative supply	-7.0V
DV_{NN}, Digital low voltage negative supply	-7.0V
Logic input voltage	-0.5V to DV_{DD}
V_{SIG}, Analog input signal	0V to 6.0V
Storage temperature range	-65°C to 150°C
Maximum junction temperature	150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Pin Configuration



100-Lead MQFP
(top view)

Product Marking

Top Marking

YY = Year Sealed
WW = Week Sealed
L = Lot Number
C = Country of Origin
A = Assembler ID
= "Green" Packaging

Package may or may not include the following marks: Si or

100-Lead MQFP

Typical Thermal Resistance

Package	θ_{ja}
100-Lead MQFP	39°C/W

Operating Conditions

Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{PP}	High voltage positive supply	125	-	300	V	---
V_{DD}	Low voltage positive supply	6.0	-	7.5	V	---
V_{NN}	Low voltage negative supply	-4.5	-	-6.5	V	---
I_{PP}	V_{PP} supply current	-	-	0.8	mA	V_{PP} = 300V, All HV_{OUT} = 0V No load
I_{DD}	V_{DD} supply current	-	-	5.0	mA	V_{DD} = 6.0V to 7.5V
I_{NN}	V_{NN} supply current	-6.0	-	-	mA	V_{NN} = -4.5V to -6.5V
T_J	Operating temperature range	-10	-	85	°C	---

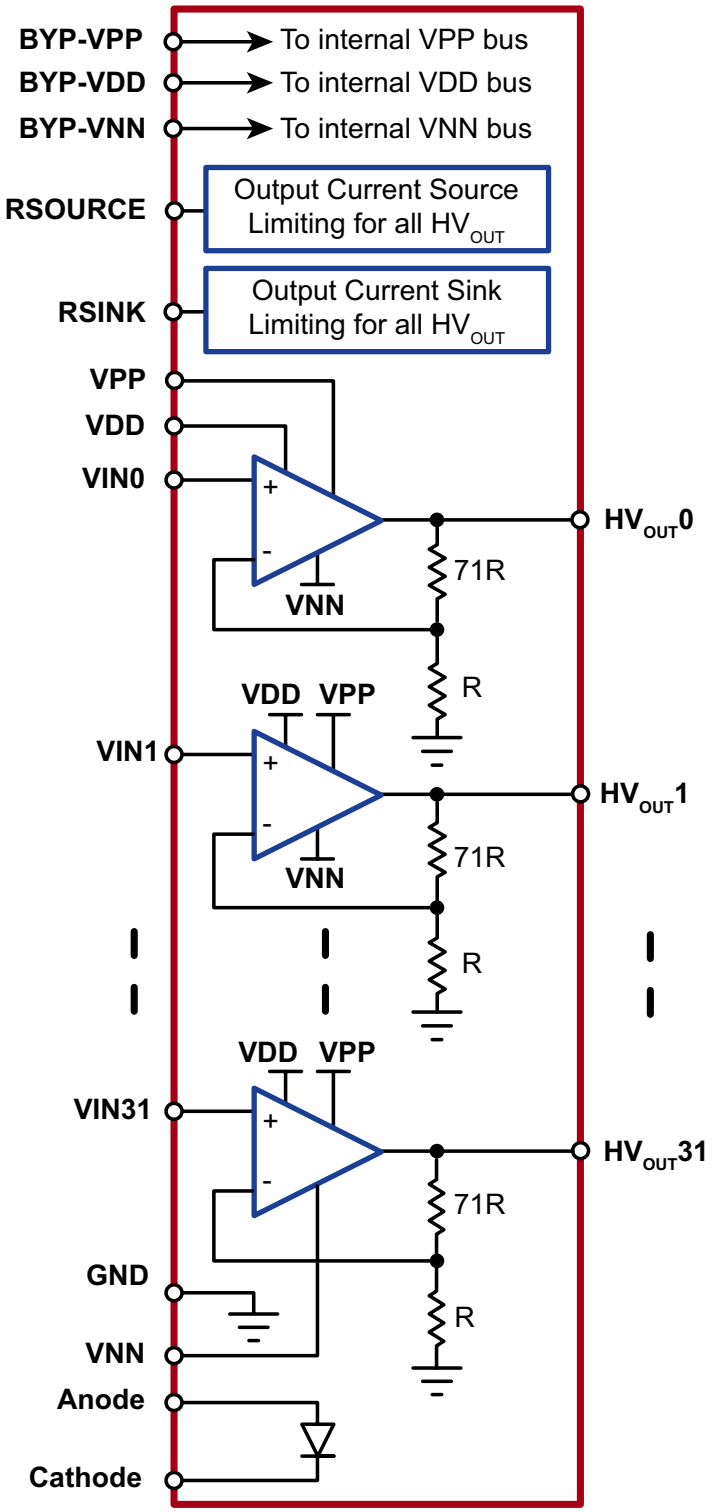
Electrical Characteristics *(over operating conditions, unless otherwise specified*

Sym	Parameter	Min	Typ	Max	Units	Conditions
HV_{OUT}	HV_{OUT} voltage swing	0	-	V_{PP} -5.0	V	---
V_{IN}	Input voltage range	0	-	5.0	V	---
V_{INOS}	Input voltage offset	-	-	±50	mV	Input referred
SR	HV_{OUT} slew rate rise	-	2.2	-	V/µs	No load
	HV_{OUT} slew rate fall	-	2.0	-	V/µs	No load
BW	HV_{OUT} -3dB channel bandwidth	-	4.0	-	KHz	V_{PP} = 300V
A_O	Open loop gain	70	100	-	dB	---
A_V	Closed loop gain	68.4	72.0	75.6	V/V	---
R_{FB}	Feedback resistance from HV_{OUT} to ground	9.6	12.0	-	MΩ	---
C_{LOAD}	HV_{OUT} capacitive load	0	-	3000	pF	---
I_{SOURCE}	HV_{OUT} sourcing current limiting range	385	550	715	µA	R_{SOURCE} = 25KΩ
I_{SINK}	HV_{OUT} sinking current limiting range	385	550	715	µA	R_{SINK} = 25KΩ
R_{SOURCE}	External resistance range for setting maximum current source	25	-	250	KΩ	---
R_{SINK}	External resistance range for setting maximum current sink	25	-	250	KΩ	---
CT_{DC}	DC channel to channel crosstalk	-80	-	-	dB	---
PSRR	Power supply rejection ratio for V_{PP}, V_{DD}, V_{NN}	-40	-	-	dB	---

Temperature Diode

Sym		Min	Typ	Max	Units	Conditions
PIV	Peak inverse voltage	-	-	5.0	V	cathode to anode
V_F	Forward diode drop	-	0.6	-	V	I_F = 100µA, anode to cathode at T_A = 25°C
I_F	Forward diode current	-	-	100	µA	anode to cathode
T_C	V_F temperature coefficient	-	-2.2	-	mV/°C	anode to cathode

HV256 Block Diagram



Power Up/Down Issues

External Diode Protection

The device can be damaged due to improper power up / down sequence. To prevent damage, please follow the acceptable power up / down sequences, and add two external diodes as shown in the diagram on the right. The first diode is a high voltage diode across VPP and VDD, where the anode of the diode is connected to VDD and the cathode of the diode is connected to VPP. Any low current, high voltage diode, such as a 1N4004, will be adequate. The second diode is a Schottky diode across VNN and DGND, where the anode of the Schottky diode is connected to VNN, and the cathode is connected to DGND. Any low current Schottky diode such as a 1N5817 will be adequate.

Acceptable Power Up Sequences

The HV256 can be powered up with any of the following sequences listed below.

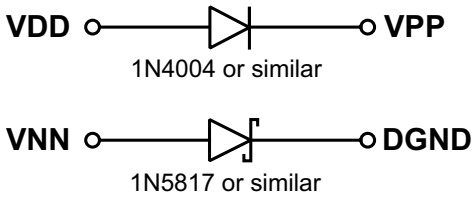
1) VPP 2) VNN 3) VDD 4) Inputs and Anode
1) VNN 2) VDD 3) VPP 4) Inputs and Anode
1) VDD & VNN 2) Inputs 3) VPP 4) Anode

Acceptable Power Down Sequences

The HV256 can be powered down with any of the following sequences listed below:

1) Inputs and Anode 2) VDD 3) VNN 4) VPP
1) Inputs and Anode 2) VPP 3) VDD 4) VNN
1) Anode 2) VPP 3) Inputs 4) VNN & VDD

External Diode Protection Connection



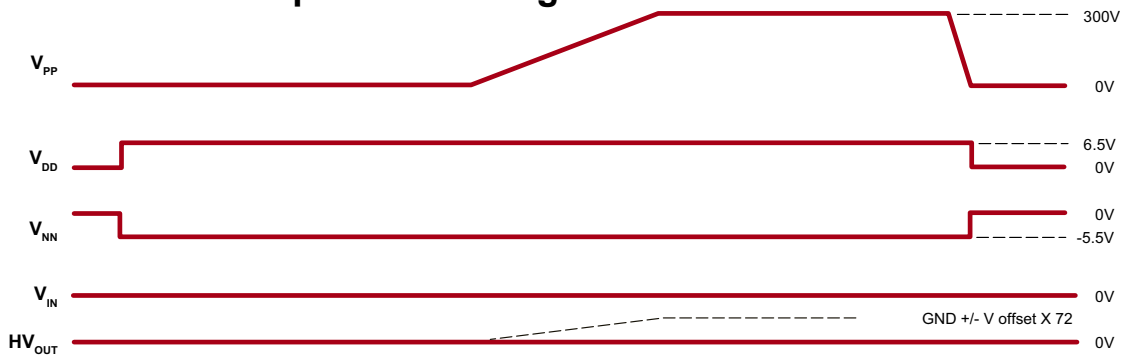
Suggested Power Up/Down Sequence

The HV256 needs all power supplies to be fully up and all channels refreshed with V_{SIG} = 0V to force all high voltage outputs to 0V. Before that time, the high voltage outputs may have temporary voltage excursions above or below GND level depending on selected power up sequence. To minimize the excursions:

1. The VDD and VNN power supplies should be applied at the same time (or within a few nanoseconds).

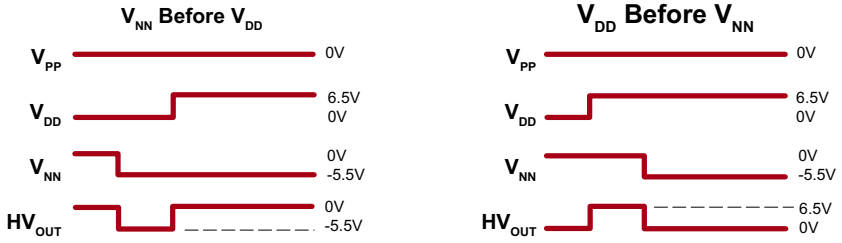
Suggested VPP ramp up speed should be 10msec or longer and ramp down to be 1msec or longer.

Recommended Power Up/Down Timing



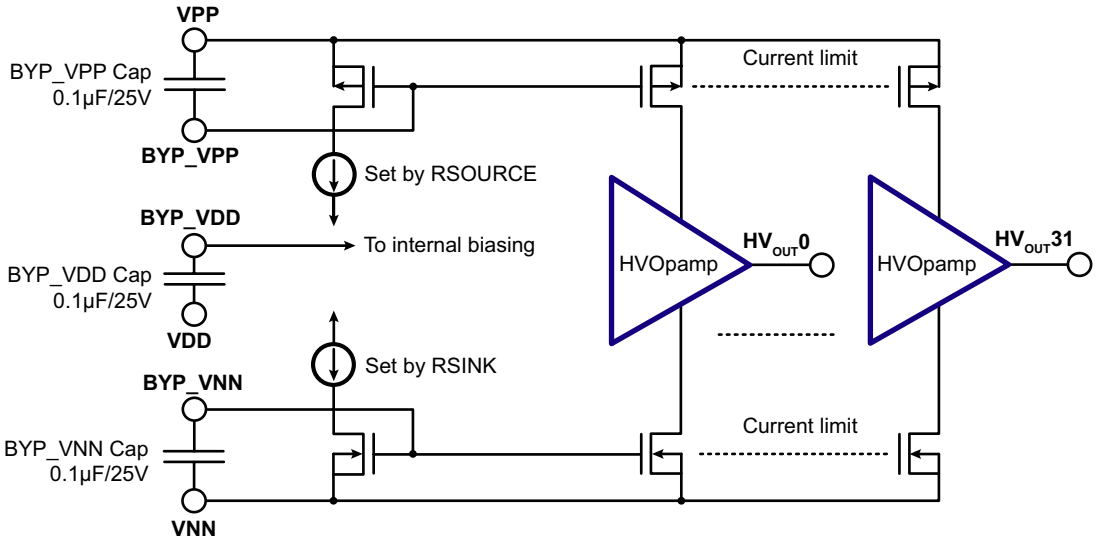
HV_{OUT} Level at Power Up

Power Up Sequence

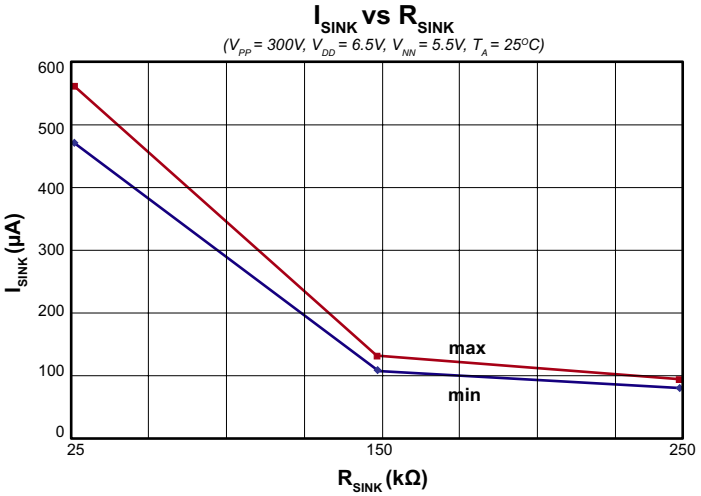


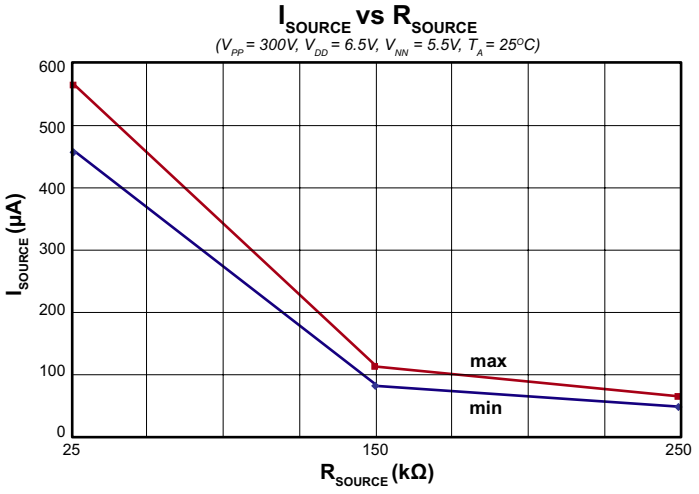
RSINK / RSOURCE

The VDD_BYP, VDD_BYP, and VNN_BYP pins are internal, high impedance current, mirror gate nodes, brought out to mantain stable opamp biasing currents in noisy power supply environments. 0.1uF/25V bypass capacitors, added from the VPP_BYP pin to VPP, from VDD_BYP pin to VDD, and from VNN_BYP to VNN, will force the high impedance gate nodes to follow the fluctuation of power lines. The expected voltages at the VDD_BYP, and VNN_BYP pins are typically 1.5 volts from their respectful power supply. The expected voltage at VPP_BYP is typically 3.0V below V_{PP}.



Typical Characteristics

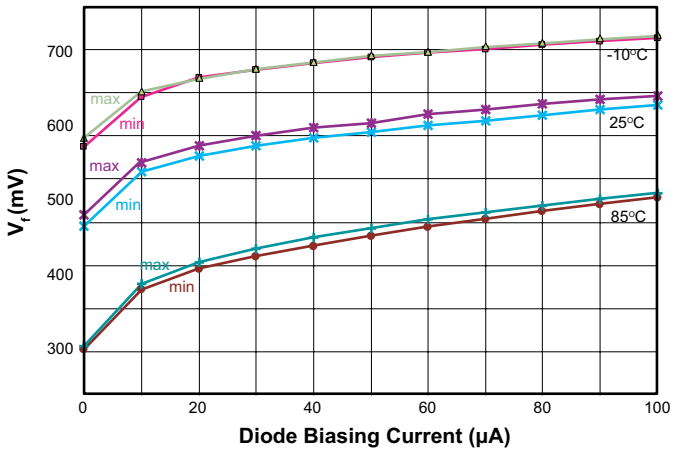




Typical Characteristics (cont.)

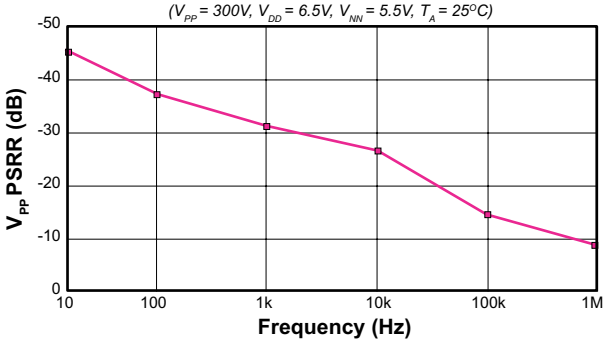
Temperature Diode vs Temperature

(V_{PP} = 300V, V_{DD} = 6.5V, V_{NN} = 5.5V)



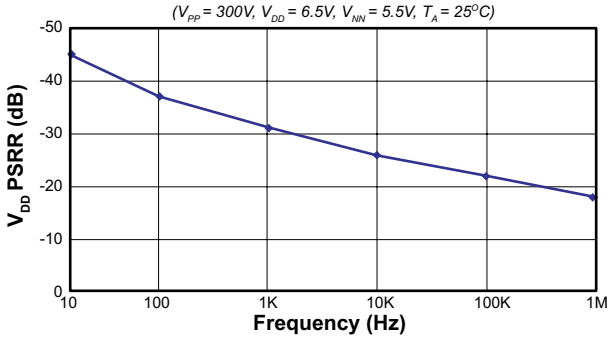
V_{PP} PSRR vs Frequency

(V_{PP} = 300V, V_{DD} = 6.5V, V_{NN} = 5.5V, T_A = 25°C)



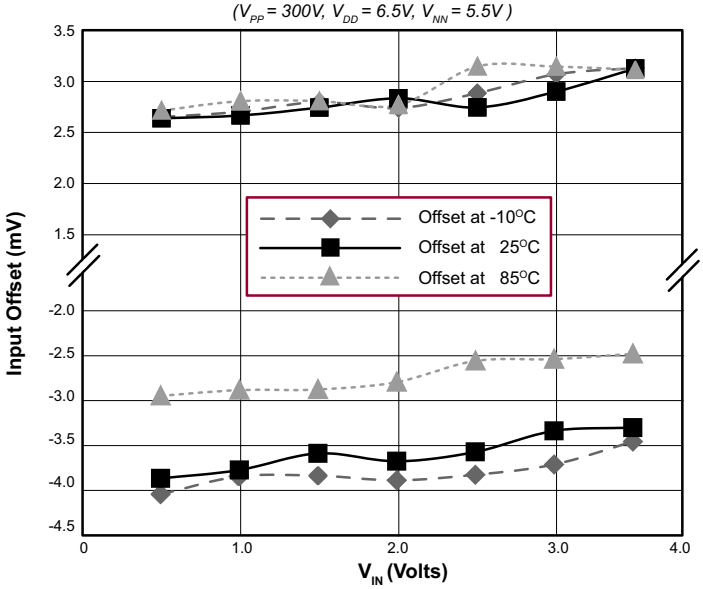
V_{DD} PSRR vs Frequency

(V_{PP} = 300V, V_{DD} = 6.5V, V_{NN} = 5.5V, T_A = 25°C)



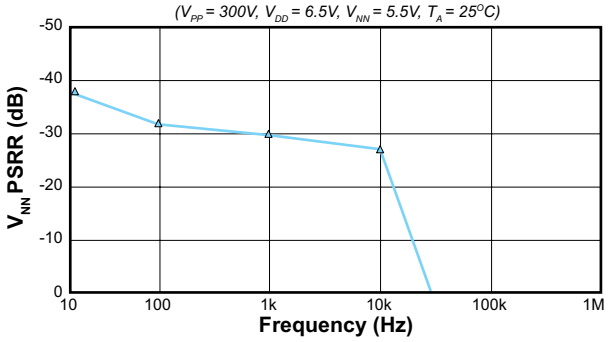
Input Offset vs V_{IN} and Temperature

(V_{PP} = 300V, V_{DD} = 6.5V, V_{NN} = 5.5V)



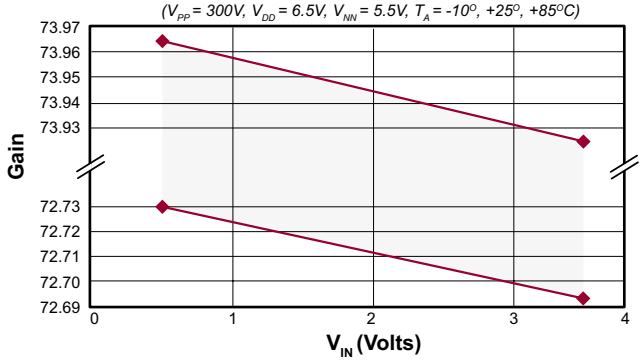
V_{NN} PSRR vs Frequency

(V_{PP} = 300V, V_{DD} = 6.5V, V_{NN} = 5.5V, T_A = 25°C)

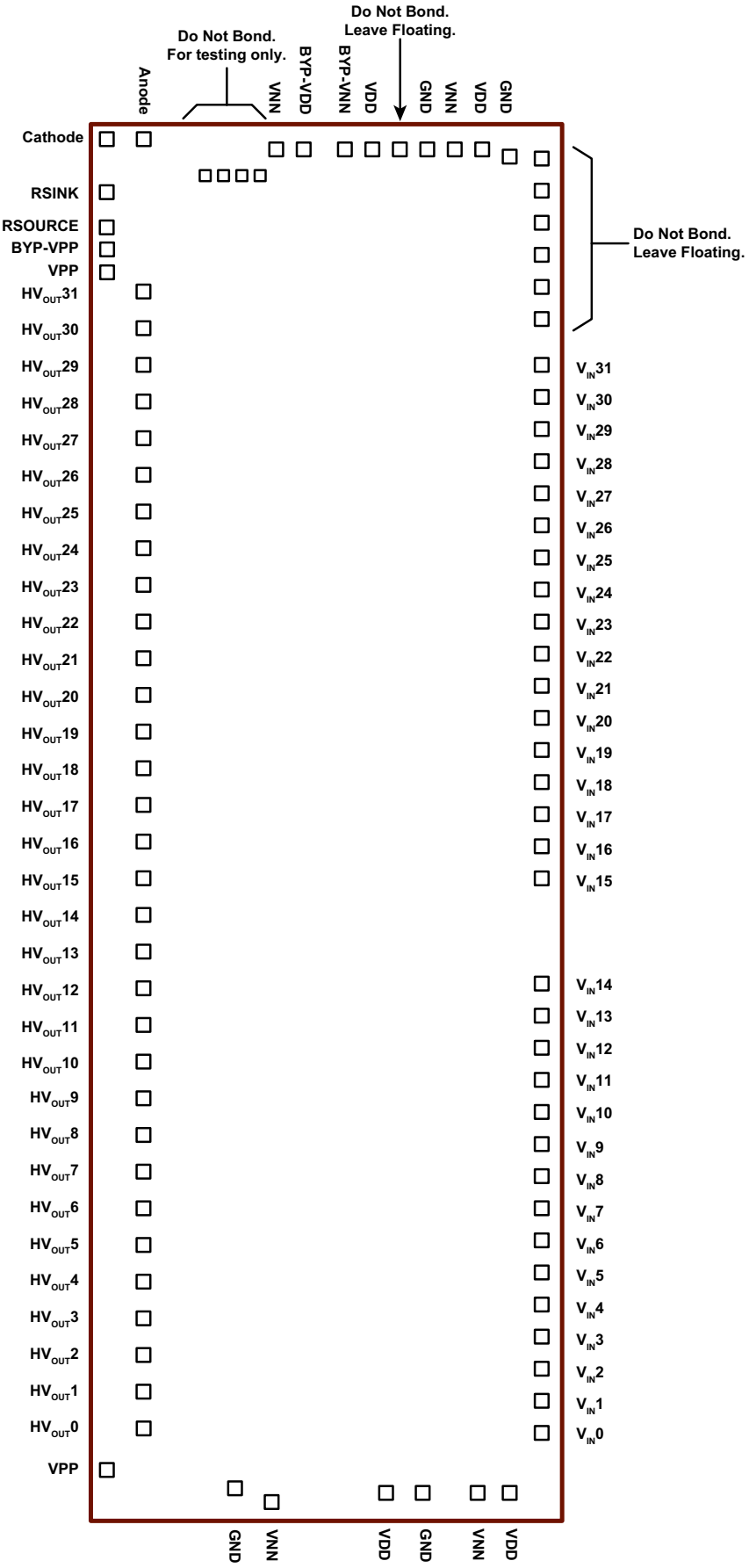


Gain vs V_{IN}

(V_{PP} = 300V, V_{DD} = 6.5V, V_{NN} = 5.5V, T_A = -10°, +25°, +85°C)



Pad Configuration *(not drawn to scale)*



Pad Coordinates

Chip size: 17160µm x 5830µm
Center of die is (0,0)

Pad Name	X (µm)	Y (µm)
VPP	-8338.5	2708.5
$HV_{OUT}0$	-7895.0	2305.5
$HV_{OUT}1$	7448.5	2305.5
$HV_{OUT}2$	-7001.5	2305.5
$HV_{OUT}3$	-6554.5	2305.5
$HV_{OUT}4$	-6107.5	2305.5
$HV_{OUT}5$	-5660.5	2305.5
$HV_{OUT}6$	-5213.5	2305.5
$HV_{OUT}7$	-4776.5	2305.5
$HV_{OUT}8$	-4319.5	2305.5
$HV_{OUT}9$	-3872.5	2305.5
$HV_{OUT}10$	-3425.5	2305.5
$HV_{OUT}11$	-2978.5	2305.5
$HV_{OUT}12$	-2513.5	2305.5
$HV_{OUT}13$	-2084.5	2305.5
$HV_{OUT}14$	-1637.5	2305.5
$HV_{OUT}15$	-1190.5	2305.5
$HV_{OUT}16$	-743.5	2305.5
$HV_{OUT}17$	-296.5	2305.5
$HV_{OUT}18$	150.0	2305.5
$HV_{OUT}19$	597.5	2305.5
$HV_{OUT}20$	1044.5	2305.5
$HV_{OUT}21$	1491.5	2305.5
$HV_{OUT}22$	1938.5	2305.5
$HV_{OUT}23$	2385.5	2305.5
$HV_{OUT}24$	2832.5	2305.5
$HV_{OUT}25$	3279.5	2305.5
$HV_{OUT}26$	3726.5	2305.5
$HV_{OUT}27$	4173.5	2305.5
$HV_{OUT}28$	4620.5	2305.5

Pad Name	X (µm)	Y (µm)
$HV_{OUT}29$	5067.5	2305.5
$HV_{OUT}30$	5514.5	2305.5
$HV_{OUT}31$	5961.5	2305.5
VPP	6659.0	2709.0
BYP-VPP	7045.0	2709.0
RSOURCE	7489.0	2709.0
RSINK	7969.0	2709.0
CATHODE	8366.0	2709.0
ANODE	8366.0	2709.0
VNN	8047.0	425.0
BYP-VDD	8047.0	125.5
BYP-VNN	8047.0	-135.5
VDD	8047.0	-704.5
GND	8047.0	-1424.0
VNN	8066.5	-1590.0
VDD	8066.5	-1958.5
GND	7867.0	-2192.0
$V_{IN}31$	5043.5	-2686.0
$V_{IN}30$	4638.5	-2686.0
$V_{IN}29$	4233.5	-2686.0
$V_{IN}28$	3828.5	-2686.0
$V_{IN}27$	3423.5	-2686.0
$V_{IN}26$	3018.5	-2686.0
$V_{IN}25$	2613.5	-2686.0
$V_{IN}24$	2208.5	-2686.0
$V_{IN}23$	1803.5	-2686.0
$V_{IN}22$	1398.5	-2686.0
$V_{IN}21$	993.5	-2686.0
$V_{IN}20$	588.5	-2686.0
$V_{IN}19$	183.5	-2686.0

Pad Name	X (µm)	Y (µm)
$V_{IN}18$	-221.5	-2686.0
$V_{IN}17$	-626.5	-2686.0
$V_{IN}16$	-1031.5	-2686.0
$V_{IN}15$	-1436.5	-2686.0
$V_{IN}14$	-2412.5	-2686.0
$V_{IN}13$	-2817.0	-2686.0
$V_{IN}12$	-3222.0	-2686.0
$V_{IN}11$	-3627.0	-2686.0
$V_{IN}10$	-4032.0	-2686.0
$V_{IN}9$	-4437.0	-2686.0
$V_{IN}8$	-4842.0	-2686.0
$V_{IN}7$	-5247.0	-2686.0
$V_{IN}6$	-5652.0	-2686.0
$V_{IN}5$	-6052.0	-2686.0
$V_{IN}4$	-6462.0	-2686.0
$V_{IN}3$	-6867.0	-2686.0
$V_{IN}2$	-7272.0	-2686.0
$V_{IN}1$	-7677.0	-2686.0
$V_{IN}0$	-8082.0	-2686.0
VDD	-8373.0	-2250.5
VNN	-8373.0	-1949.0
GND	-8367.0	-1561.0
VDD	-8387.0	-1143.0
VNN	-8338.5	577.5
GND	-8341.0	916.5

Pin Description

Pin #	Function	Description
1	$HV_{OUT}31$	Amplifier outputs.
2	$HV_{OUT}30$	
3	$HV_{OUT}29$	
4	$HV_{OUT}28$	
5	$HV_{OUT}27$	
6	$HV_{OUT}26$	
7	$HV_{OUT}25$	
8	$HV_{OUT}24$	
9	$HV_{OUT}23$	
10	$HV_{OUT}22$	
11	$HV_{OUT}21$	
12	$HV_{OUT}20$	
13	$HV_{OUT}19$	
14	$HV_{OUT}18$	
15	$HV_{OUT}17$	
16	$HV_{OUT}16$	
17	$HV_{OUT}15$	
18	$HV_{OUT}14$	
19	$HV_{OUT}13$	
20	$HV_{OUT}12$	
21	$HV_{OUT}11$	
22	$HV_{OUT}10$	
23	$HV_{OUT}9$	
24	$HV_{OUT}8$	
25	$HV_{OUT}7$	
26	$HV_{OUT}6$	
27	$HV_{OUT}5$	
28	$HV_{OUT}4$	
29	$HV_{OUT}3$	
30	$HV_{OUT}2$	
31	$HV_{OUT}1$	
32	$HV_{OUT}0$	
33	VPP	High voltage positive supply. There are two pads.
34-38	NC	No connect.
39	GND	Digital ground. There are four pads.

Pin Description *(cont.)*

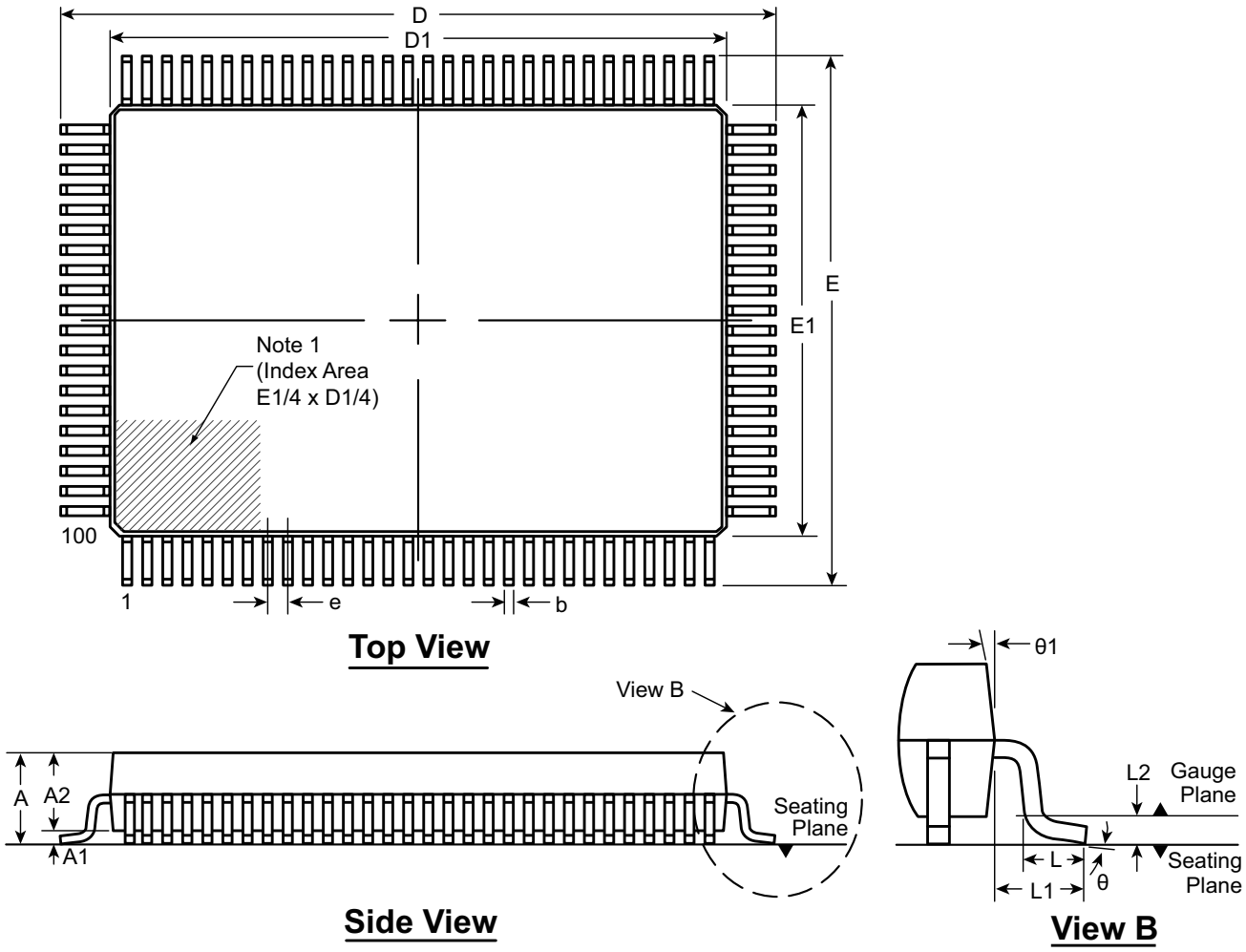
Pin #	Function	Description
40	VNN	Analog low voltage negative supply. There are four pads.
41	NC	No connect.
42	VDD	Analog low voltage positive supply. There are four pads.
43	GND	Digital ground. There are four pads.
44	VNN	Analog low voltage negative supply. There are four pads.
45	VDD	Analog low voltage positive supply. There are four pads.
46-47	NC	No connect.
48	$V_{IN}0$	Amplifier inputs.
49	$V_{IN}1$	
50	$V_{IN}2$	
51	$V_{IN}3$	
52	$V_{IN}4$	
53	$V_{IN}5$	
54	$V_{IN}6$	
55	$V_{IN}7$	
56	$V_{IN}8$	
57	$V_{IN}9$	
58	$V_{IN}10$	
59	$V_{IN}11$	
60	$V_{IN}12$	
61	$V_{IN}13$	
62	$V_{IN}14$	
63	$V_{IN}15$	
64	$V_{IN}16$	
65	$V_{IN}17$	
66	$V_{IN}18$	
67	$V_{IN}19$	
68	$V_{IN}20$	

Pin Description *(cont.)*

Pin #	Function	Description
69	$V_{IN}21$	Amplifier inputs.
70	$V_{IN}22$	
71	$V_{IN}23$	
72	$V_{IN}24$	
73	$V_{IN}25$	
74	$V_{IN}26$	
75	$V_{IN}27$	
76	$V_{IN}28$	
77	$V_{IN}29$	
78	$V_{IN}30$	
79	$V_{IN}31$	
80-85	NC	No connect.
86	GND	Digital ground. There are four pads.
87	VDD	Analog low voltage positive supply. There are four pads.
88	VNN	Analog low voltage negative supply. There are four pads.
89	GND	Digital ground. There are four pads.
90	NC	No connect.
91	VDD	Analog low voltage positive supply. There are four pads.
92	BYP-VNN	A low voltage 1.0 to 10nF decoupling decoupling capacitor across VNN and BYP-VNN is required.
93	BYP-VDD	A low voltage 1.0 to 10nF decoupling decoupling capacitor across VDD and BYP-VDD is required.
94	VNN	Analog low voltage negative supply. There are four pads.
95	ANODE	Anode side of of a low voltage silicon diode that can be used to monitor die temperature.
96	CATHODE	Cathode side of of a low voltage silicon diode that can be used to monitor die temperature.
97	RSINK	External resistor from RSINK to VNN sets output current sinking limit. Current limit is approximately 12.5V divided by RSINK resistor value.
98	RSOURCE	External resistor from RSOURCE to VNN sets output current sourcing limit. Current limit is approximately 12.5V divided by RSOURCE resistor value.
99	BYP-VPP	A low voltage 1.0 to 10nF decoupling decoupling capacitor across VPP and BYP-VPP is required.
100	VPP	High voltage positive supply. There are two pads.

100-Lead MQFP Package Outline (FG)

20.00x14.00mm body, 3.15mm height (max), 0.65mm pitch, 3.20mm footprint



Note:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	θ	θ1
Dimension (mm)	MIN	2.50*	0.00	2.50	0.22	22.95*	19.80*	16.95*	13.80*	0.65 BSC	0.73	1.60 REF	0.25 BSC	0°	5°
	NOM	-	-	2.70	-	23.20	20.00	17.20	14.00		0.88			-	-
	MAX	3.15	0.25	2.90	0.40	23.45*	20.20*	17.45*	14.20*		1.03			7°	16°

JEDEC Registration MS-022, Variation GC-2, Issue B, Dec. 1996.
** This dimension is not specified in the JEDEC drawing.*
Drawings are not to scale.
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