OptiMOS(TM)3 Power-Transistor

Features

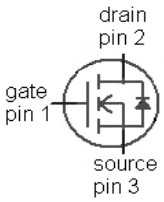
- Ideal for high frequency switching and sync. rec.
- Optimized technology for DC/DC converters
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- N-channel, normal level
- 100% avalanche tested
- Pb-free plating; RoHS compliant
- Qualified according to JEDEC[1] for target applications

RoHS

Product Summary

V_{DS}	80	V
$R_{DS(on),max}$	10.3	mΩ
I_D	50	A

Type	IPU103N08N3 G
	
Package	PG-TO251-3
Marking	103N08N



Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	T_C=25 °C[2]	50	A
		T_C=100 °C	50	
Pulsed drain current[2]	$I_{D,pulse}$	T_C=25 °C	200	
Avalanche energy, single pulse[3]	E_{AS}	I_D=46 A, R_{GS}=25 Ω	90	mJ
Gate source voltage	V_{GS}		±20	V
Power dissipation	P_{tot}	T_C=25 °C	100	W
Operating and storage temperature	T_j, T_{stg}		-55 ... 175	°C
IEC climatic category; DIN IEC 68-1			55/175/56	

[1] J-STD20 and JESD22
[2] See figure 3 for more detailed information
[3] See figure 13 for more detailed information

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics						
Thermal resistance, junction - case	R_{thJC}		-	-	1.5	K/W
Thermal resistance, junction - ambient	R_{thJA}	minimal footprint	-	-	75	
		6 cm^2 cooling area[4)]	-	-	50	
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=1 mA	80	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=46 µA	2	2.8	3.5	
Zero gate voltage drain current	I_{DSS}	V_{DS}=80 V, V_{GS}=0 V, T_j=25 °C	-	0.1	1	µA
		V_{DS}=80 V, V_{GS}=0 V, T_j=125 °C	-	10	100	
Gate-source leakage current	I_{GSS}	V_{GS}=20 V, V_{DS}=0 V	-	1	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=10 V, I_D=46 A	-	8.7	10.3	mΩ
		V_{GS}=6 V, I_D=23 A	-	11.5	18.5	
Gate resistance	R_G		-	1.6	-	Ω
Transconductance	g_{fs}	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=46 A	29	57	-	S

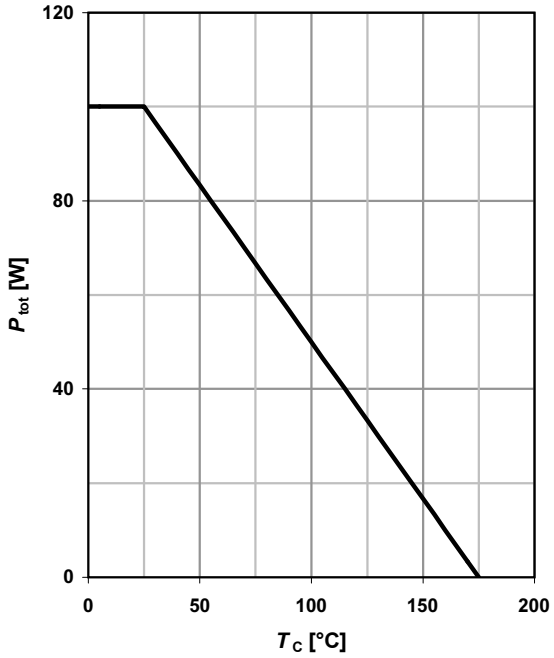
[4)] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=40 V, f=1 MHz	-	1810	2410	pF
Output capacitance	C_{oss}		-	490	652	
Reverse transfer capacitance	C_{rss}		-	20	-	
Turn-on delay time	$t_{d(on)}$	V_{DD}=40 V, V_{GS}=10 V, I_D=46 A, R_G=1.6 Ω	-	13	-	ns
Rise time	t_r		-	21	-	
Turn-off delay time	$t_{d(off)}$		-	22	-	
Fall time	t_f		-	5	-	
Gate Charge Characteristics[5)]						
Gate to source charge	Q_{gs}	V_{DD}=40 V, I_D=46 A, V_{GS}=0 to 10 V	-	10	-	nC
Gate to drain charge	Q_{gd}		-	5	-	
Switching charge	Q_{sw}		-	10	-	
Gate charge total	Q_g		-	26	35	
Gate plateau voltage	$V_{plateau}$		-	5.3	-	V
Output charge	Q_{oss}	V_{DD}=40 V, V_{GS}=0 V	-	35	47	nC
Reverse Diode						
Diode continous forward current	I_S	T_C=25 °C	-	-	50	A
Diode pulse current	$I_{S,pulse}$		-	-	200	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=46 A, T_j=25 °C	-	1.0	1.2	V
Reverse recovery time	t_{rr}	V_R=40 V, I_F=46A, di_F/dt=100 A/µs	-	53	-	ns
Reverse recovery charge	Q_{rr}		-	78	-	nC

[5)] See figure 16 for gate charge parameter definition

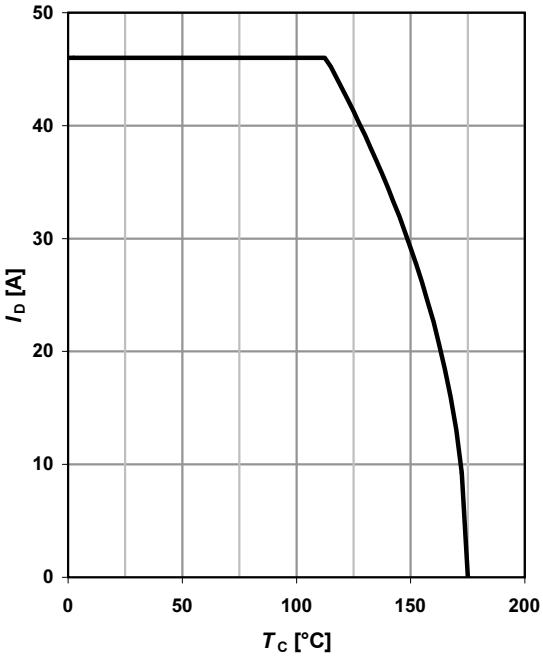
1 Power dissipation

$P_{tot}=f(T_C)$



2 Drain current

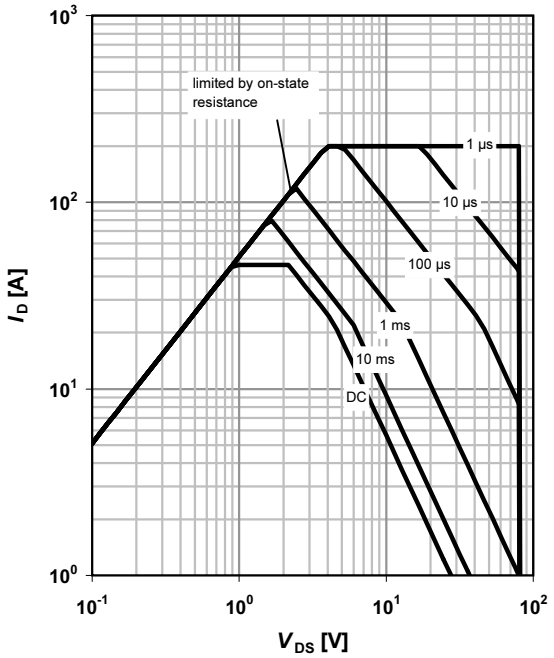
$I_D=f(T_C)$; $V_{GS}\geq 10$ V



3 Safe operating area

$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$

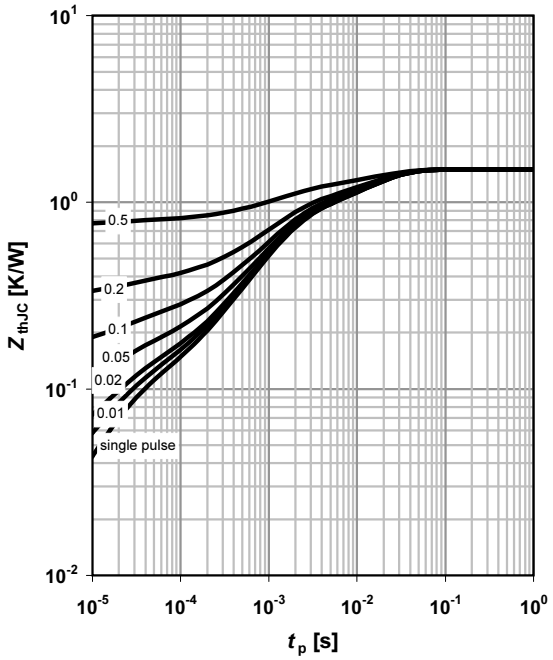
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC}=f(t_p)$

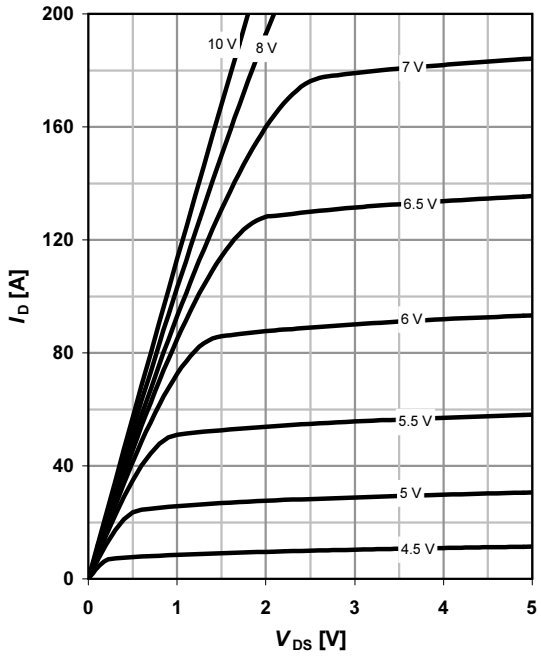
parameter: $D=t_p/T$



5 Typ. output characteristics

$I_D=f(V_{DS})$; $T_j=25$ °C

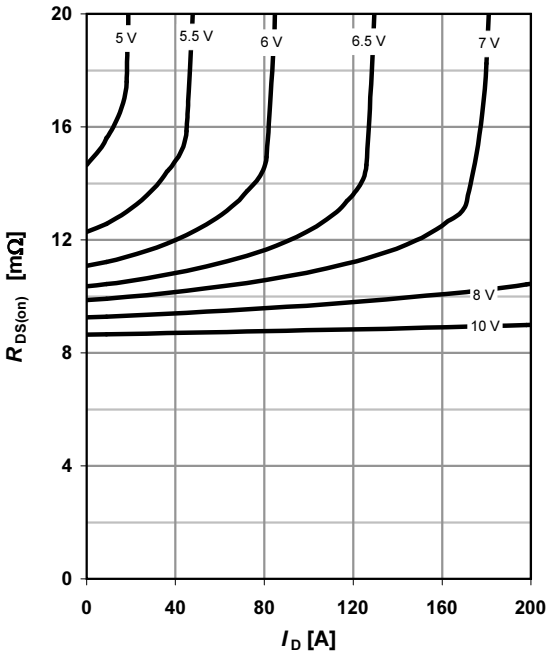
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)}=f(I_D)$; $T_j=25$ °C

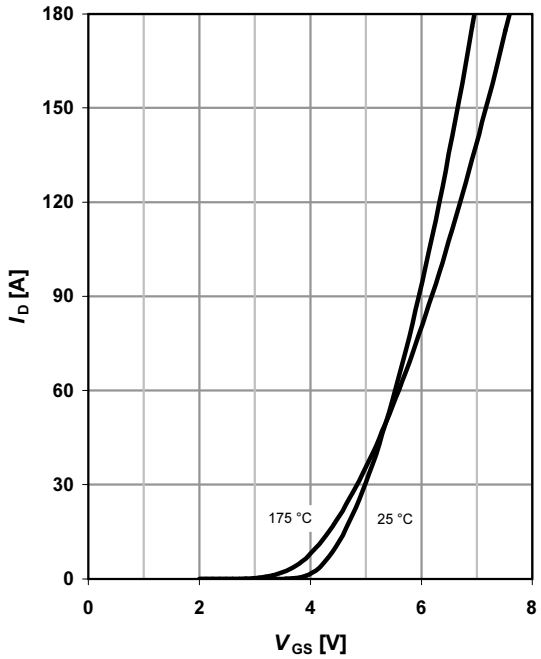
parameter: V_{GS}



7 Typ. transfer characteristics

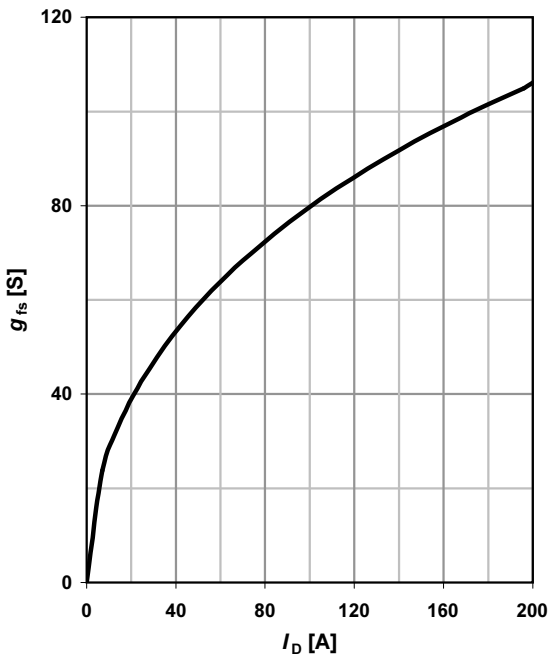
$I_D=f(V_{GS})$; $|V_{DS}|>2|I_D|R_{DS(on)max}$

parameter: T_j



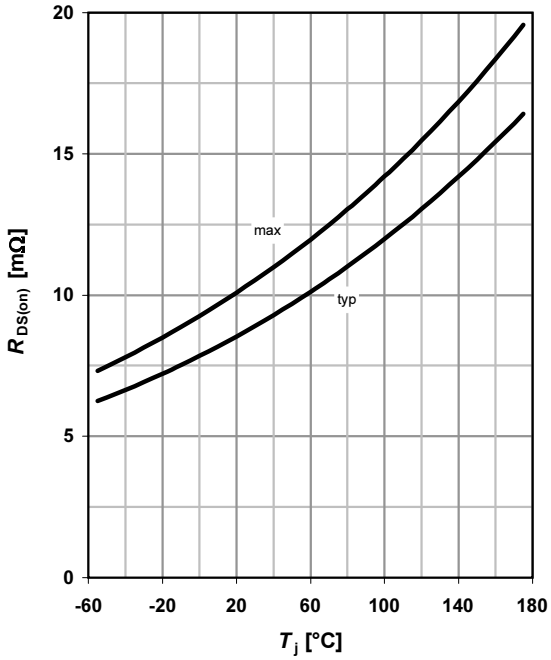
8 Typ. forward transconductance

$g_{fs}=f(I_D)$; $T_j=25$ °C



9 Drain-source on-state resistance

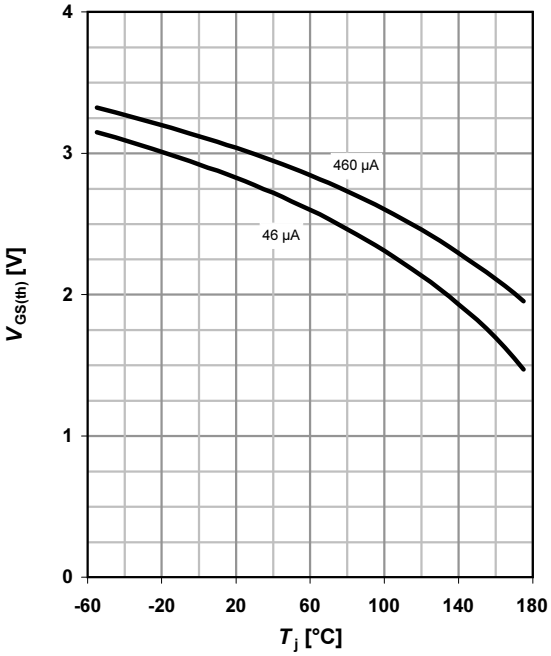
$R_{DS(on)}=f(T_j)$; $I_D=46$ A; $V_{GS}=10$ V



10 Typ. gate threshold voltage

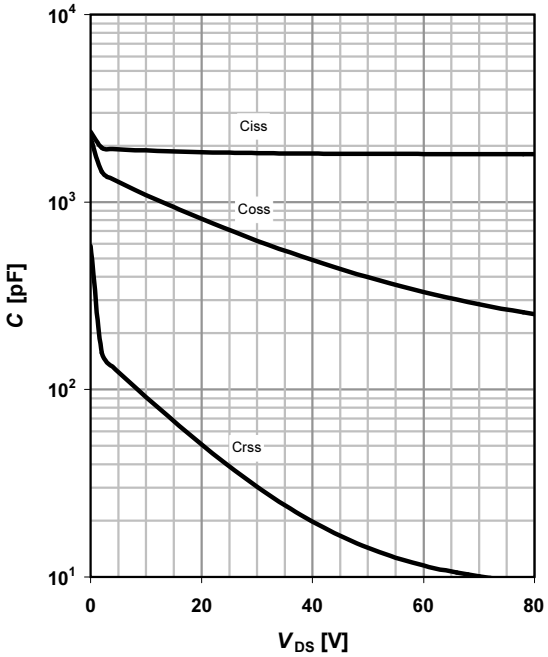
$V_{GS(th)}=f(T_j)$; $V_{GS}=V_{DS}$

parameter: I_D



11 Typ. capacitances

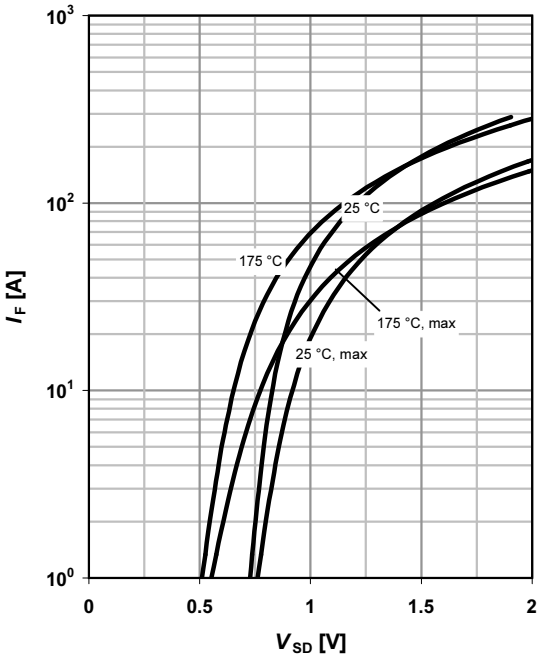
$C=f(V_{DS})$; $V_{GS}=0$ V; $f=1$ MHz



12 Forward characteristics of reverse diode

$I_F=f(V_{SD})$

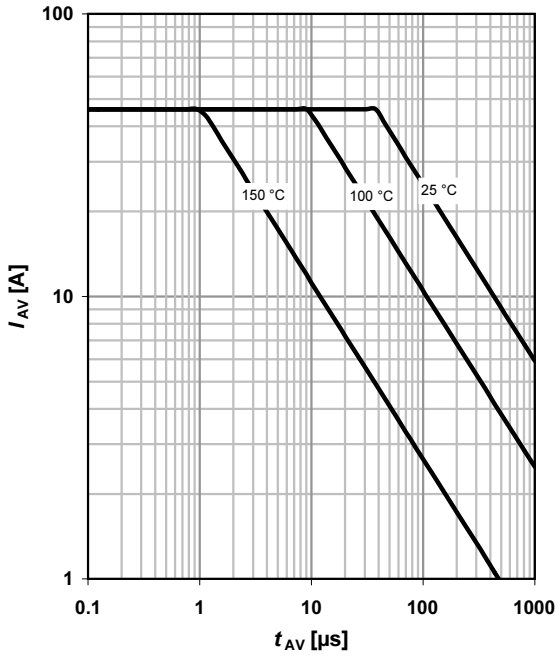
parameter: T_j



13 Avalanche characteristics

I_{AS}=f(t_{AV}); R_{GS}=25 Ω

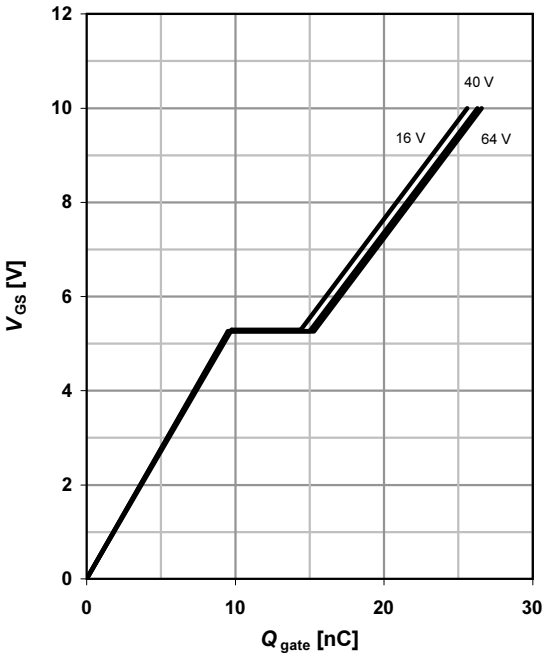
parameter: $T_{j(start)}$



14 Typ. gate charge

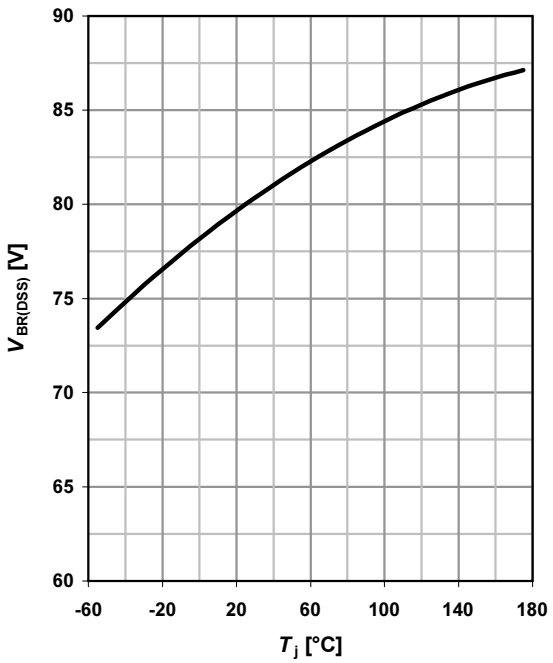
V_{GS}=f(Q_{gate}); I_D=46 A pulsed

parameter: V_{DD}

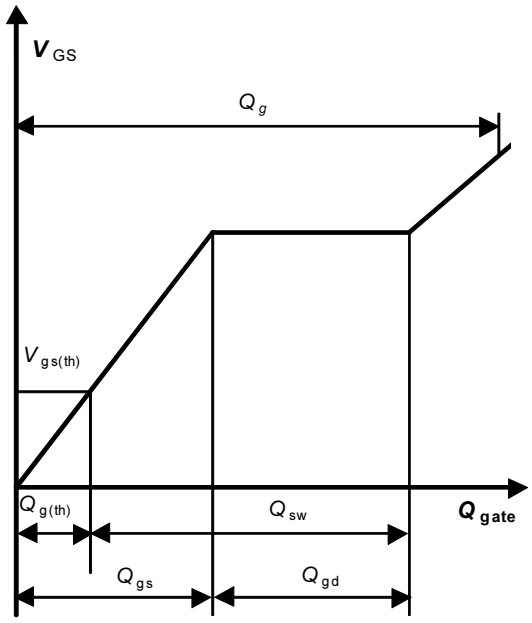


15 Drain-source breakdown voltage

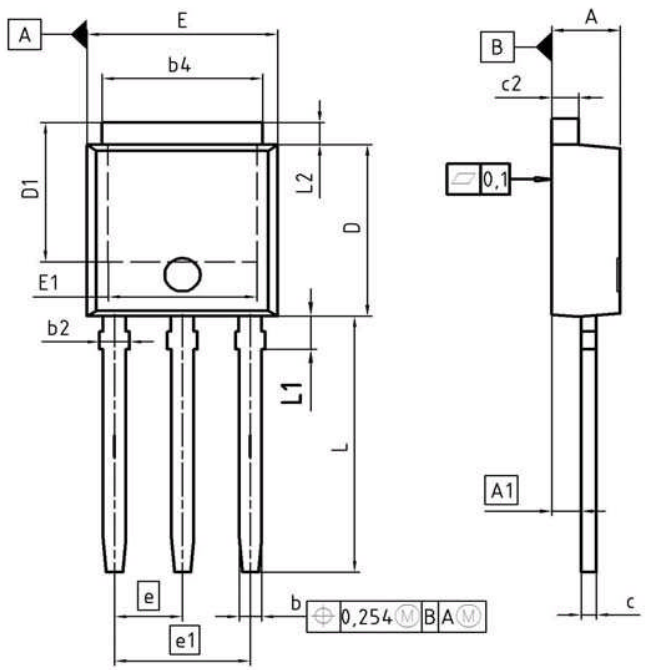
$V_{BR(DSS)}$=f(T_j); I_D=1 mA



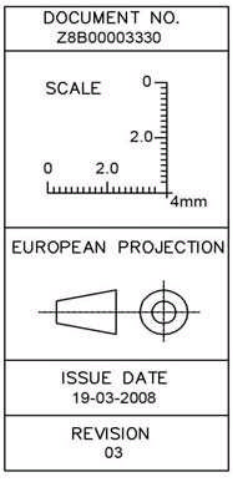
16 Gate charge waveforms



PG-TO251-3: Outline



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.16	2.41	0.085	0.095
A1	0.90	1.14	0.035	0.045
b	0.64	0.89	0.025	0.035
b2	0.65	1.15	0.026	0.045
b4	4.95	5.50	0.195	0.217
c	0.46	0.60	0.018	0.024
c2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	5.04	5.77	0.198	0.227
E	6.35	6.73	0.250	0.265
E1	4.70	5.21	0.185	0.205
e	2.29		0.090	
e1	4.57		0.180	
N	3		3	
L	8.89	9.65	0.350	0.380
L1	1.90	2.29	0.075	0.090
L2	0.89	1.37	0.035	0.054



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