

N-channel 600 V, 0.108 Ω typ., 26 A MDmesh II Plus™ low Q_g Power MOSFETs in TO-220FP, I²PAK, TO-220 and TO-247 packages

Datasheet - production data

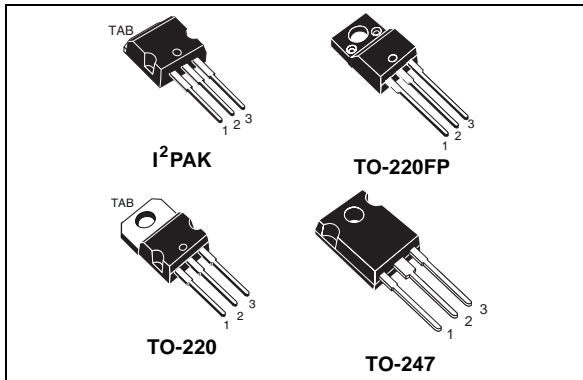
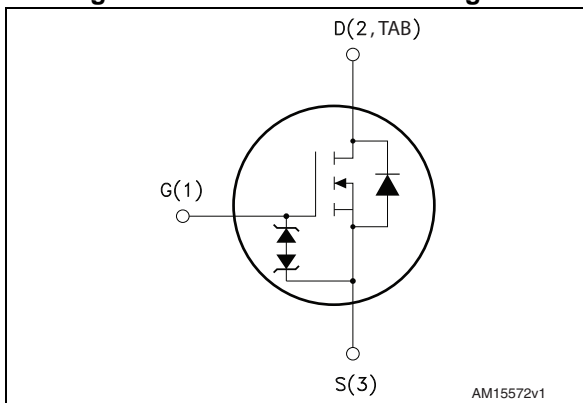


Figure 1. Internal schematic diagram



Features

Order codes	$V_{DS} @ T_{Jmax}$	$R_{DS(on) max}$	I_D
STF33N60M2	650 V	0.125 Ω	26 A ⁽¹⁾
STI33N60M2			26 A
STP33N60M2			
STW33N60M2			

1. Limited by maximum junction temperature.

- Extremely low gate charge
- Lower $R_{DS(on)}$ x area vs previous generation
- MDmesh™ II technology
- Low gate input resistance
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications
- LCC converters, resonant converters

Description

These devices are N-channel Power MOSFETs developed using a new generation of MDmesh™ technology: MDmesh II Plus™ low Q_g . These revolutionary Power MOSFETs associate a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. They are therefore suitable for the most demanding high efficiency converters.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STF33N60M2	33N60M2	TO-220FP	Tube
STI33N60M2		I ² PAK	
STP33N60M2		TO-220	
STW33N60M2		TO-247	

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		I ² PAK, TO-220 TO-247	TO-220FP	
V _{GS}	Gate-source voltage	± 25		V
I _D	Drain current (continuous) at T _C = 25 °C	26	26 ⁽¹⁾	A
I _D	Drain current (continuous) at T _C = 100 °C	16	16 ⁽¹⁾	A
I _{DM} ⁽²⁾	Drain current (pulsed)	104	104 ⁽¹⁾	A
P _{TOT}	Total dissipation at T _C = 25 °C	190	35	W
dv/dt ⁽³⁾	Peak diode recovery voltage slope	15		V/ns
dv/dt ⁽⁴⁾	MOSFET dv/dt ruggedness	50		V/ns
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T _C = 25 °C)	2500		V
T _{stg}	Storage temperature	- 55 to 150		°C
T _j	Max. operating junction temperature			

- Limited by maximum junction temperature.
- Pulse width limited by safe operating area.
- I_{SD} ≤ 26 A, di/dt ≤ 400 A/μs; V_{DS peak} < V_{(BR)DSS}; V_{DD} = 400 V.
- V_{DS} ≤ 480 V

Table 3. Thermal data

Symbol	Parameter	Value			Unit
		TO-220FP	I ² PAK, TO-220	TO-247	
R _{thj-case}	Thermal resistance junction-case max	3.6	0.66		°C/W
R _{thj-amb}	Thermal resistance junction-ambient max	62.5		50	°C/W

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T _{jmax})	5	A
E _{AS}	Single pulse avalanche energy (starting T _j = 25 °C, I _D = I _{AR} ; V _{DD} = 50)	2300	mJ

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	600			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 600\text{ V}$ $V_{DS} = 600\text{ V}$, $T_C = 125\text{ °C}$			1 100	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 25\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 13\text{ A}$		0.108	0.125	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	1781	-	pF
C_{oss}	Output capacitance		-	85	-	pF
C_{riss}	Reverse transfer capacitance		-	2.5	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }480\text{ V}$, $V_{GS} = 0$	-	135	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	5.2	-	Ω
Q_g	Total gate charge	$V_{DD} = 480\text{ V}$, $I_D = 26\text{ A}$, $V_{GS} = 10\text{ V}$ (see Figure 19)	-	45.5	-	nC
Q_{gs}	Gate-source charge		-	9.9	-	nC
Q_{gd}	Gate-drain charge		-	18.5	-	nC

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_d(on)$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 13\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 18 and Figure 23)	-	16	-	ns
$t_r(v)$	Voltage rise time		-	9.6	-	ns
$t_d(off)$	Turn-off-delay time		-	109	-	ns
$t_f(i)$	Fall time		-	9	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		26	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		104	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 26 \text{ A}$, $V_{GS} = 0$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 26 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$ (see Figure 23)	-	375		ns
Q_{rr}	Reverse recovery charge		-	5.6		μC
I_{RRM}	Reverse recovery current		-	30		A
t_{rr}	Reverse recovery time	$I_{SD} = 26 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$, $T_j = 150 \text{ }^\circ\text{C}$ (see Figure 23)	-	478		ns
Q_{rr}	Reverse recovery charge		-	7.7		μC
I_{RRM}	Reverse recovery current		-	32.5		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220FP

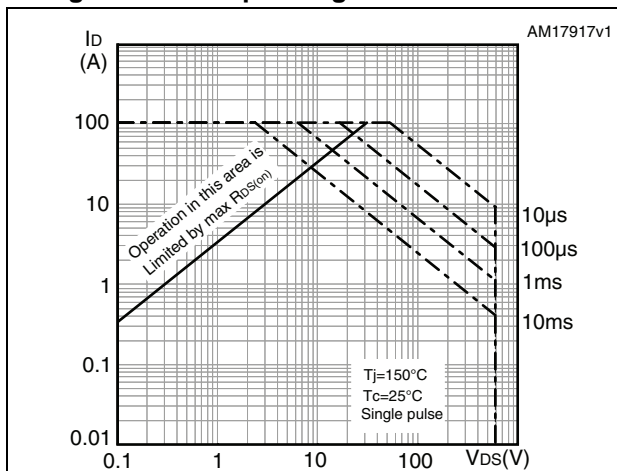


Figure 3. Thermal impedance for TO-220FP

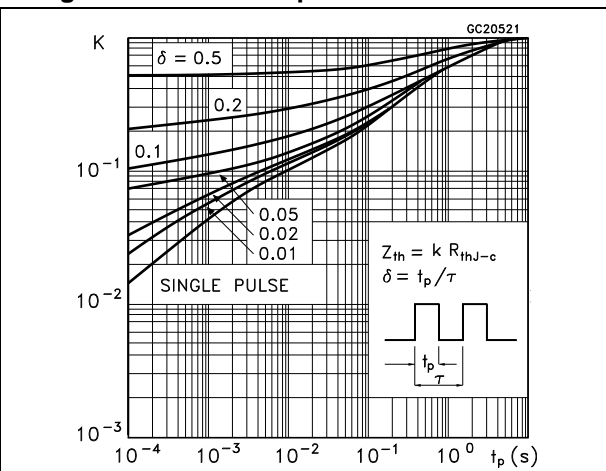


Figure 4. Safe operating area for I²PAK and TO-220

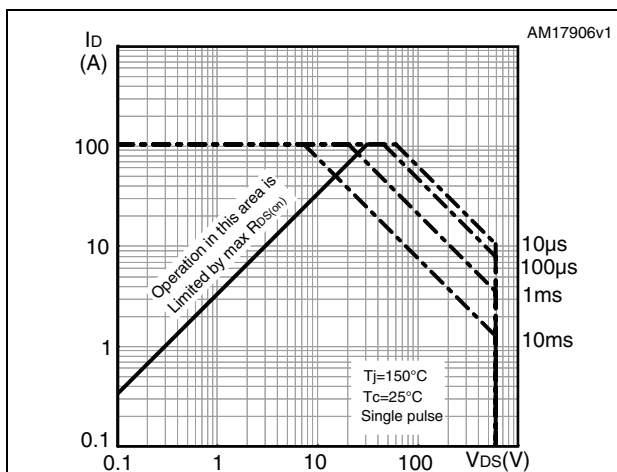


Figure 5. Thermal impedance for I²PAK and TO-220

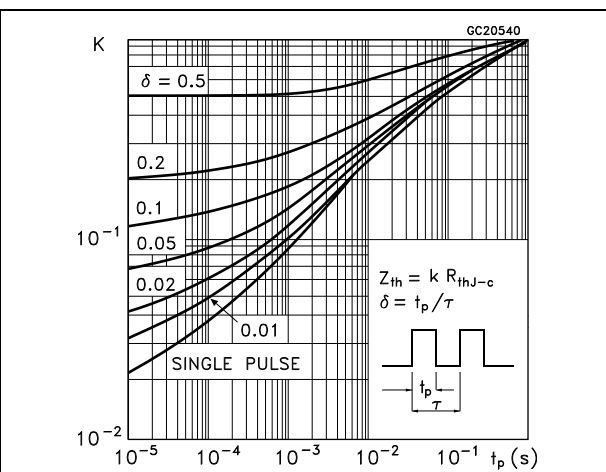


Figure 6. Safe operating area for TO-247

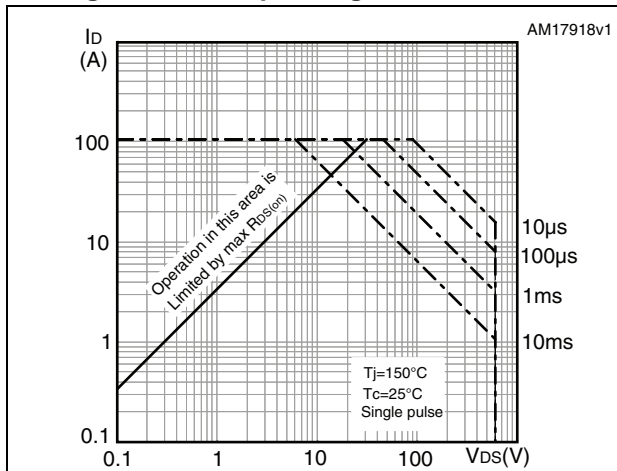


Figure 7. Thermal impedance for TO-247

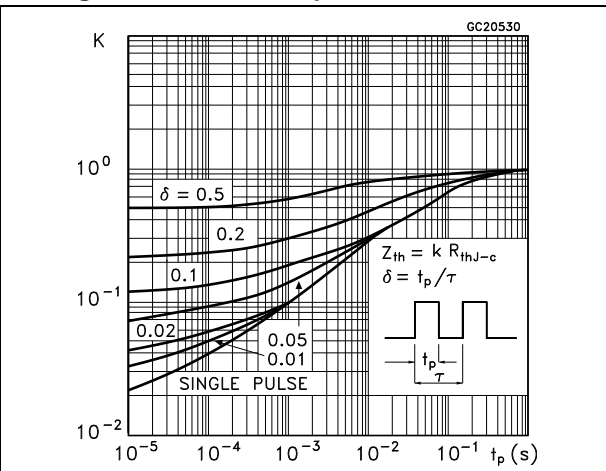


Figure 8. Output characteristics

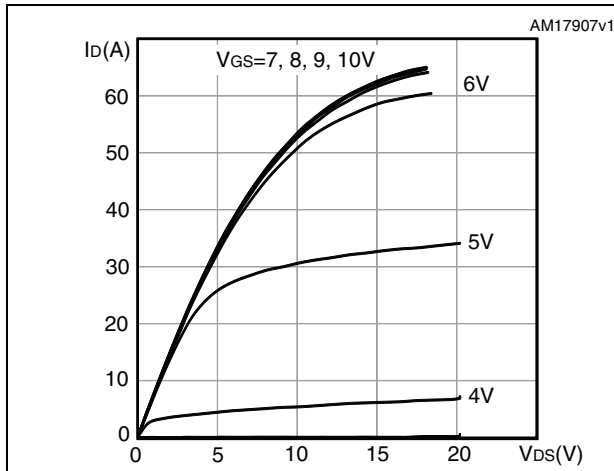


Figure 9. Transfer characteristics

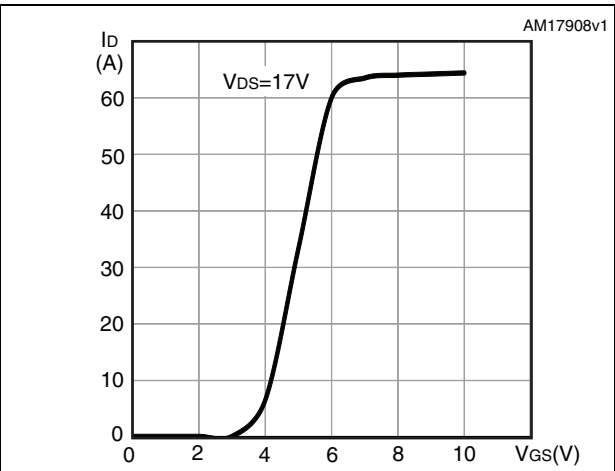


Figure 10. Gate charge vs gate-source voltage

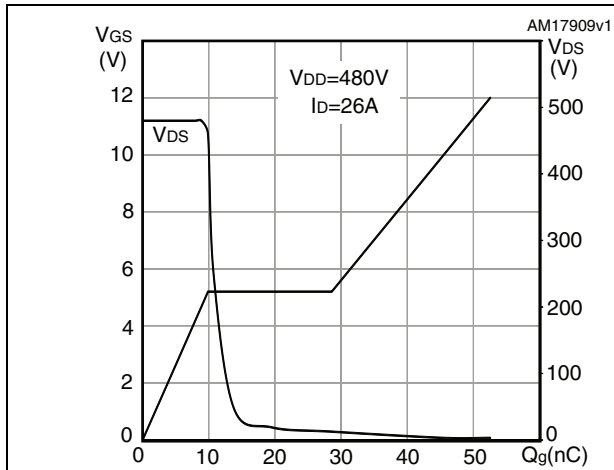


Figure 11. Static drain-source on-resistance

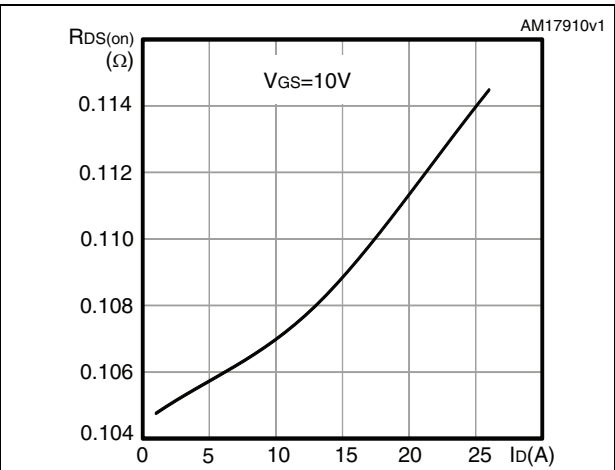


Figure 12. Capacitance variations

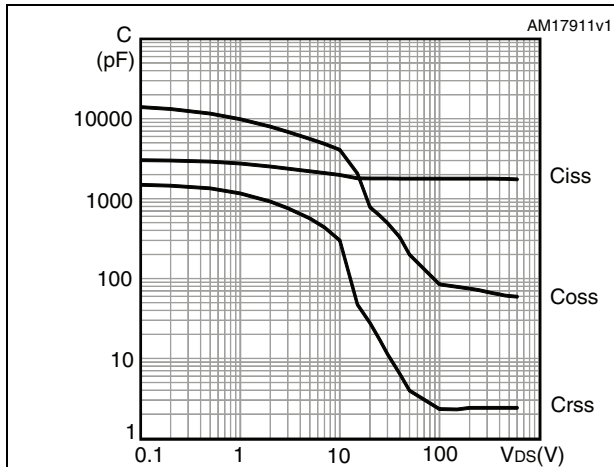


Figure 13. Output capacitance stored energy

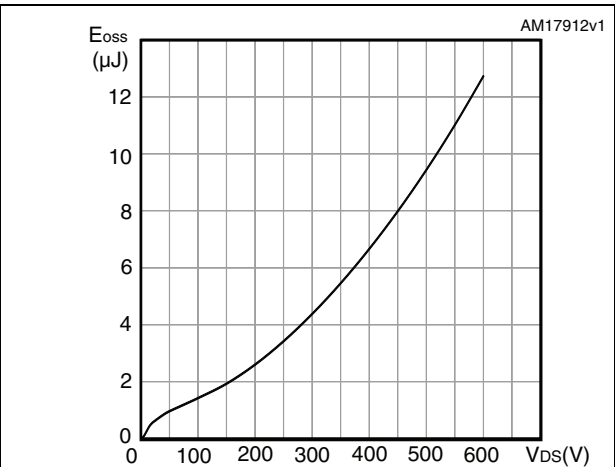


Figure 14. Normalized gate threshold voltage vs temperature

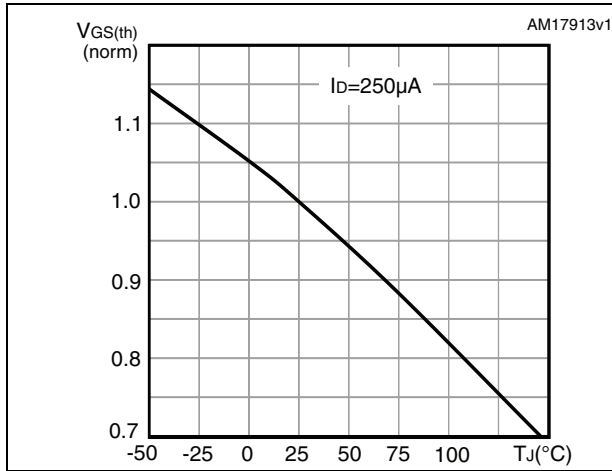


Figure 15. Normalized on-resistance vs temperature

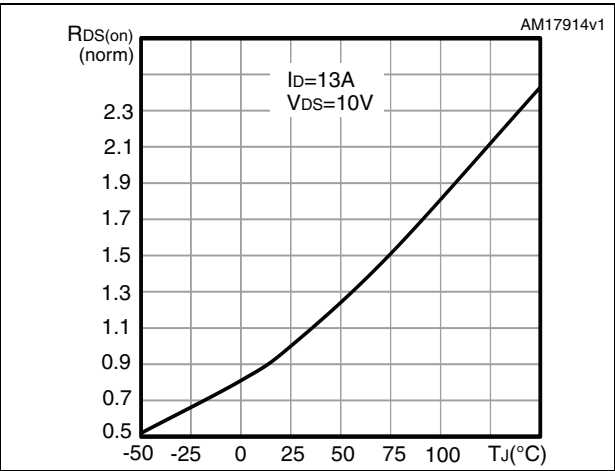


Figure 16. Normalized V_{DS} vs temperature

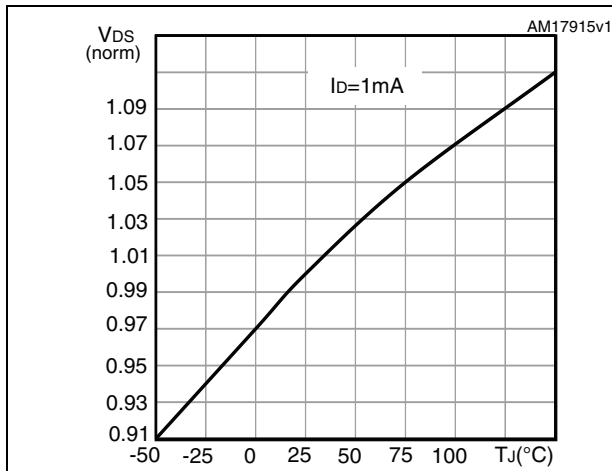
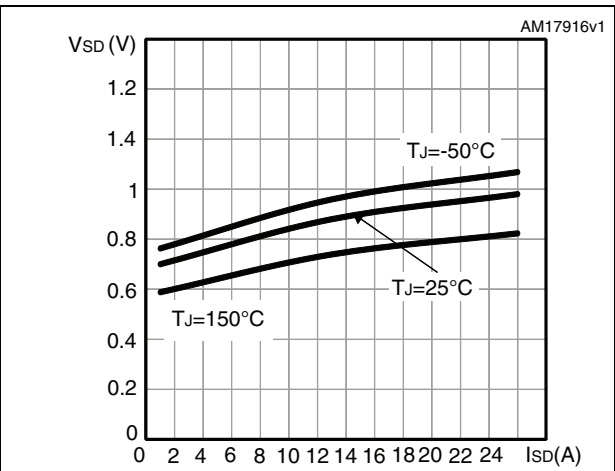


Figure 17. Source-drain diode forward characteristics



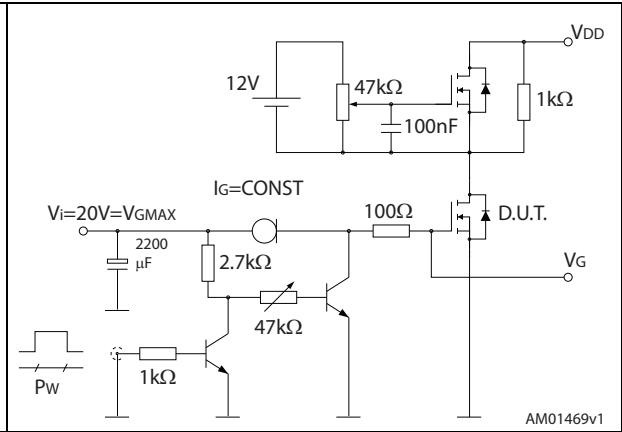
3 Test circuits

Figure 18. Switching times test circuit for resistive load



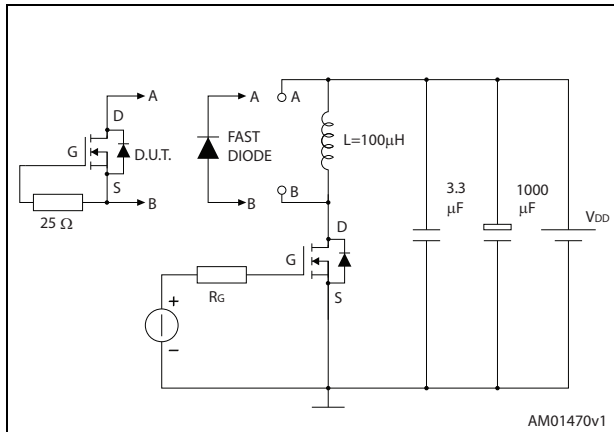
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Figure 19. Gate charge test circuit



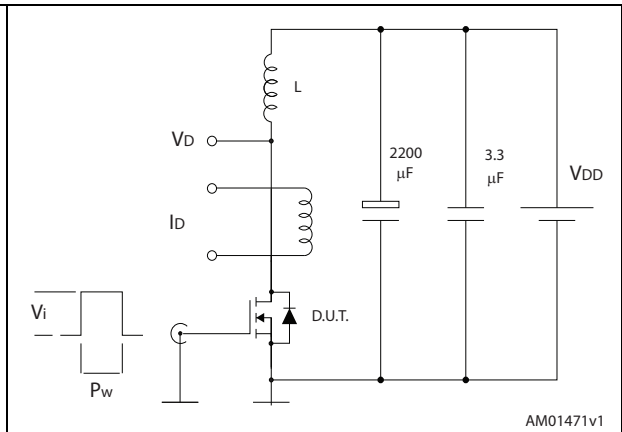
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Figure 20. Test circuit for inductive load switching and diode recovery times



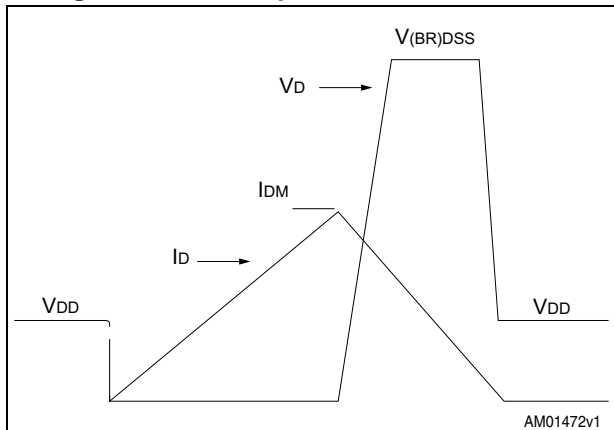
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Figure 21. Unclamped inductive load test circuit



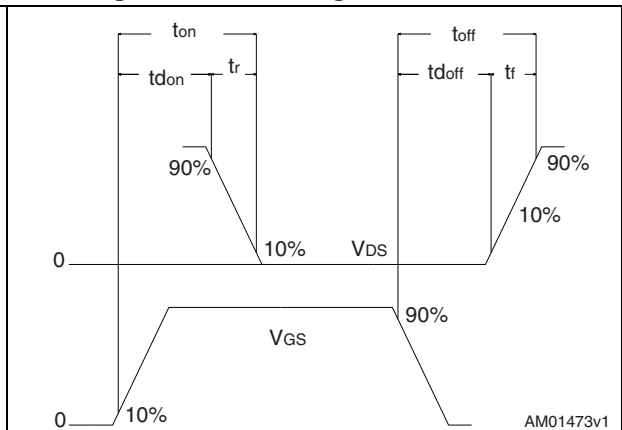
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Figure 22. Unclamped inductive waveform



AM01472v1

Figure 23. Switching time waveform



AM01473v1

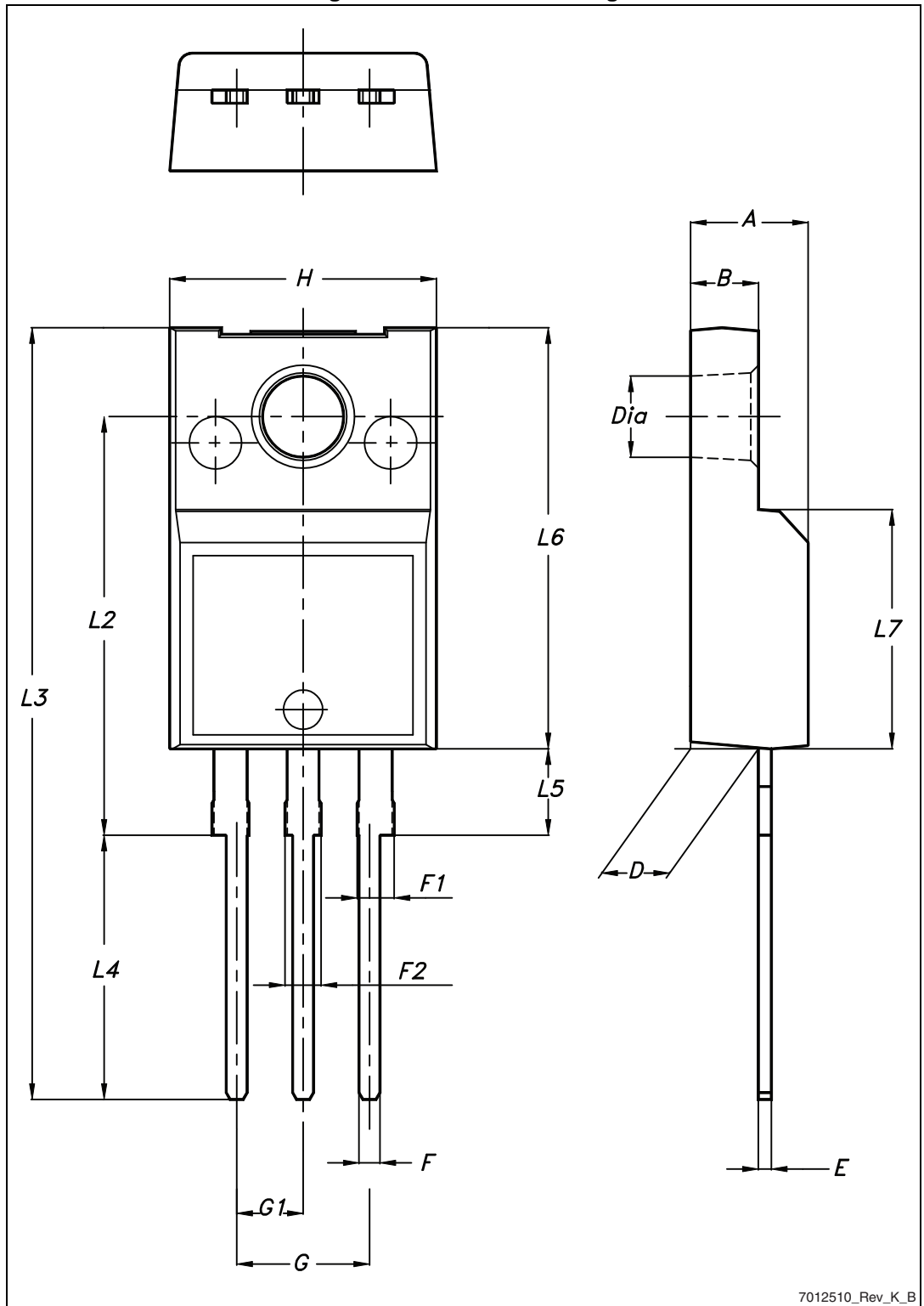
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Table 9. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 24. TO-220FP drawing



7012510_Rev_K_B

Table 10. I²PAK (TO-262) mechanical data

DIM.	mm.		
	min.	typ	max.
A	4.40		4.60
A1	2.40		2.72
b	0.61		0.88
b1	1.14		1.70
c	0.49		0.70
c2	1.23		1.32
D	8.95		9.35
e	2.40		2.70
e1	4.95		5.15
E	10		10.40
L	13		14
L1	3.50		3.93
L2	1.27		1.40

Figure 25. I²PAK (TO-262) drawing

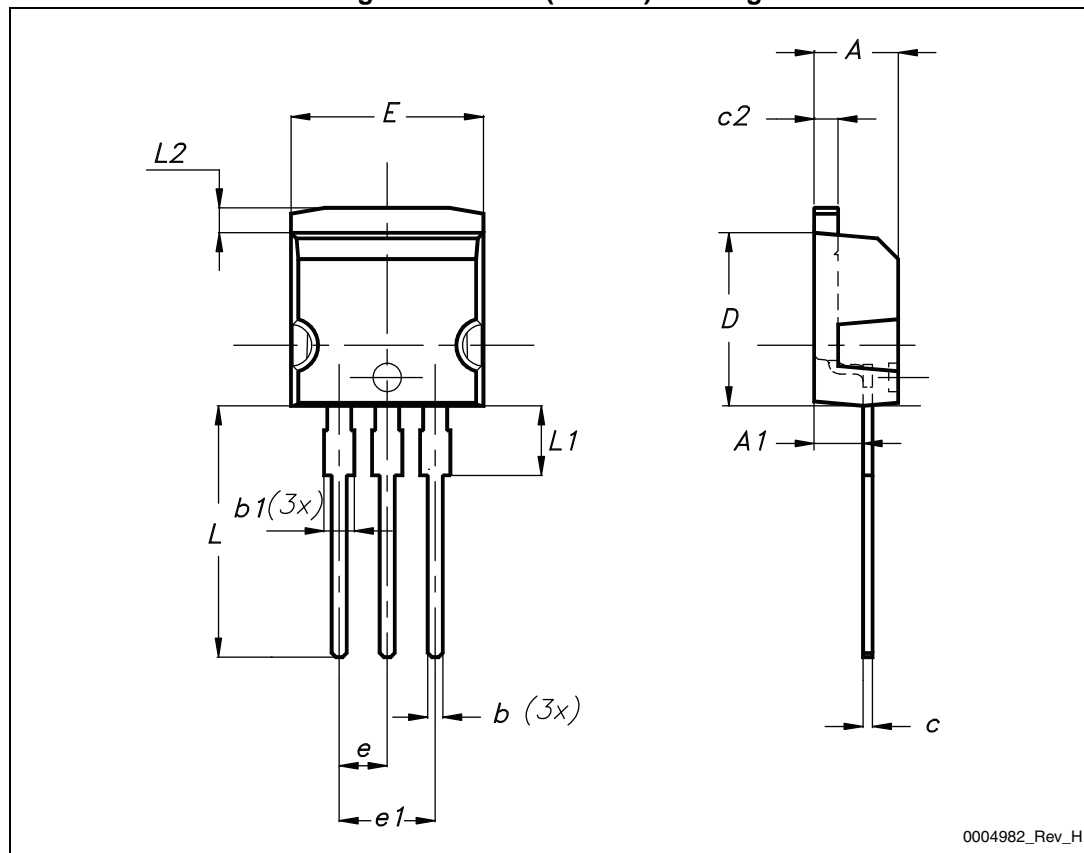


Table 11. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95

Figure 26. TO-220 type A drawing

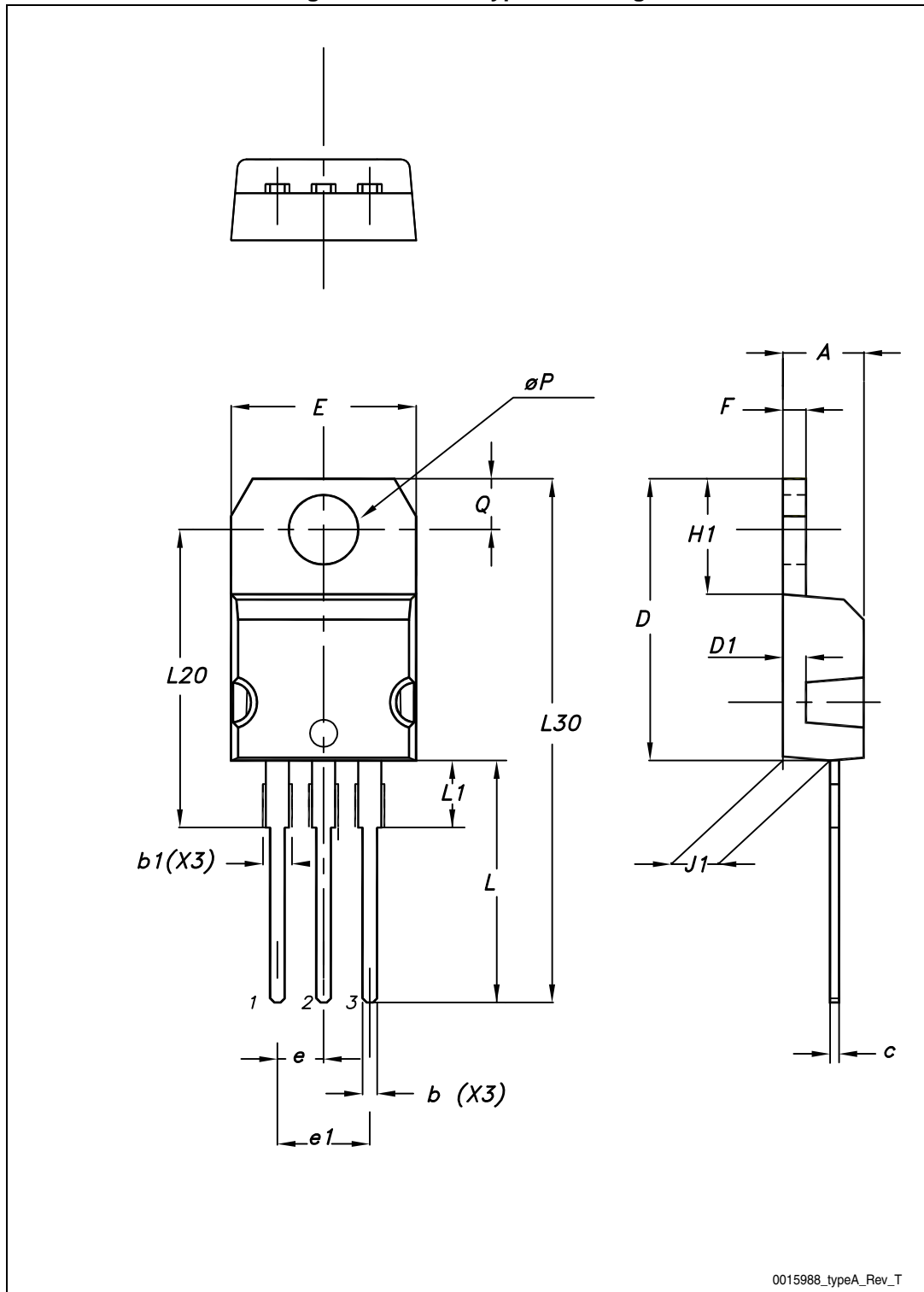
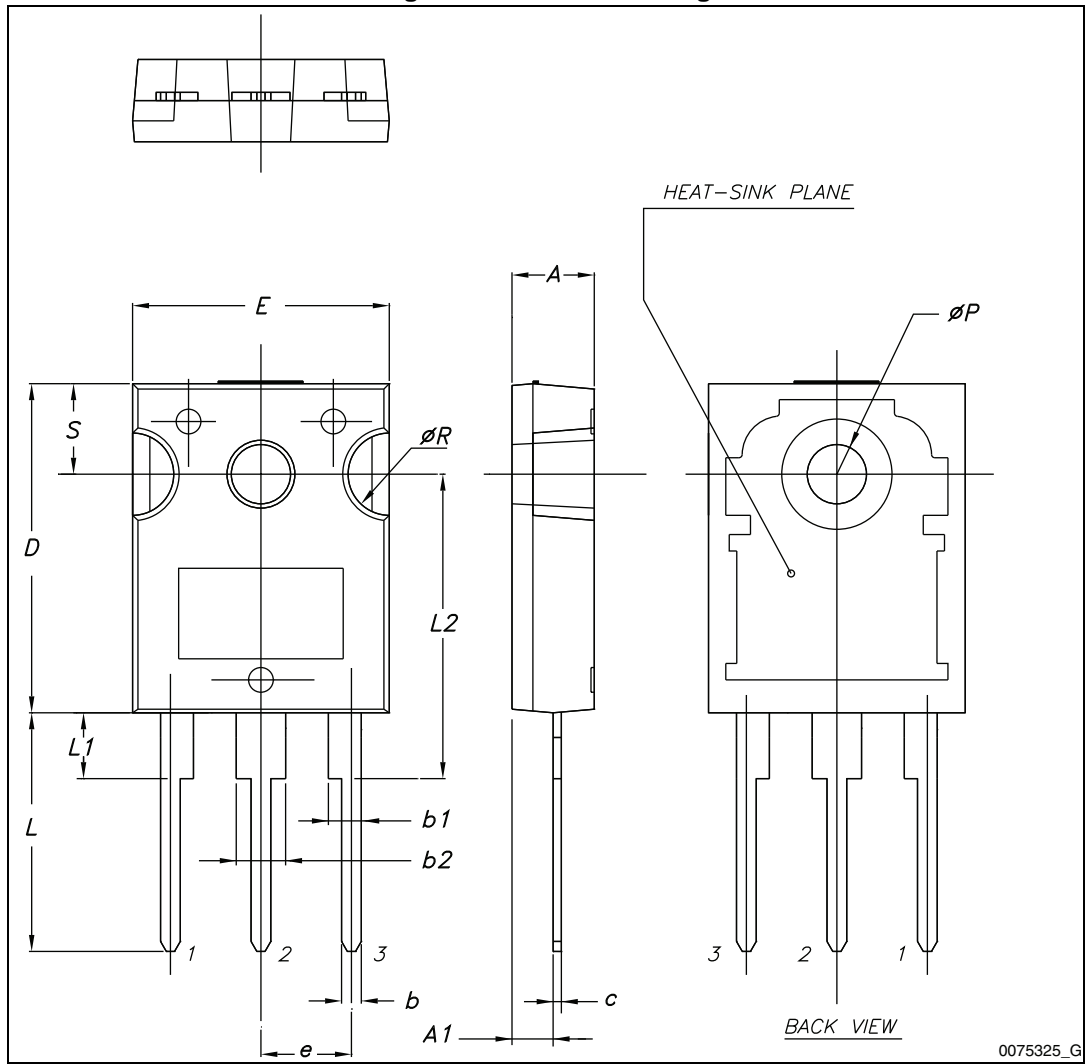


Table 12. TO-247 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

Figure 27. TO-247 drawing



5 Revision history

Table 13. Document revision history

Date	Revision	Changes
13-Sep-2013	1	First release.
19-Nov-2013	2	<ul style="list-style-type: none">– Modified: $R_{DS(on)}$ and I_D values in cover page– Modified: values in Table 4– Modified: $R_{DS(on)}$ typical and maximum values in Table 5, the entire typical values in Table 6, 7 and 8– Added: Section 2.1: Electrical characteristics (curves)– Minor text changes

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