DATA SHEET

SAA1305T
On/off logic IC

Product specification
Supersedes data of 1998 Sep 04

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Philips
Semiconductors

PHILIPS

On/off logic IC SAA1305T

FEATURES

- 8 accurate Schmitt trigger inputs with clamp circuits
- Very low quiescent current
- Reset generator circuit
- Changed information output
- On/off output to control a regulator IC which supplies the microcontroller
- 32.768 kHz RC oscillator and/or a 32.768 kHz crystal oscillator
- No delayed reset needed (start-up behaviour oscillator fixed by internal logic)
- Watchdog timer function
- Blinking LED oscillator with drive circuit for LED
- Watch function.

GENERAL DESCRIPTION

The SAA1305T is an on/off logic IC, intended for use in car radios to interface between a microcontroller and various input signals such as ignition, low supply detection, on/off key and external control signals.

The SAA1305T can replace an existing on/off logic built-up with discrete components.

The SAA1305T contains 8 inputs with accurate Schmitt triggers and clamp circuits. The main function of this IC is an intelligent I/O expander with 2 modes of operation:

1. Normal I/O expander: the microcontroller (master) is running and the SAA1305T acts like a slave.
2. Sleep mode of the total application: the microcontroller is stopped and the SAA1305T acts like a master. During an event, the microcontroller is awakened.

The communication with the IC is performed via the I^2C-bus (400 kHz). Extra functions of the SAA1305T are:

- LED blinker circuit
- One-day watch
- Watchdog timer.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	operating	4.5	5.0	5.5	V
I_q	quiescent supply current	V_{DD} = 5 V; standby mode	–	130	200	µA
$f_{SCL(max)}$	maximum SCL clock frequency		–	–	400	kHz
T_{vj}	virtual junction temperature		–	–	150	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA1305T	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1

BLOCK DIAGRAM

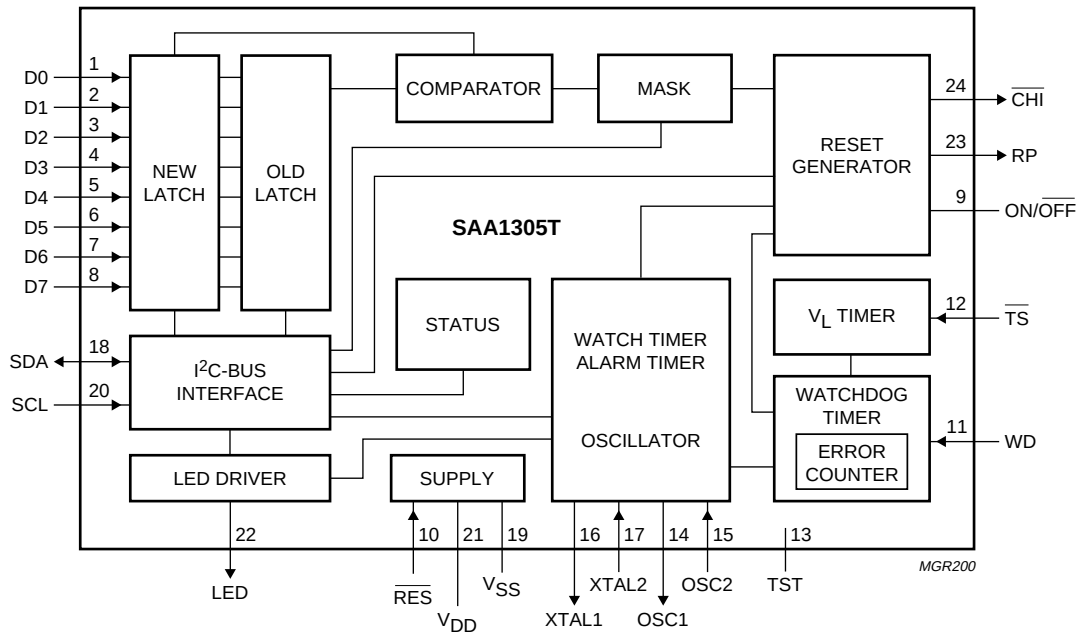


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
D0	1	input D0; generates a reset pulse on pin RP and a LOW-level voltage on pin $\overline{CHI}$
D1	2	input D1; generates a reset pulse on pin RP and a LOW-level voltage on pin $\overline{CHI}$
D2	3	input D2; generates a reset pulse on pin RP and a LOW-level voltage on pin $\overline{CHI}$
D3	4	input D3; generates a reset pulse on pin RP and a LOW-level voltage on pin $\overline{CHI}$
D4	5	input D4; generates a reset pulse on pin RP and a LOW-level voltage on pin $\overline{CHI}$
D5	6	input D5; generates a reset pulse on pin RP and a LOW-level voltage on pin $\overline{CHI}$
D6	7	input D6; generates a reset pulse on pin RP and a LOW-level voltage on pin $\overline{CHI}$
D7	8	input D7; generates a reset pulse on pin RP and a LOW-level voltage on pin $\overline{CHI}$
ON/$\overline{OFF}$	9	on/off output (off is active LOW); for controlling the enable of a separate power supply IC from the microcontroller
$\overline{RES}$	10	reset input (active LOW); for power-on or system reset for the IC
WD	11	Watchdog timer trigger input signal from the microcontroller
$\overline{TS}$	12	timer start input (active LOW); to trigger the V_L (is an undervoltage) timer (250 ms)
TST	13	test purpose input; must be connected to V_{SS}
OSC1	14	RC oscillator output (32.768 kHz)
OSC2	15	RC oscillator input (32.768 kHz)
XTAL1	16	crystal oscillator output (32.768 kHz)
XTAL2	17	crystal oscillator input (32.768 kHz)
SDA	18	I^2C-bus serial data input/output; interface to the microcontroller
V_{SS}	19	ground supply (0 V)
SCL	20	I^2C-bus serial clock line input; interface to the microcontroller
V_{DD}	21	supply voltage; 5 V ±10% with a current consumption of maximum 200 μA (without LED current)
LED	22	light emitting diode output; to drive a LED up to 20 mA (high side switch to V_{DD})
RP	23	reset pulse output
$\overline{CHI}$	24	change information output (active LOW); note 1

Note

1. The following results in a LOW-level voltage on pin $\overline{CHI}$:
   a) A change on any of the (non-masked) inputs D0 to D7.
   b) A device reset.
   c) An alarm or V_L timer event.
   d) An oscillator fault or a failed I^2C-bus read sequence after a change information signal.
   e) A failed Watchdog timer trigger sequence.

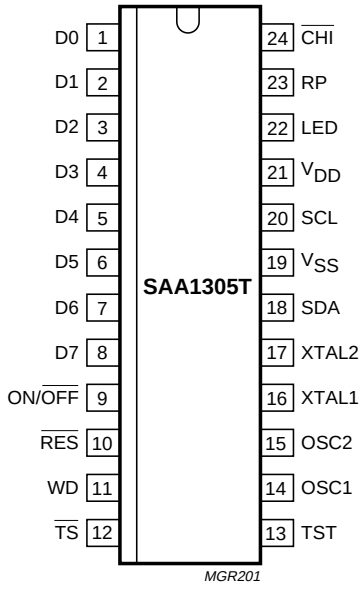


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Figure 1 shows the block diagram for the SAA1305T. Details are explained in the subsequent sections.

Watch and alarm functions

An internal RAM (watch register) counts automatically the seconds for one-day (one-day reset also automatically). The watch register can be set and read from the I²C-bus. An alarm function is possible via a second RAM (alarm register) and is programmable via the I²C-bus. The alarm timer triggers pin $\overline{CHI}$ and if enabled the reset pulse on pin RP. After a device reset the content of the alarm register is FFFFH (alarm function is disabled) and the content of watch register is 0000H.

LED control

The I²C-bus interface control (see Table 10) for the LED contains:

- Two function control bits
- Two control bits for the blink LED frequency
- Two control bits for the blink LED duration time.

All bits are combined within the LED register.

Reset time

The pulse time on pin RP is selectable via an I²C-bus command; see Table 8. The default value after Power-on reset is the longest time (20 ms). Selectable pulse times via the control register are: 1, 5, 10 and 20 ms.

With the rising edge of the reset pulse all inputs, except the Watchdog timer and V_L timer, are disabled until the I²C-bus command ENABLE-RESET. Each pulse on pin RP resets the internal I²C-bus interface.

On/off

The output signal on pin ON/$\overline{OFF}$ remains HIGH after a trigger event. Trigger sources are:

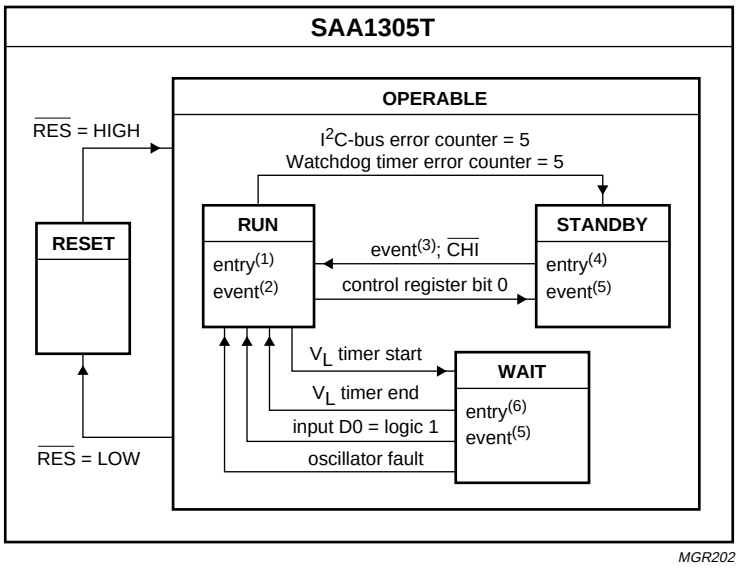
- Alterations on any of the inputs D0 to D7
- An impedance detection
- A device reset
- A V_L (is an undervoltage) timer or alarm timer event
- An oscillator fault.

In the event of a five time failed Watchdog timer trigger or missed I²C-bus read sequence (after a change information indication), an internal logic circuit will reset pin ON/$\overline{OFF}$ and set the IC in the standby mode. It is also possible to control pin ON/$\overline{OFF}$ during the run mode via an I²C-bus command (see Table 8, bit 1). In principal two stable IC modes are possible; see Fig.3:

1. Standby mode: an oscillator fault and the following IC function groups can trigger a reset pulse to enter the run mode;
   a) Watch (alarm timer).
   b) Supply (device reset).
   c) Inputs D0 to D7 (a change on any of these inputs or an impedance detection).

   The Watchdog timer and the V_L timer are disabled in the standby mode.
2. Run mode: only the Watchdog timer (WD), an oscillator fault, a missed I² C-bus communication and the reset input ($\overline{RES}$) can trigger a reset pulse. It is possible to enter the standby mode via control register bit 0; see Table 8.

The dynamic mode or wait mode is possible but can only be started from the run mode (see Section “V_L timer”).



(1) See Section “Run mode entries”.
(2) See Section “Run mode events”.
(3) Possible events are: alterations on any of the inputs D0 to D7, an impedance detection, an alarm timer event and an oscillator fault.
(4) See Section “Standby mode entries”.
(5) Not available.
(6) See Section “Wait mode entries”.

Fig.3 State diagram for IC modes.

RUN MODE ENTRIES

- Reset Watchdog timer error counter
- Enable Watchdog timer
- Enable V_L timer function
- Generate reset pulse
- Disable reset generation via inputs D0 to D7 changes (inclusive impedance detection) and watch compare
- Reset I^2C-bus interface
- Set pin $\overline{CHI}$ to LOW (LOW = active)
- Set pin ON/$\overline{OFF}$ to HIGH (ON is active).

RUN MODE EVENTS

- I^2C-bus read and write commands
- Watchdog timer reset
- Missed I^2C-bus communication after a ($\overline{CHI}$) change information signal
- Oscillator fault.

WAIT MODE ENTRIES

- Disable Watchdog timer
- Reset I^2C-bus error counter
- Reset Watchdog timer error counter
- Start V_L timer
- Set pin $\overline{CHI}$ in 3-state
- Set pin ON/$\overline{OFF}$ to LOW (OFF is active).

STANDBY MODE ENTRIES

- Disable Watchdog timer
- Reset Watchdog timer error counter
- Reset I^2C-bus error counter
- Disable V_L timer function
- Enable reset generation via inputs D0 to D7 changes (inclusive impedance detection) and watch compare
- Set pin ON/$\overline{OFF}$ to LOW (OFF is active)
- Set pin $\overline{CHI}$ in 3-state.

Serial I/O

The hardware of the I^2C-bus interface (slave) operates with a maximum clock frequency of 400 kHz.

Inputs

Pins D0 to D7 are connected to latches (new register). Each latch contains and stores the input change until the read out via the I^2C-bus (read out of new register). A second register (old register, latches) contains the input situation before a 'reset pulse' signal or HIGH-to-LOW transition of pin $\overline{CHI}$. After a level change on any of the inputs D0 to D7 (content of new register into 'old' register), pin $\overline{CHI}$ will indicate this event. Reading the 'old' register has no influence on any latch content. Reading the new register will shift the content into the old register. During the I^2C-bus read sequence of the new register the latch content will be shifted into the corresponding old latch and afterwards the new latches are enabled until the next change on this input. The functions of the inputs D0 to D7 are shown in Table 1.

Due to the fact, that a 'reset pulse' signal or a 'change information' signal are also possible via the Watchdog timer, V_L timer, alarm timer, impedance detection, oscillator fault or after a device reset, the information about these different events is also available via corresponding bits within the status register; see Table 5.

A status I^2C-bus read sequence resets the status register and pin $\overline{CHI}$. Only after a change on any of the inputs D0 to D7, an I^2C-bus read sequence of the status register, old register and new register is it necessary to reset pin $\overline{CHI}$. The inputs D4 to D7 are maskable via the I^2C-bus; see Table 8. All masked inputs (defined via the control register) are blocked to trigger pins $\overline{CHI}$ and RP. During the disable phase of the masked inputs the corresponding bits within the old and new registers will be continuously refreshed with the actual input level.

Table 1 Input logic levels and functions

INPUT	SCHMITT TRIGGER INPUT	SPECIAL INPUT	MASKABLE	V_L TIMER INTERRUPT	IMPEDANCE DETECTION
D7	X	–	X	–	–
D6	X	–	X	–	–
D5	X	–	X	–	–
D4	–	X	X	–	–
D3	–	X	–	–	–
D2	–	X	–	–	–
D1	X	–	–	–	X
D0	X	–	–	X	–

IMPEDANCE DETECTION

Input D1 is a normal input with comparable behaviour like the other seven inputs. The only difference is an additional internal exclusive-NOR (EXNOR) connected between the two comparator outputs for high and low detection; see Fig.4. The EXNOR signal indicates, in combination with a special external circuit on input D1, a voltage of $\frac{1}{2}V_{DD}$ on this input.

The simple input description for impedance detection is probably not the real solution, but helps to explain the function. Input D1 can be used as a normal input and for impedance detection as described in Table 2. For normal use the output Q acts like every other input, but for impedance detection the EXNOR output S is also important. Output S is linked to the status register bit 6 and indicates the $\frac{1}{2}V_{DD}$; see Table 5.

Between detection and indication via the status register bit 6, a delay time is integrated (programmable via the impedance register bits 1 and 0; see Table 15). When the $\frac{1}{2}V_{DD}$ value is detected the EXNOR output will be set to logic 1 (active) and after the programmed delay time the status register bit 6 will be set to logic 1 (active). This event will also be indicated via pin $\overline{CHI}$ and (if enabled) pin RP. The impedance information (bit 6 is active) within the status register is present until the I^2C-bus status is read. With the disappearance of the impedance information no further actions will be generated. Every impedance signal change during the delay time will restart the delay time. However an impedance detection is only possible in the event of a stable signal, at least for the programmed delay time. Setting the status register bit 6 with a repetition time which equals the 'impedance delay time' as long as input D1 stays in high-impedance state is implemented.

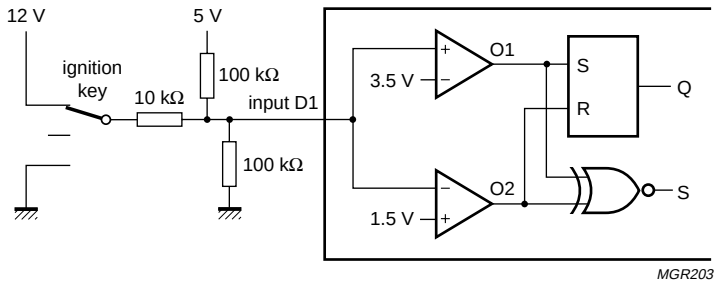


Fig.4 Simple input description for impedance detection.

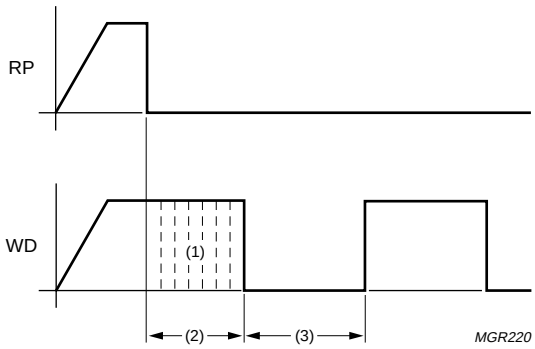
Table 2 Logic levels for impedance detection

IGNITION KEY	O1	O2	Q	S
12 V	1	0	1	0
Open-circuit (V_I = 2.5 V)	0	0	0 or 1	1
Ground (V_I < 1.5 V)	0	1	0	0

Watchdog timer

An internal Watchdog timer is active after each reset pulse output and can be triggered via pin WD. In the event of a not specified pulse, a delayed or missing trigger pulse, a reset on pin RP will be the immediate reaction.

After the HIGH-to-LOW transition of the reset pulse output, the first transition change within 500 ms on pin WD will be detected as the first trigger from the microcontroller. The timing diagram for the Watchdog timer trigger signal is shown in Fig.5.



(1) In the event of a not specified, a delayed or missing trigger signal, a reset on pin RP will be the immediate reaction.
(2) The maximum time until signal change for first Watchdog timer is 500 ms.
(3) The time until next signal change is minimum 200 ms and maximum 300 ms.

Fig.5 Watchdog timer trigger timing.

Oscillators

Two oscillator types are built-in, a RC oscillator (designed for 32.768 kHz) and a crystal oscillator (32.768 kHz), both with separate pins. For a proper device function an oscillator control circuit is integrated. This circuit supervises the oscillator function and creates a reset and oscillator restart in the event of an oscillator failure.

In the event of an oscillator fault, the event will be indicated after a restart via the status register bit 5. During the oscillator failure phase some outputs remain at a defined level as shown in Table 3.

The RC oscillator accuracy is 5%.

When operating with the RC oscillator, pin XTAL2 must be connected to V_{DD} or V_{SS} to minimize the quiescent current. When operating with the crystal oscillator pin OSC2 must be connected to V_{SS} or V_{DD}.

V_L timer

A built-in timer, which can be started with a HIGH-to-LOW transition on pin $\overline{TS}$, triggers, after 250 ms, pins RP and $\overline{CHI}$ and sets pin ON/$\overline{OFF}$. The V_L timer starts only once after a valid start condition. Default state after a Power-on reset is not active. A V_L timer start resets the Watchdog timer. During run time of the V_L timer is ON/$\overline{OFF}$ = LOW, $\overline{CHI}$ = 3-state and the Watchdog timer is disabled.

Pin $\overline{TS}$ is only active during the run mode. During run time of the V_L timer the IC remains in the wait mode. Only a HIGH-level signal on input D0 can stop the V_L timer in the same way as after 250 ms. In the event of an oscillator fault the IC also enters the run mode but without an influence on the status register bit 2. During the wait mode an influence of the status register via other sources (e.g. timer and inputs) is possible, but a transition from wait mode to run mode is only possible as described above.

Power-on or system reset

The reset input (pin $\overline{RES}$) is of the CMOS input levels type. During a LOW level on pin $\overline{RES}$ the outputs are as shown in Table 3 for $\overline{RES}$ = LOW.

After the system reset (rising edge on pin $\overline{RES}$) all internal registers are in a defined condition (see Table 4) and the outputs are as shown in Table 3 for $\overline{RES}$ = HIGH.

Table 3 Logic levels for the reset input and oscillator failure

PIN	$\overline{RES}$ = LOW	$\overline{RES}$ = HIGH	OSCILLATOR FAILURE
RP	HIGH	HIGH (voltage on V_{DD}) 3-state [after a defined time (maximum reset time)]	3-state
ON/$\overline{OFF}$	LOW	HIGH	LOW
LED	LOW	LOW	LOW
SDA	3-state	3-state (receiving mode if RP = LOW)	3-state
$\overline{CHI}$	3-state	LOW (information for microcontroller)	LOW

Table 4 Defined condition after reset for the registers; $\overline{RES}$ = HIGH

REGISTER	CONTENTS
Status register	02 (HEX)
New register	all input latches are enabled
Old register	same levels as corresponding inputs during falling edge on pin $\overline{RES}$
Control register	03 (HEX)
LED register	04 (HEX)
Alarm register	FFFF (HEX); see Table 7
Watch register	0000 (HEX)
Impedance register	03 (HEX)

I²C-BUS INTERFACE COMMANDS

I²C-bus communication is only possible in the run mode.

Read mode operations

Only the sequential read mode is possible. The IC starts after every device select (code 48) to output data 1. However, in this event the master does acknowledge the data output and the IC continues to output the next data in sequence; see Figs 6 and 7.

To terminate the stream of bytes, the master must not acknowledge the last byte output, but must generate a STOP condition. The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. In the event of higher read sequences than available data bytes, the 7th and 8th bit content are 0 and the address counter will generate a wrap around (output at address 0).

The definitions of the bits are given in Tables 5, 6 and 7.

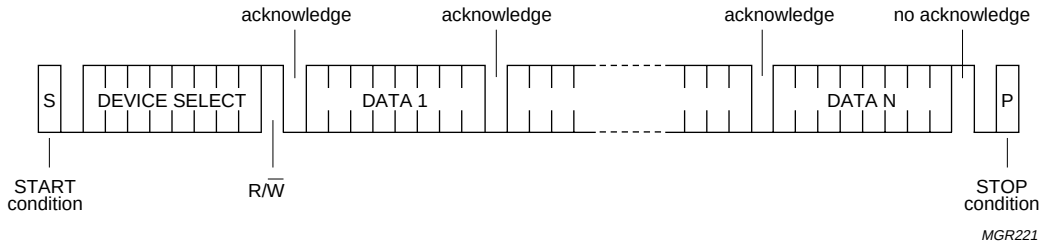


Fig.6 I²C-bus read mode sequence.

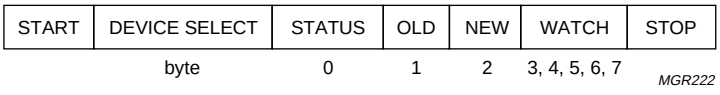


Fig.7 I²C-bus read data sequence.

Table 5 Definition of the status register bits

BIT	DESCRIPTION
7	a logic 1 indicates a change on any of the inputs D7 to D0
6	a logic 1 indicates a $\frac{1}{2}V_{DD}$ on input D1 (impedance detection)
5	a logic 1 indicates a reset after an oscillator fault
4	a logic 1 indicates a reset caused by a missed I^2C-bus communication after a change information signal (no communication between two Watchdog timer trigger pulses)
3	a logic 1 indicates a timer alarm
2	a logic 1 indicates a V_L timer reset
1	a logic 1 indicates a device reset (via pin $\overline{RES}$)
0	a logic 1 indicates a Watchdog timer reset

Table 6 Definition of the old and new register bits

BIT	DESCRIPTION
7	data of input D7
6	data of input D6
5	data of input D5
4	data of input D4
3	data of input D3
2	data of input D2
1	data of input D1
0	data of input D0

Table 7 Definition of the watch and alarm register bits (read mode); note 1

ADDRESS (HEX)	DATA BITS	DESCRIPTION	VALUES	DEFAULT
2	4 to 0	hours of alarm	0 to 31	31
3	5 to 0	minutes of alarm	0 to 63	63
4	5 to 0	seconds of alarm	0 to 63	63
5	4 to 0	hours of watch	0 to 23	0
6	5 to 0	minutes of watch	0 to 59	0
7	5 to 0	seconds of watch	0 to 59	0

Note

1. The alarm is disabled by writing a time larger than 24:00:00. With the default values the alarm function is disabled.

Write mode operations

After a START condition the master sends a device select code with the R/$\overline{W}$ bit reset to logic 0; see Fig.8. The IC acknowledge this and waits for the address byte. After the address the master sends the corresponding data, which is acknowledged by the IC. It is possible to continue with the data transfer, each byte is acknowledged by the IC. The internal byte address counter is incremented after each data transmission.

The transfer is terminated when the master generates a STOP condition. In the event of a wrong address decoding the IC sends a no acknowledge signal and ignores all following data.

Figure 9 shows the sequence for write data mode. Both alarm and watch registers consist of 3 bytes. The first byte (2 and 5) is the most significant byte. The definitions of the bits are given in Tables 8, 10, 14 and 15.

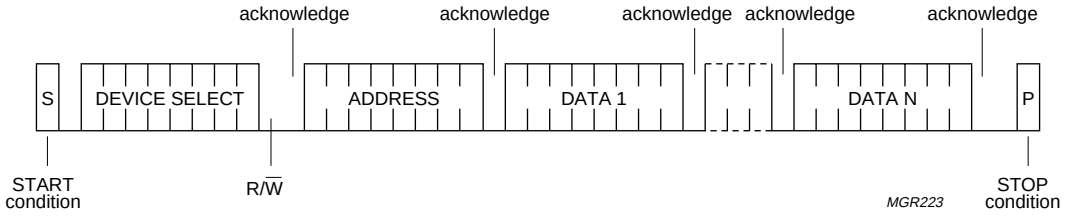


Fig.8 I^{2}C-bus write mode sequence.

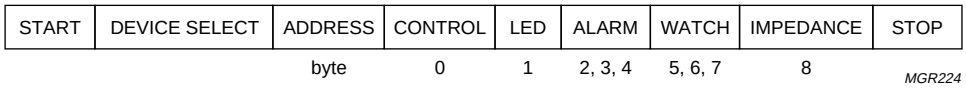


Fig.9 I^{2}C-bus write data sequence.

Table 8 Definition of the control register bits

BIT	DESCRIPTION
7	part of the mask register; corresponds to input D7; a logic 1 disables input D7 (no influence on pin $\overline{CHI}$)
6	part of the mask register; corresponds to input D6; a logic 1 disables input D6 (no influence on pin $\overline{CHI}$)
5	part of the mask register; corresponds to input D5; a logic 1 disables input D5 (no influence on pin $\overline{CHI}$)
4	part of the mask register; corresponds to input D4; a logic 1 disables input D4 (no influence on pin $\overline{CHI}$)
3	content of bits 3 and 2 corresponds with the pulse width of the reset pulse output; see Table 9
2	
1	control bit for pin ON/$\overline{OFF}$; a logic 0 sets pin ON/$\overline{OFF}$ to V_{SS}; a logic 1 sets pin ON/$\overline{OFF}$ to V_{DD}
0	control bit (ENABLE-RESET) for the IC modes; only setting a logic 0 is possible; standby mode with disabled Watchdog timer, enabled reset generation, ON/$\overline{OFF}$ = LOW and $\overline{CHI}$ = 3-state; with the rising edge of the reset pulse output the IC enters the run mode with enabled Watchdog timer, disabled reset generation, ON/$\overline{OFF}$ = HIGH (but controllable via control register bit 1) and $\overline{CHI}$ = HIGH (is active, not in 3-state)

Table 9 Pulse width of the reset pulse output

BIT 3	BIT 2	PULSE WIDTH (ms)
0	0	20
0	1	10
1	0	5
1	1	1

Table 10 Definition of the LED register bits

BIT	DESCRIPTION
7	bits 7 and 6 are function control bits; see Table 11
6	
5	no function
4	reset I^2C-bus error counter
3	bits 3 and 2 are control bits for the blink LED frequency (output LOW time); see Table 12
2	
1	bits 1 and 0 are control bits for the blink LED duration time; see Table 13
0	

Table 11 Function control bits

BIT 7	BIT 6	FUNCTION
0	0	LED output switched to ground
0	1	blink function according the LED register bits 0 to 3
1	0	LED output switched to V_{DD}
1	1	blink function according the LED register bits 0 to 3

Table 12 Control bits for the blink LED frequency

BIT 3	BIT 2	FREQUENCY
0	0	2 Hz (0.5 s)
0	1	1 Hz (1 s)
1	0	0.67 Hz (1.5 s)
1	1	0.5 Hz (2 s)

Table 13 Control bits for the blink LED duration time

BIT 1	BIT 0	DURATION TIME (ms)
0	0	20
0	1	30
1	0	40
1	1	50

Table 14 Definition of the watch and alarm register bits (write mode); notes 1, 2 and 3

ADDRESS (HEX)	DATA BITS	DESCRIPTION	VALUES	DEFAULT
2	4 to 0	hours of alarm	0 to 31	31
3	5 to 0	minutes of alarm	0 to 63	63
4	5 to 0	seconds of alarm	0 to 63	63
5	4 to 0	hours of watch	0 to 23	0
6	5 to 0	minutes of watch	0 to 59	0
7	5 to 0	seconds of watch	0 to 59	0

Notes

1. The alarm is disabled by writing a time larger than 24:00:00. With the default values the alarm function is disabled. The alarm is also disabled if hours >23 or minutes >59 or seconds >59.
2. There are several attention points if a senseless time is written to the alarm register, for example:
   a) Write 25 to address 2; data bits 4 to 0 = 25 ⇒ hours = 25 (alarm disabled).
   b) Write 70 to address 3; data bits 5 to 0 = 6 ⇒ minutes = 6.
   c) Write 81 to address 4; data bits 5 to 0 = 17 ⇒ seconds = 17.
3. There are several attention points if a senseless time is written to the watch register, for example:
   a) Write 25 to address 5; data bits 4 to 0 = 25 ⇒ hours = 23 (limited).
   b) Write 70 to address 6; data bits 5 to 0 = 6 ⇒ minutes = 6.
   c) Write 81 to address 7; data bits 5 to 0 = 17 ⇒ seconds = 17.

Table 15 Definition of the impedance register bits

BIT	DESCRIPTION
7	no function
6	no function
5	no function
4	no function
3	no function
2	enable or disable bit for the impedance detection 0 = inactive ($\frac{1}{2}V_{DD}$ detection without influence on the status register) 1 = active ($\frac{1}{2}V_{DD}$ detection with influence on the status register)
1	bits 1 and 0 are control bits for the impedance detection delay time; see Table 16
0	

Table 16 Control bits for the impedance detection delay time

BIT 1	BIT 0	DELAY TIME
0	0	100 ms
0	1	250 ms
1	0	500 ms
1	1	1 s

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage	operating	–0.5	+6.5	V
I_q	quiescent supply current	V_{DD} = 5 V; standby mode	–	200	µA
$V_{I(n)}$	input voltage on pins	f_{osc} = 32 kHz			
	SDA, SCL, $\overline{RES}$, WD and $\overline{TS}$		–0.5	+6.5	V
	D0 to D7	with 5 kΩ series resistor	–0.5	+17	V
$V_{O(n)}$	output voltage on pins $\overline{CHI}$, RP, ON/$\overline{OFF}$ and LED	f_{osc} = 32 kHz	–0.5	+6.5	V
$f_{SCL(max)}$	maximum SCL clock frequency		–	400	kHz
T_{vj}	virtual junction temperature		–	150	°C
T_{stg}	storage temperature		–65	+150	°C
T_{amb}	ambient temperature		–40	+85	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	78	K/W

CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage	operating	4.5	5.0	5.5	V
I_q	quiescent supply current	note 1	–	130	200	µA
Inputs						
PINS D0 TO D7						
$V_{i(clamp)}$	input clamping voltage	I_{clamp} = 2 mA	5.5	6.5	8.3	V
$I_{clamp(h)}$	high clamping current	V_{D0} to V_{D7} >V_{DD}	–	–	2	mA
I_{LI}	input leakage current	V_{Dx} = 5 V	–	–	1	µA
SCHMITT TRIGGER INPUTS FOR PINS D0, D1 AND D5 TO D7						
$V_{th(r)}$	rising threshold voltage		3.4	3.5	3.6	V
$V_{th(f)}$	falling threshold voltage		1.4	1.5	1.6	V
V_{hys}	hysteresis voltage		1.8	2	2.2	V
SPECIAL INPUTS FOR PINS D2, D3 AND D4						
$V_{th(r)}$	rising threshold voltage		2.4	2.5	2.6	V
$V_{th(f)}$	falling threshold voltage		1.7	1.8	1.9	V
V_{hys}	hysteresis voltage		0.5	0.7	0.9	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PIN SCL						
V_{IL}	LOW-level input voltage		0	–	1.5	V
V_{IH}	HIGH-level input voltage		3	–	V_{DD}	V
I_{LI}	input leakage current	V_i = 5 V; with output off	–	–	1	µA
$f_{SCL(max)}$	maximum SCL clock frequency		–	–	400	kHz
$t_{i(r)}$	input rise time		–	tbf	–	µs
$t_{i(f)}$	input fall time		–	tbf	–	µs
C_i	input capacitance		–	–	7	pF
PINS $\overline{RES}$, WD AND $\overline{TS}$						
V_{IL}	LOW-level input voltage		0	–	$0.2V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.8V_{DD}$	–	V_{DD}	V
I_{LI}	input leakage current	V_i = 5 V; with output off	–	–	1	µA
C_i	input capacitance		–	–	7	pF
Inputs/outputs						
PIN SDA						
V_{IL}	LOW-level input voltage		0	–	1.5	V
V_{IH}	HIGH-level input voltage		3	–	V_{DD}	V
V_{OL}	LOW-level output voltage	I_{OL} = 3 mA	0	–	1	V
I_{off}	3-state off current	V_i = 5 or 0 V	–	–	10	µA
$t_{i(r)}$	input rise time		–	–	2	µs
$t_{i(f)}$	input fall time		–	–	2	µs
$t_{o(f)}$	output fall time	1 V ≤ V_i ≤ 3 V	–	–	200	ns
C_i	input capacitance		–	–	7	pF
C_L	load capacitance		–	–	400	pF
CRYSTAL OSCILLATOR; notes 2 and 3; see Fig.10						
P_{dr}	drive level power		–	10	–	µW
C_L	load capacitance		–	7 to 12	–	pF
R_S	series resistance		–	40	–	kΩ
f_{osc}	oscillator frequency		–	32.768	–	kHz
Q	Q factor		–	40000	100000	
RC OSCILLATOR; note 4; see Fig.11						
C_{osc}	oscillator capacitance		100	300	–	pF
R_{osc}	oscillator resistance		5	90	–	kΩ
f_{osc}	oscillator frequency	C_{osc} = 300 pF; R_{osc} = 90 kΩ; note 5	–	32.768	–	kHz
$f_{clk(min)}$	minimum clock frequency	note 6	–	–	10	kHz

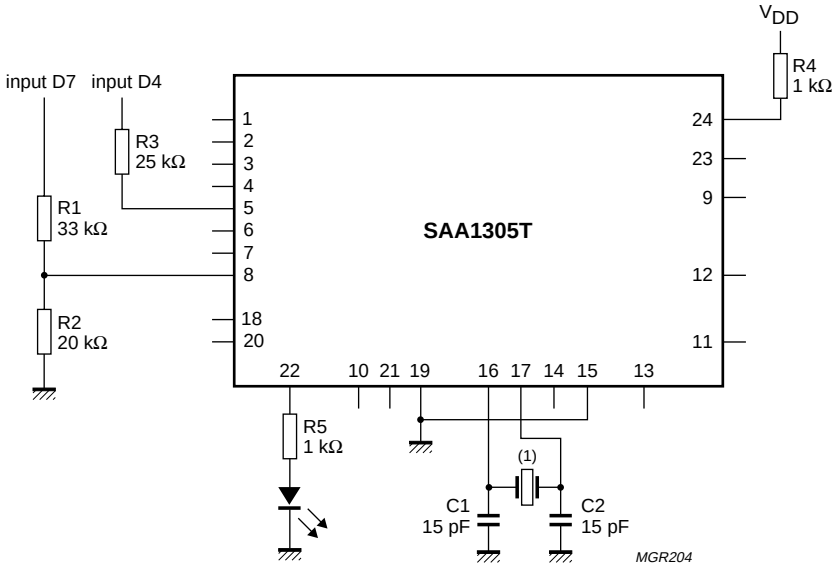
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Outputs						
PIN LED						
V_{OL}	LOW-level output voltage	I_{OL} = 16 mA	0	–	0.5	V
V_{OH}	HIGH-level output voltage	I_{OL} = 16 mA	4	–	V_{DD}	V
I_{OH}	HIGH-level output current	V_{OH} > 1 V	–20	–	–	mA
PIN ON/$\overline{OFF}$						
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA	0	–	0.5	V
V_{OH}	HIGH-level output voltage	I_{OH} = –600 μA	4.8	–	V_{DD}	V
		I_{OH} = –4 mA	4	–	V_{DD}	V
PIN $\overline{CHI}$						
V_{OL}	LOW-level output voltage	I_{OL} = 200 μA	0	–	0.5	V
I_{LO}	output leakage current	$V_{OH} = V_{DD}$	–	–	5	μA
PIN RP						
V_{OH}	HIGH-level output voltage	I_{OH} = –4 mA	4	–	V_{DD}	V
I_{off}	3-state off current	$V_o = V_{DD}$ or V_{SS}	–	–	5	μA

Notes

1. The IC is programmed to standby mode via the I^2C-bus command, no LED is connected, no I^2C-bus communication, one oscillator is running and the Watchdog timer is disabled.
2. When running on crystal oscillator, the input of the RC oscillator must be connected to V_{DD} or V_{SS}.
3. Preferable crystal types: MU206S and DMX38.
4. When running on RC oscillator, the input of the crystal oscillator must be connected to V_{DD} or V_{SS}.
5. The RC oscillator frequency $f_{osc} = \frac{0.87}{R_{osc} \times C_{osc}}$

   The RC oscillator frequency tolerance $\Delta f_{osc} = \sqrt{\Delta R_{osc}^2 + \Delta C_{osc}^2 + (0.05 \times f_{osc})^2}$
6. Below this maximum value the IC will detect an oscillator fault.

APPLICATION CIRCUITS



(1) Crystal oscillator type MU206S (32.768 kHz).

Fig.10 Application circuit for crystal oscillator.

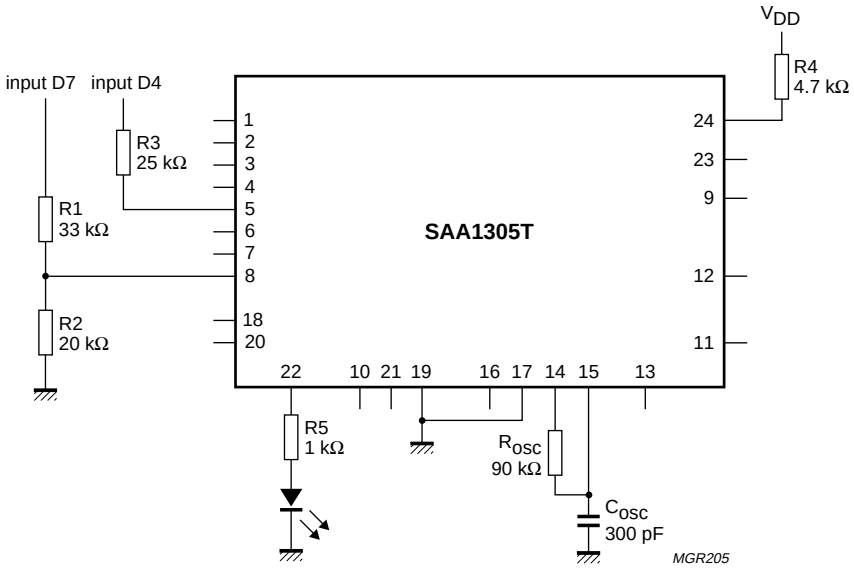


Fig.11 Application circuit for RC oscillator.

ON/$\overline{OFF}$ LOGIC WITH MICROCONTROLLER IN POWER-DOWN STATE

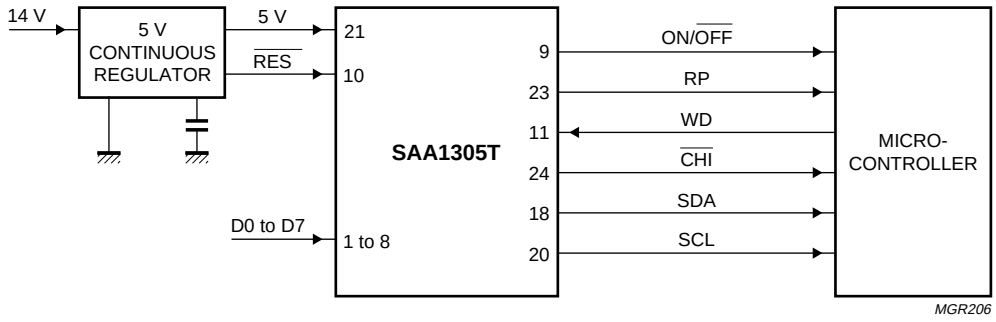
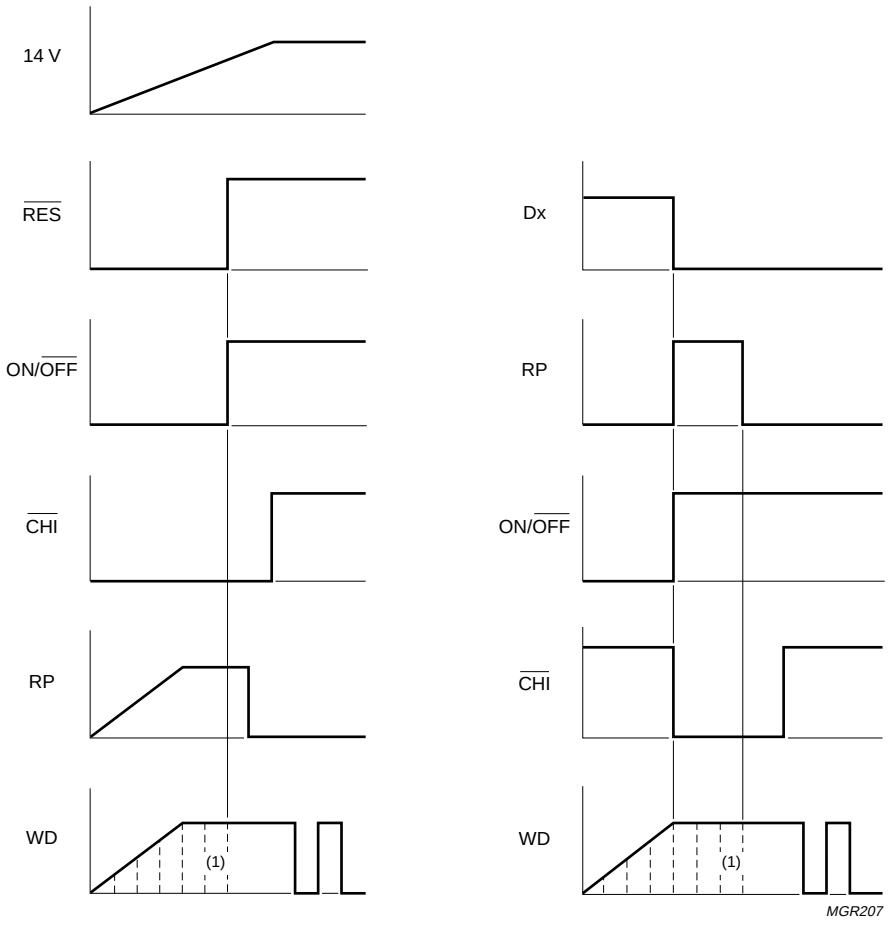


Fig.12 Block diagram with continuous microcontroller supply.



a. First power-on. b. Normal switch-on.

(1) Level not defined.

Fig.13 Timing diagrams with continuous microcontroller supply.

Scenarios for ON/$\overline{OFF}$ logic with microcontroller in power-down state

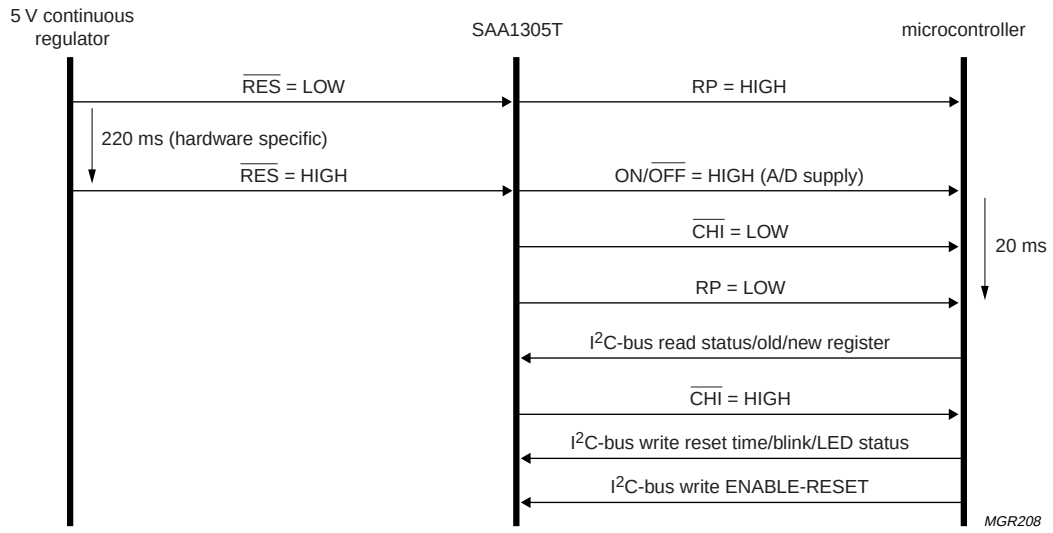


Fig.14 Proper first connection on power supply.

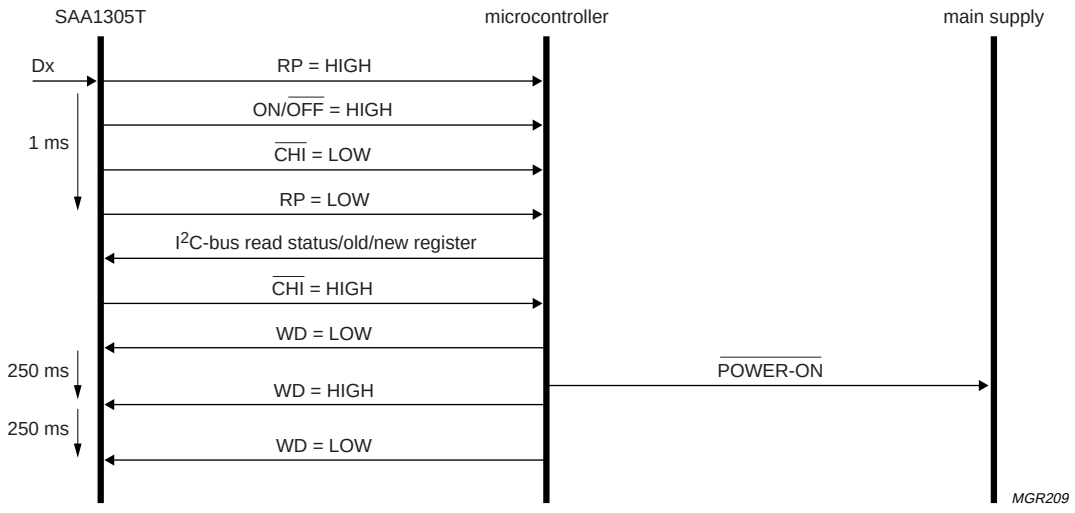


Fig.15 Switch-on after a valid input change.

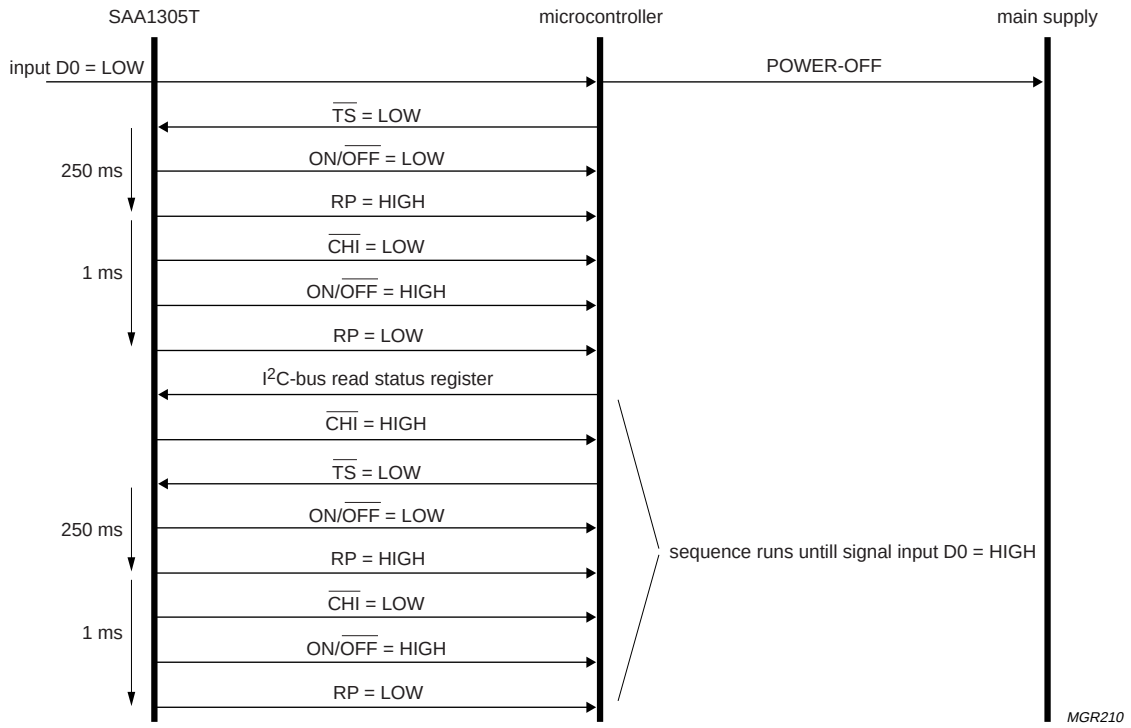


Fig.16 V_L timer behaviour (voltage drops >250 ms).

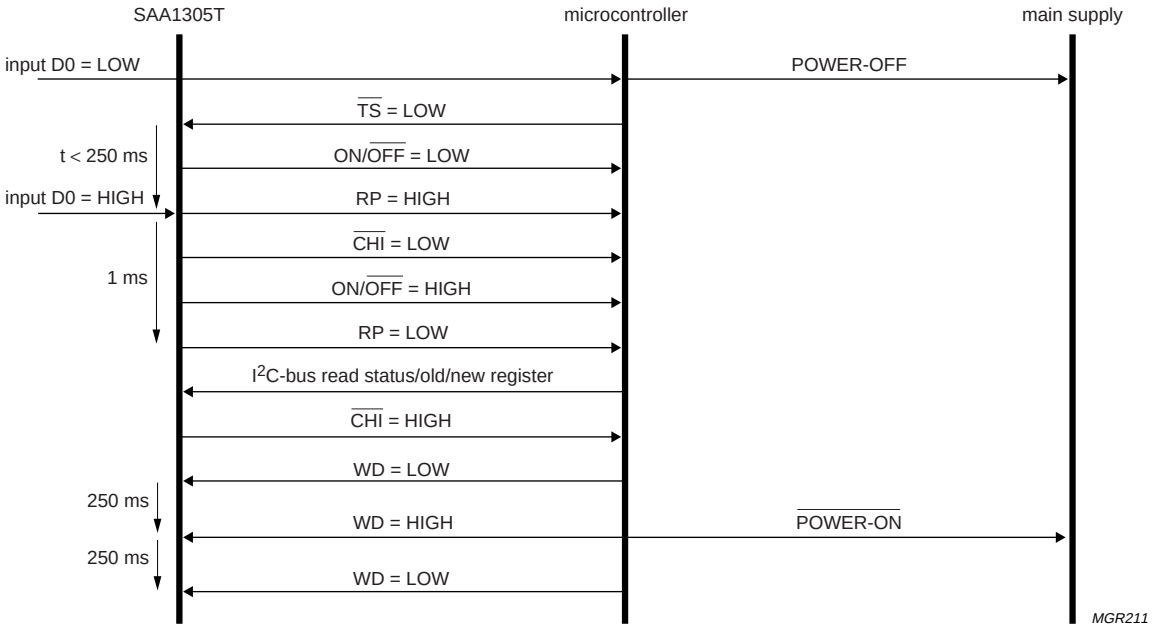
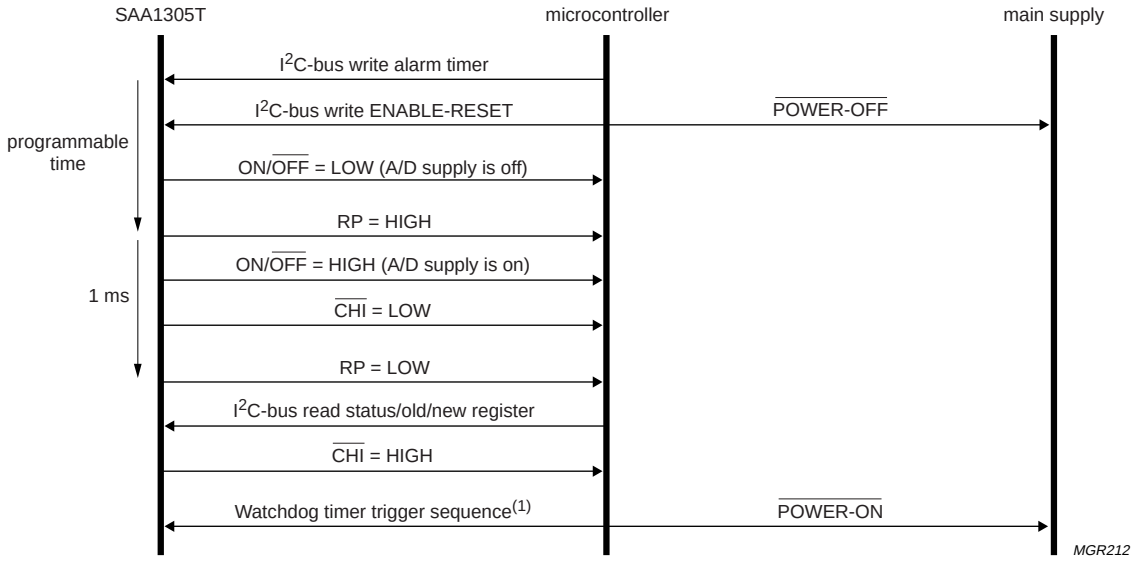


Fig.17 V_L timer behaviour (voltage drops <250 ms).



(1) See Fig.5.

Fig.18 Wake-up via alarm.

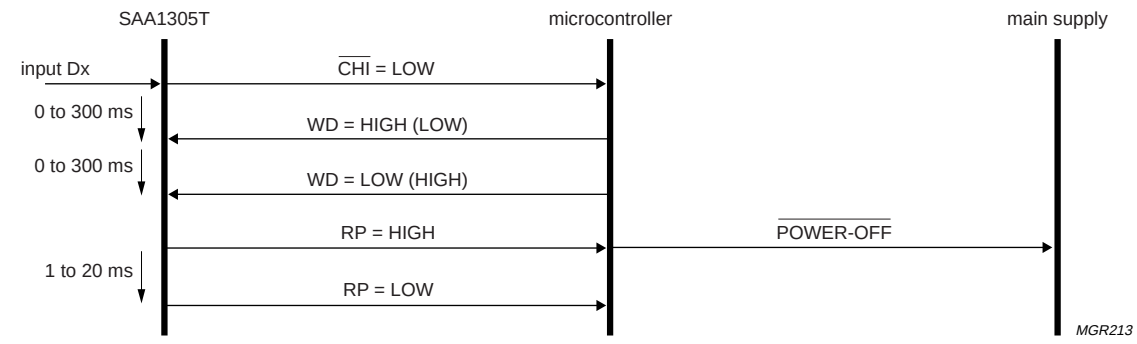


Fig.19 Behaviour after missed I2C-bus read sequence.

ON/$\overline{OFF}$ LOGIC WITH SWITCHED MICROCONTROLLER SUPPLY

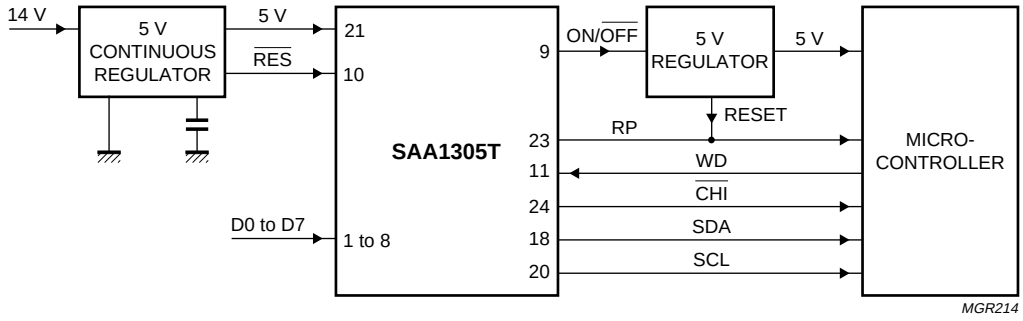
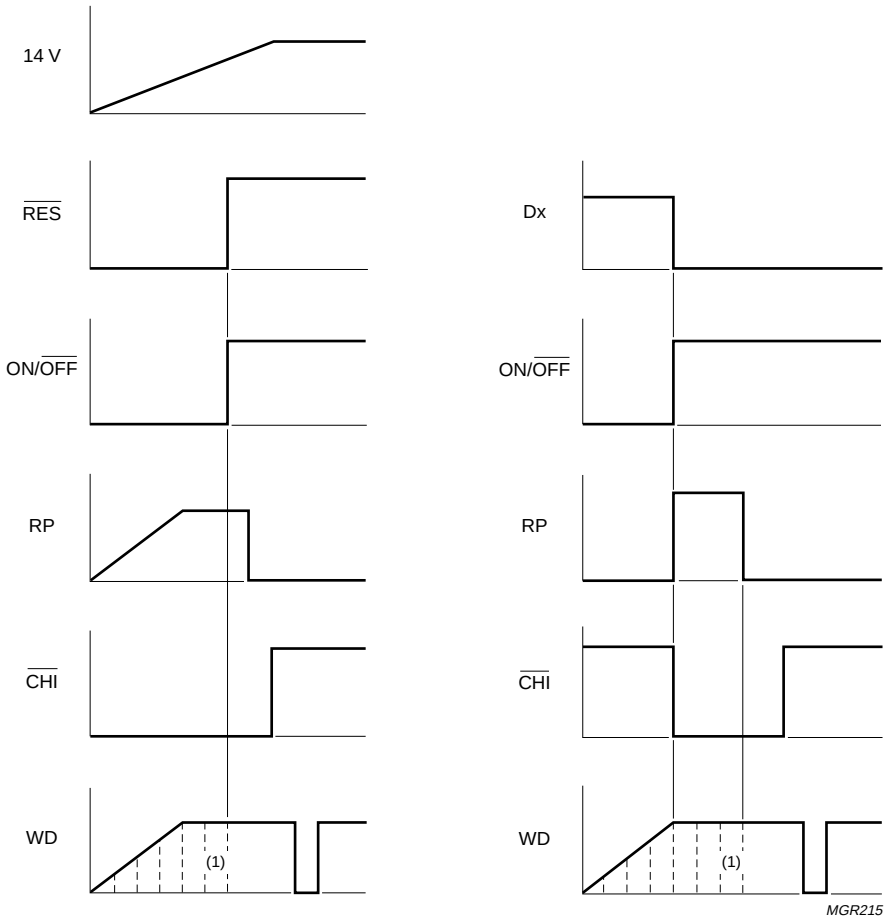


Fig.20 Block diagram with switched microcontroller supply.



a. First power-on. b. Normal switch-on.

(1) Level not defined.

Fig.21 On/off description with switched microcontroller supply.

Scenarios for ON/$\overline{OFF}$ logic with switched microcontroller supply

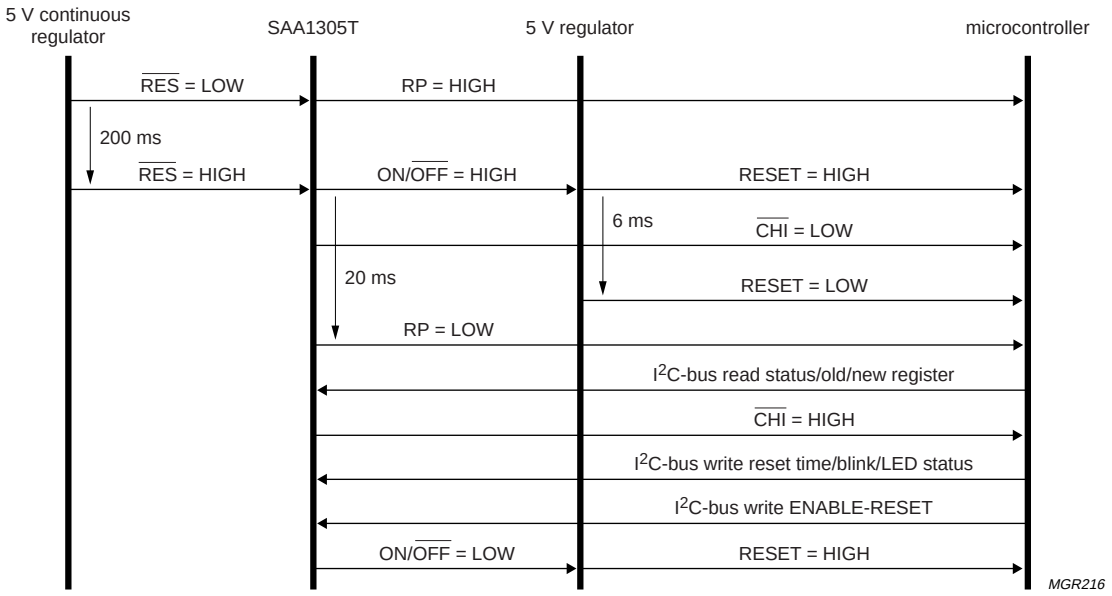


Fig.22 Proper first connection on power supply.

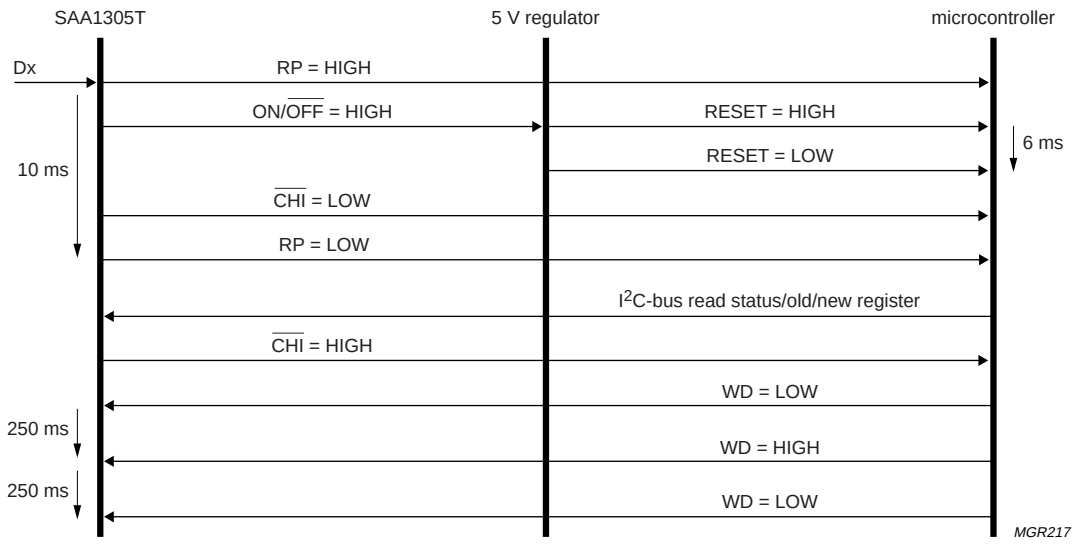
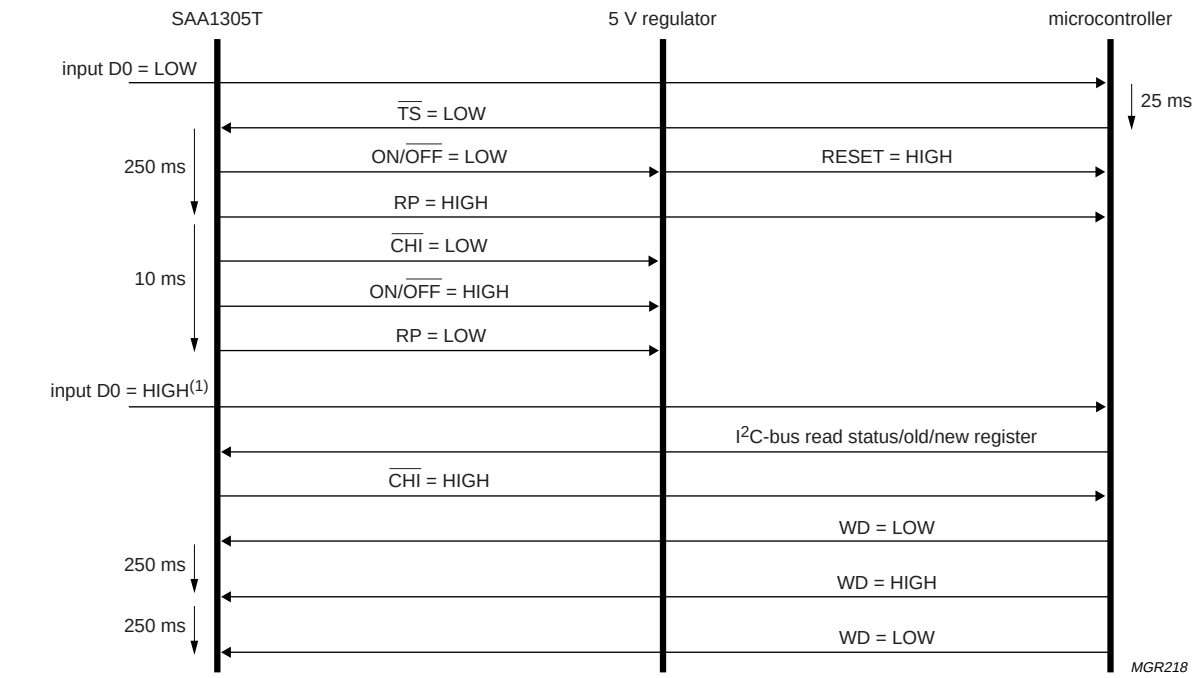


Fig.23 Switch-on after a valid input change.



(1) If input D0 = LOW, the microcontroller will restart the V_L timer.

Fig.24 V_L timer behaviour.

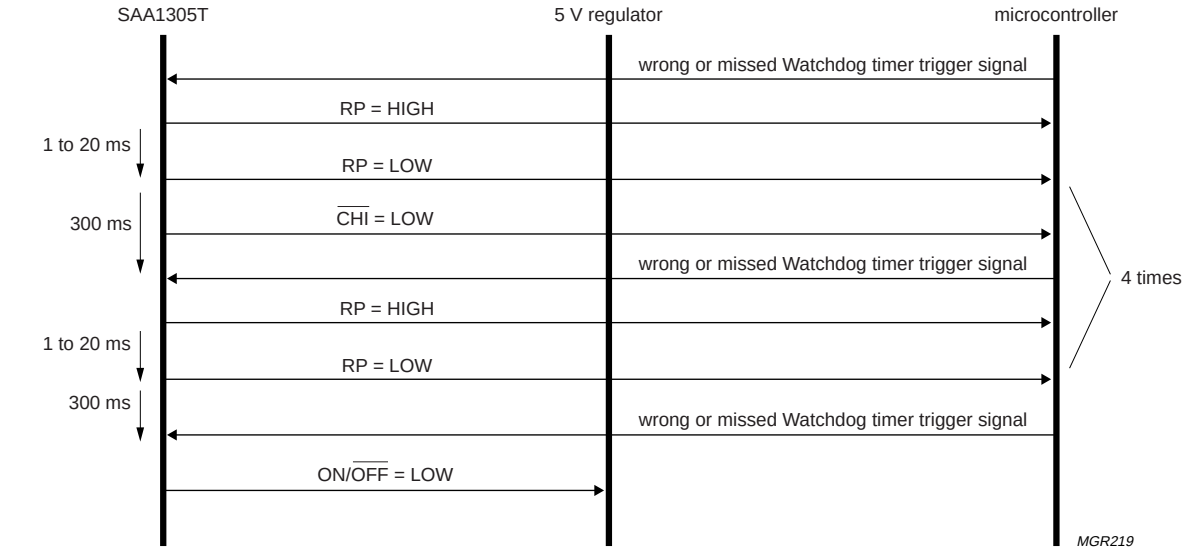
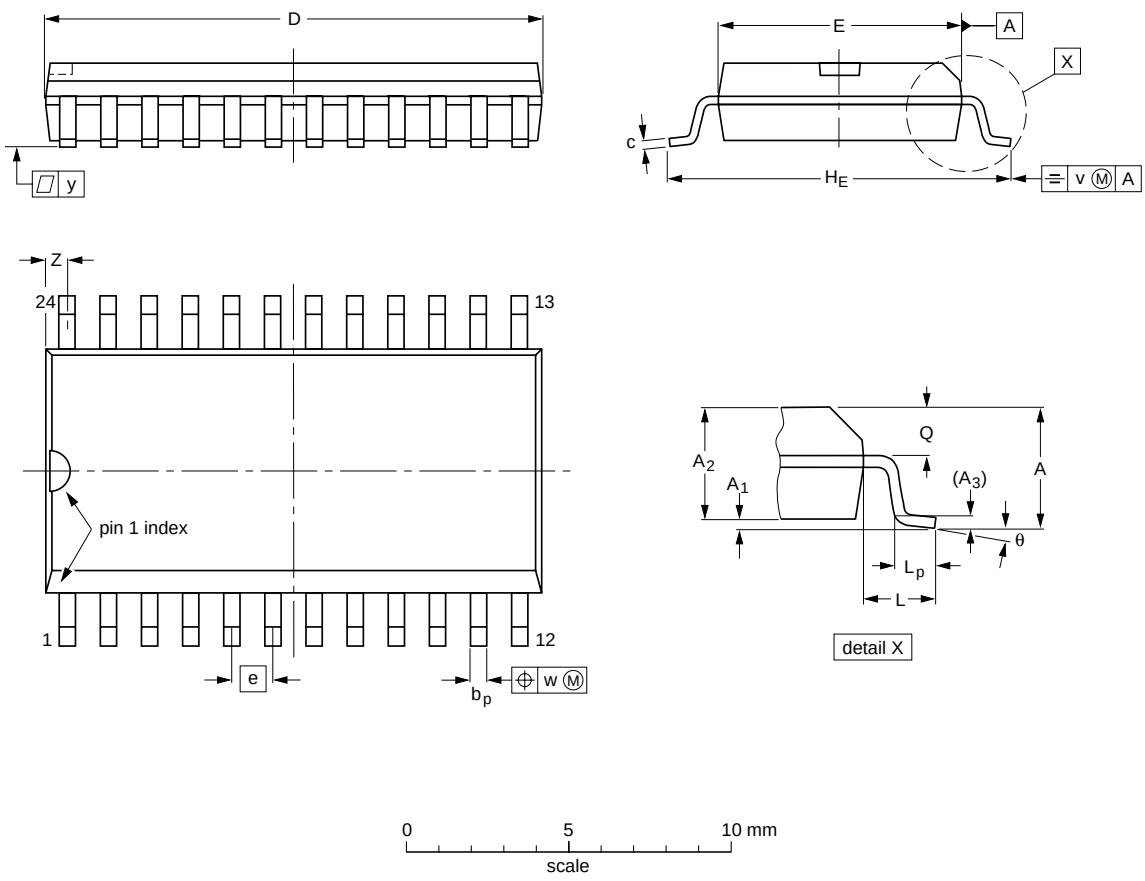


Fig.25 Wrong or missed Watchdog timer trigger.

PACKAGE OUTLINE

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT137-1	075E05	MS-013				~~99-12-27~~ 03-02-19

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON-T and SSOP-T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE[1]	SOLDERING METHOD	
	WAVE	REFLOW[2]
BGA, HTSSON..T[3], LBGA, LFBGA, SQFP, SSOP..T[3], TFBGA, USON, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[4]	suitable
PLCC[5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[5][6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended[7]	suitable
CWQCCN..L[8], PMFP[9], WQCCN..L[8]	not suitable	not suitable

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note*" (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.
4. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
5. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
6. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
7. Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.
8. Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.
9. Hot bar or manual soldering is suitable for PMFP packages.

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

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2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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