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Development Tools J-Trace for Cortex-M3 Overview

J-Trace for Cortex-M3 JTAG emulator with trace support for Cortex-M3 cores

J-Trace for Cortex-M3 is a JTAG emulator designed for Cortex-M3 cores which includes trace (ETM) support. J-Trace for Cortex-M3 can also be used as a J-Link and it also supports ARM7/9 cores. Tracing on ARM7/9 targets is not supported.

Features

- Has all the J-Link functionality
- Supports tracing on Cortex-M3 targets

Documentation download Subscribe to J-Link software notification

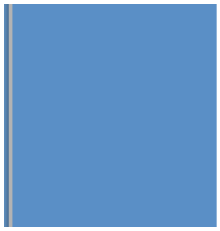
19-pin JTAG/SWD and Trace connector

J-Trace provides a JTAG/SWD+Trace connector. This connector is a 19-pin connector. It connects to the target via an 1-1 cable. The following table lists the J-Link / J-Trace SWD pinout.

Pin	Signal	Type	Description
1	VTref	Input	This is the target reference voltage. It is used to check if the target has power, to create the logic-level reference for the input comparators and to control the output logic levels to the target. It is normally fed from Vdd of the target board and must not have a series resistor.
2	SWDIO/ TMS	I/O / output	JTAG mode set input of target CPU. This pin should be pulled up on the target. Typically connected to TMS of the target CPU.
4	SWCLK/TCK	Output	JTAG clock signal to target CPU. It is recommended that this pin is pulled to a defined state of the target board. Typically connected to TCK of the target CPU.
6	SWO / TDO	Input	JTAG data output from target CPU. Typically connected to TDO of the target CPU.
---	---	---	This pin (normally pin 7) is not existent on the 19-pin JTAG/SWD and Trace connector.
8	TDI	Output	JTAG data input of target CPU.- It is recommended that this pin is pulled to a defined state on the target board. Typically connected to TDI of the target CPU.
9	NC	NC	Not connected inside J-Link. Leave open on target hardware.
10	nRESET	I/O	Target CPU reset signal. Typically connected to the RESET pin of the target CPU, which is typically called "nRST","nRESET" or "RESET".
11	5V- Supply	Output	This pin can be used to supply power to the target hardware. For more information about how to enable/disable the power supply, please refer to Target power supply on page 142.
12	TRACECLK	Input	Input trace clock. Trace clock = 1/2 CPU clock.
13	5V- Supply	Output	This pin can be used to supply power to the target hardware. For more information about how to enable/disable the power supply, please refer to Target power supply on page 142.
14	TRACEDATA [0]	Input	Input Trace data pin 0.
16	TRACEDATA [1]	Input	Input Trace data pin 1.
18	TRACEDATA [2]	Input	Input Trace data pin 2.
20	TRACEDATA [3]	Input	Input Trace data pin 3.

Specifications

General	
Supported OS	Microsoft Windows 2000 Microsoft Windows XP Microsoft Windows XP x64 Microsoft Windows 2003 Microsoft Windows 2003 x64 Microsoft Windows Vista Microsoft Windows Vista x64 Windows 7 Windows 7 x64
Electromagnetic compatibility (EMC)	EN 55022, EN 55024
Operating temperature	+5°C ... +60°C
Storage temperature	-20°C ... +65 °C
Relative humidity (non-condensing)	Max. 90% rH
Size (without cables)	123mm x 68mm x 30mm
Weight	(without cables) 120g
Mechanical	
USB interface	USB 2.0, full speed
Target interface	JTAG 20-pin (14-pin adapter available)
JTAG/SWD Interface, Electrical	
Power supply	USB powered Max. 50mA + Target Supply current.
Target interface voltage (V_{IF})	1.2V ... 5V
Target supply voltage	4.5V ... 5V (if powered with 5V on USB)
Target supply current	Max. 300mA
LOW level input voltage (V_{IL})	Max. 40% of VIF
HIGH level input voltage (V_{IH})	Min. 60% of VIF
JTAG/SWD Interface, Timing	
Data input rise time (T_{rtI})	Max. 20ns
Data input fall time (T_{ftI})	Max. 20ns
Data output rise time (T_{rtO})	Max. 10ns
Data output fall time (T_{ftO})	Max. 10ns
Clock rise time (T_{rC})	Max. 10ns
Clock fall time (T_{fC})	Max. 10ns
Trace Interface, Electrical	
Power supply	USB powered Max. 50mA + Target Supply current.
Target interface voltage (V_{IF})	1.2V ... 5V
Voltage interface low pulse (V_{IL})	Max. 40% of VIF
Voltage interface high pulse (V_{IH})	Min. 60% of VIF
Trace Interface, Timing	
TRACECLK low pulse width (T_{WL})	Min. 2ns
TRACECLK high pulse width (T_{WH})	Min. 2ns
Data rise time (T_{r})	Max. 2ns



Clock fall time (T_{fc})	Max. 3ns
Data setup time (T_s)	Min. 3ns
Data hold time (T_h)	Min. 2ns