CDB4398

Evaluation Board for CS4398

Features

- Demonstrates recommended layout and grounding arrangements
- CS8414 receives S/PDIF, & EIAJ-340 compatible digital audio
- Headers for external audio input for either PCM or DSD
- Requires only a digital signal source and power supplies for a complete Digital-to-Analog-Converter system

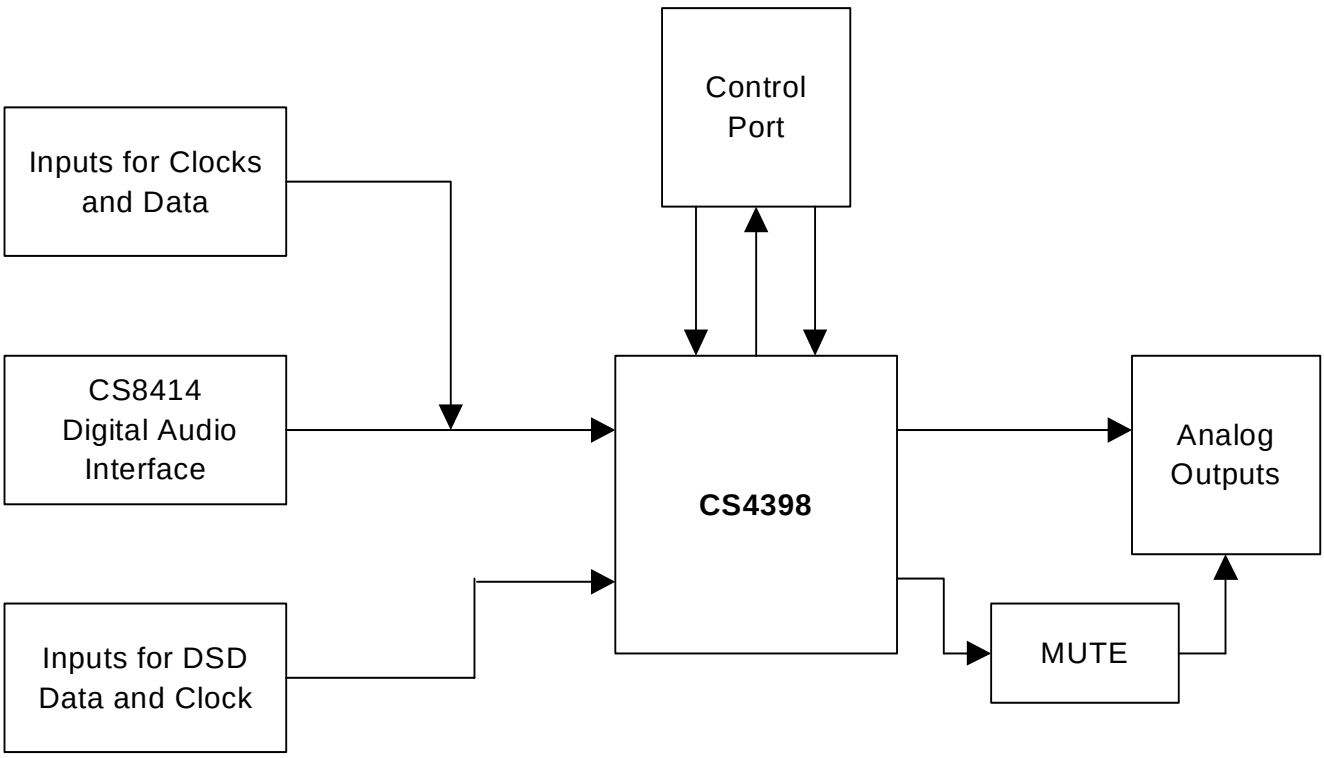
Description

The CDB4398 evaluation board is an excellent means for quickly evaluating the CS4398 24-bit, high performance stereo D/A converter. Evaluation requires an analog signal analyzer, a digital signal source, a PC for controlling the CS4398 (stand alone operation is also available) and a power supply. Analog line level outputs are provided via RCA phono jacks and balanced XLR.

The CS8414 digital audio receiver I.C. provides the system timing necessary to operate the Digital-to-Analog converter and will accept S/PDIF, and EIAJ-340 compatible audio data. The evaluation board may also be configured to accept external timing and data signals for operation in a user application during system development.

ORDERING INFORMATION

CDB4398 Evaluation Board



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Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find one nearest you go to www.cirrus.com

CDB4398 SYSTEM OVERVIEW

The CDB4398 evaluation board is an excellent means of quickly evaluating the CS4398. The CS8414 digital audio interface receiver provides an easy interface to digital audio signal sources including the majority of digital audio test equipment. The evaluation board also allows the user to supply either PCM or DSD clocks and data through headers for system development.

The CDB4398 schematic has been partitioned into 7 schematics shown in Figures 2 through 8. Each partitioned schematic is represented in the system diagram shown in Figure 1. Notice that the system diagram also includes the interconnections between the partitioned schematics.

1. CS4398 DIGITAL TO ANALOG CONVERTER

A description of the CS4398 is included in the CS4398 datasheet.

2. CS8414 DIGITAL AUDIO RECEIVER

The system receives and decodes the standard S/PDIF data format using a CS8414 Digital Audio Receiver, Figure 3. The outputs of the CS8414 include a serial bit clock, serial data, left-right clock (FSYNC), and a 256 Fs master clock. The CS8414 data format is selected by switch S1. The operation of the CS8414 and a discussion of the digital audio interface is included in the CS8414 datasheet.

The evaluation board has been designed such that the input can be either optical or coax, see Figure 3. However, both inputs cannot be driven simultaneously.

3. INPUT/OUTPUT FOR CLOCKS AND DATA

The evaluation board has been designed to allow interfacing to external systems via the headers, J12 and J14. Header J12 allows the evaluation board to accept externally generated PCM clocks and data. The schematic for the clock/data input is shown in Figure 4.

Header J14 allows the evaluation board to accept externally generated DSD data and clock. The schematic for the clock/data input is shown in Figure 4. A synchronous MCLK must still be provided via header J13. Please see the CS4398 datasheet for more information.

4. POWER SUPPLY CIRCUITRY

Power is supplied to the evaluation board by seven binding posts (GND, +5V, VLS, VLC, VD, +12V and -12V), see Figure 8. The VLC and VLS supplies can be jumpered to the +5V binding post for ease of use. VD and VA should be set to the recommended values stated in the CS4398 datasheet. +12V and -12V supply power to the op-amps and can be +/-12 to +/-18 volts.

WARNING: Refer to the CS4398 datasheet for maximum allowable voltages levels. Operation outside of this range can cause permanent damage to the device.

5. GROUNDING AND POWER SUPPLY DECOUPLING

The CS4398 requires careful attention to power supply and grounding arrangements to optimize performance. Figure 2 details the connections to the CS4398 and Figures 9, 10, and 11 show the component placement and top and bottom layout. The decoupling capacitors are located as close to the CS4398 as possible. Extensive use of ground plane fill in the evaluation board yields large reductions in radiated noise.

6. CONTROL PORT SOFTWARE

The CDB4398 is shipped with Windows 95/98/ME based software as well as Windows NT/2000/XP drivers for interfacing with the CS4398 control port via the DB25 connector, J21. The software can be used to communicate with the CS4398 in either SPI® or I^2C mode. See the readme.txt for more information.

7. DSD OPERATION

The CDB4398 supports Direct Stream Digital (DSD) operation through the header for external clocks and data, J14. The CS4398 must be configured for the DSD mode and header J11 should be set to "external". See Table 2 for more information.

8. ANALOG OUTPUT FILTERING

The analog output on the CDB4398 has been designed to add flexibility when evaluating the CS4398. Two output filter options are offered a 2-pole butterworth 50kHz low-pass filter with single ended outputs and a 3-pole filter with XLR outputs.

The 2-pole filter (RCA) is designed to have the in-band impedance matched between the positive and negative legs. It also provides a balanced to single ended conversion for standard un-balanced outputs.

The 3-pole filter (XLR) is designed to have extremely low self noise and distortion in order to evaluate the full performance of the CS4398.

CONNECTOR	INPUT/OUTPUT	SIGNAL PRESENT
+5V	Input	+ 5 Volt power
VD	Input	+ 3.3 to +5V power for the CS4398 digital supply
VLS	Input	+ 1.8 to +5V power for the CS4398 serial interface
VLC	Input	+ 1.8 to +5V power for the CS4398 control interface
J9	Input	-18 to -12V negative supply for the op-amps
J10	Input	+12 to +18V positive supply for the op-amps
GND	Input	Ground connection from power supply
SPDIF INPUT - J17	Input	Digital audio interface input via coax
SPDIF INPUT - OPTO-1	Input	Digital audio interface input via optical
PCM INPUT - J12	Input	Input for master, serial, left/right clocks and serial data
DSD INPUT - J14	Input	Input for DSD data and clock
PC Port	Input/Output	Parallel connection to PC for SPI / I^2C control port signals
EXT CTRL I/O	Input/Output	I/O for SPI / I^2C control port signals
OUTA and OUTB	Output	RCA and XLR line level analog outputs

Table 1. System Connections

JUMPER / SWITCH	PURPOSE	POSITION	S/C	FUNCTION SELECTED
J3	Selects source of voltage for the VLC supplies	VLC *+5V		Voltage source is VLC binding post Voltage source is +5V binding post
J4	Selects source of voltage for the VLS supplies	VLS *+5V		Voltage source is VLS binding post Voltage source is +5V binding post
J7	Selects source of voltage for the VD supply	*VD +5V		Voltage source is VD binding post Voltage source is +5V binding post
J11	Clock Source Select	*CS8414 External		CS8414 provides PCM inputs to CS4398 PCM or DSD inputs are provided externally
S1	Sets Mode of CS8414	*M1 = open *M0, M2, M3 = closed		Default setting is I^2S mode See CS8414 datasheet for details
J19	Stand-Alone/Control Port Select	SA *CP	S C	Stand-Alone Mode (No PC required) Control Port Mode (PC required)
J20	M0/AD0/CS	HI *LO	- SC	See CS4398 datasheet for details
J22	M1/SDA/CDOUT	*HI LO	SC -	See CS4398 datasheet for details
J24	M2/SCL/CCLK	*HI LO	C S	See CS4398 datasheet for details
J28	M3/AD1/CDIN	HI *LO	- SC	See CS4398 datasheet for details
CH_A CH_B	Filter select	*RCA XLR		Selects standard 2-pole filter Selects low noise balanced outputs
R19 and R82	Mute Enables	*SHUNTED OPEN		Enables the external mute circuit for each channel when 0 Ohm is present (default)

Table 2. CDB4398 Jumper Settings

*Default Factory Settings.

The S/C column denotes standard jumper settings for either stand-alone (S) or control port (C) operation.

9. ERRATA

CDB4398 Revision B.0

None at this time.

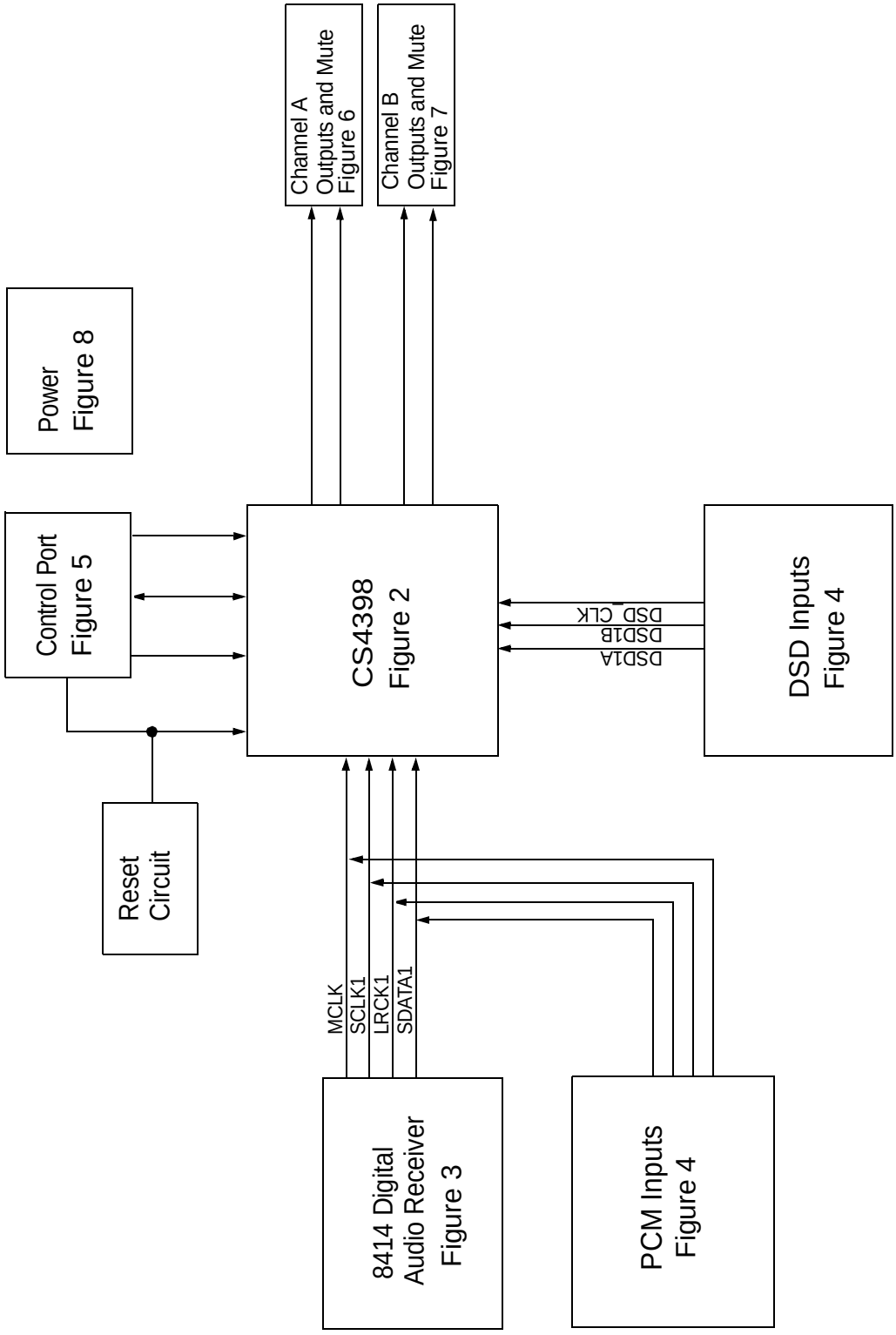

Figure 1. System Block Diagram and Signal Flow

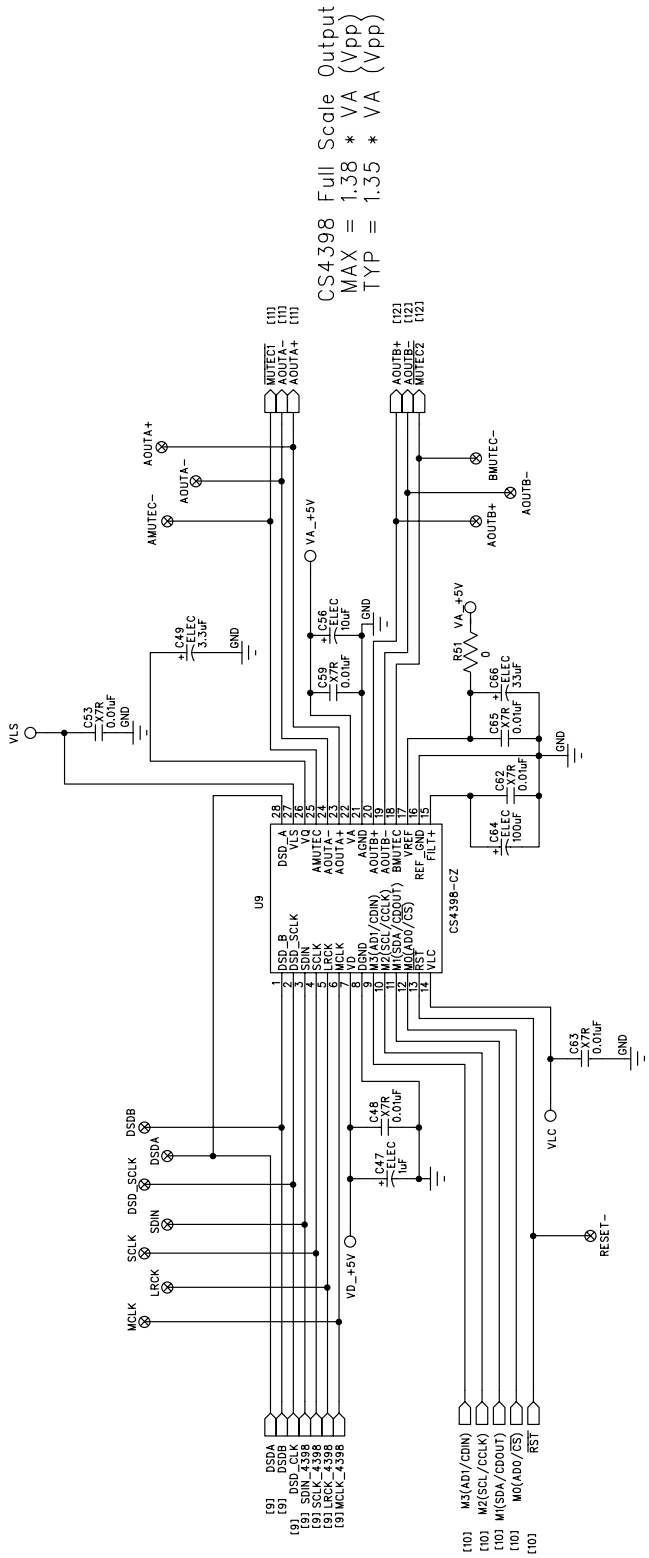

Figure 2. CS4398

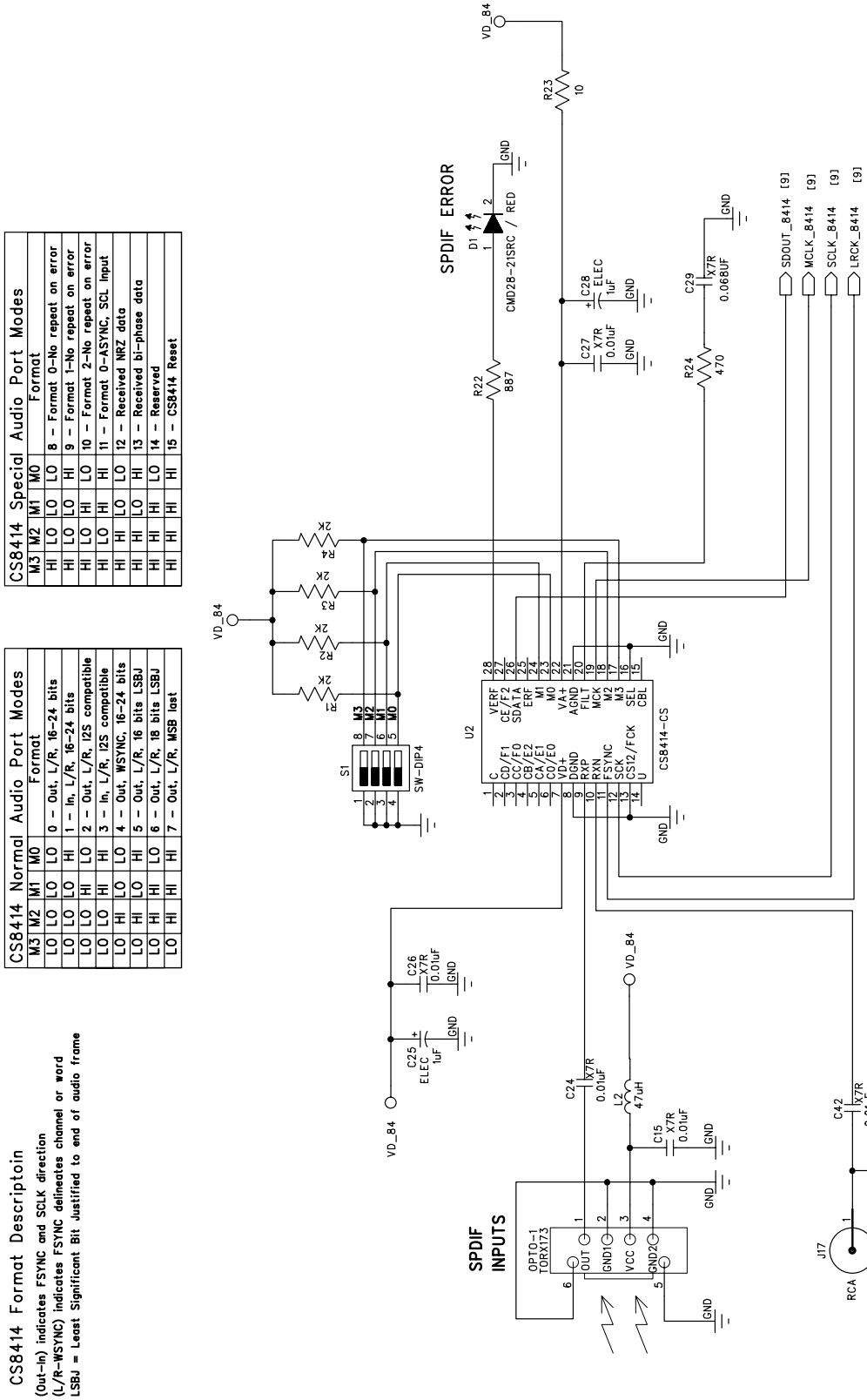

Figure 3. CS8414 Digital Audio Receiver

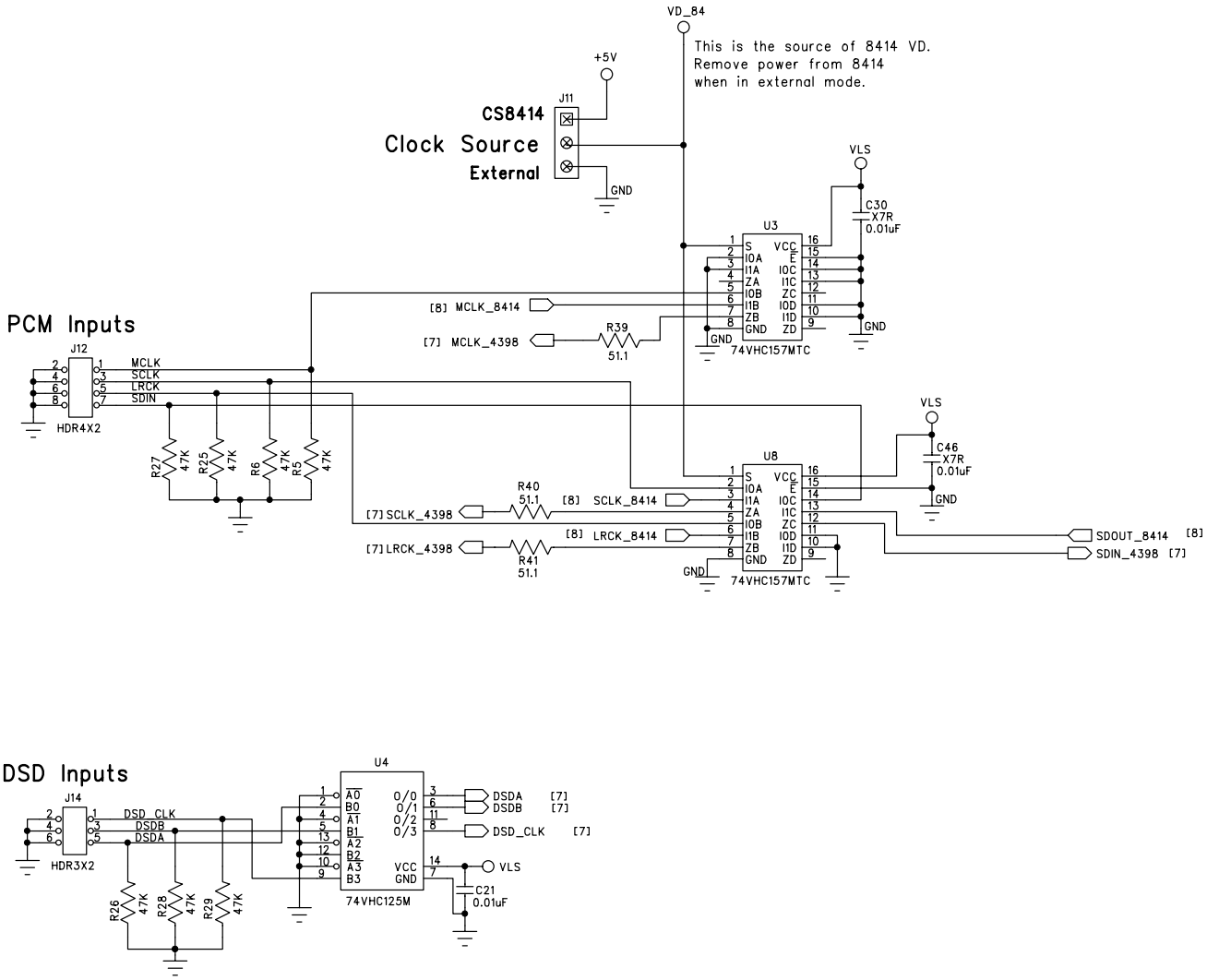

Figure 4. PCM and DSD Input Headers

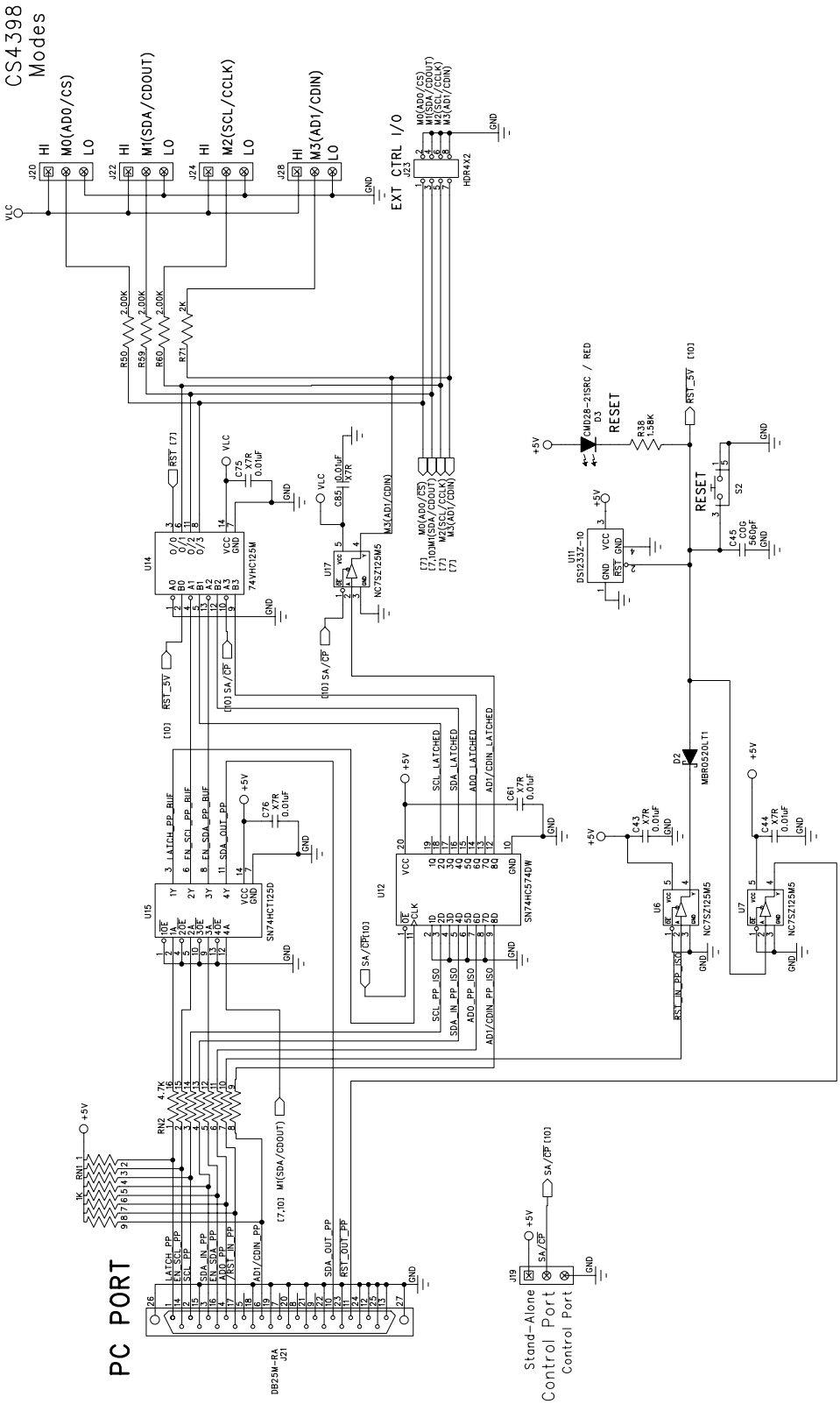

Figure 5. Control Port Interface

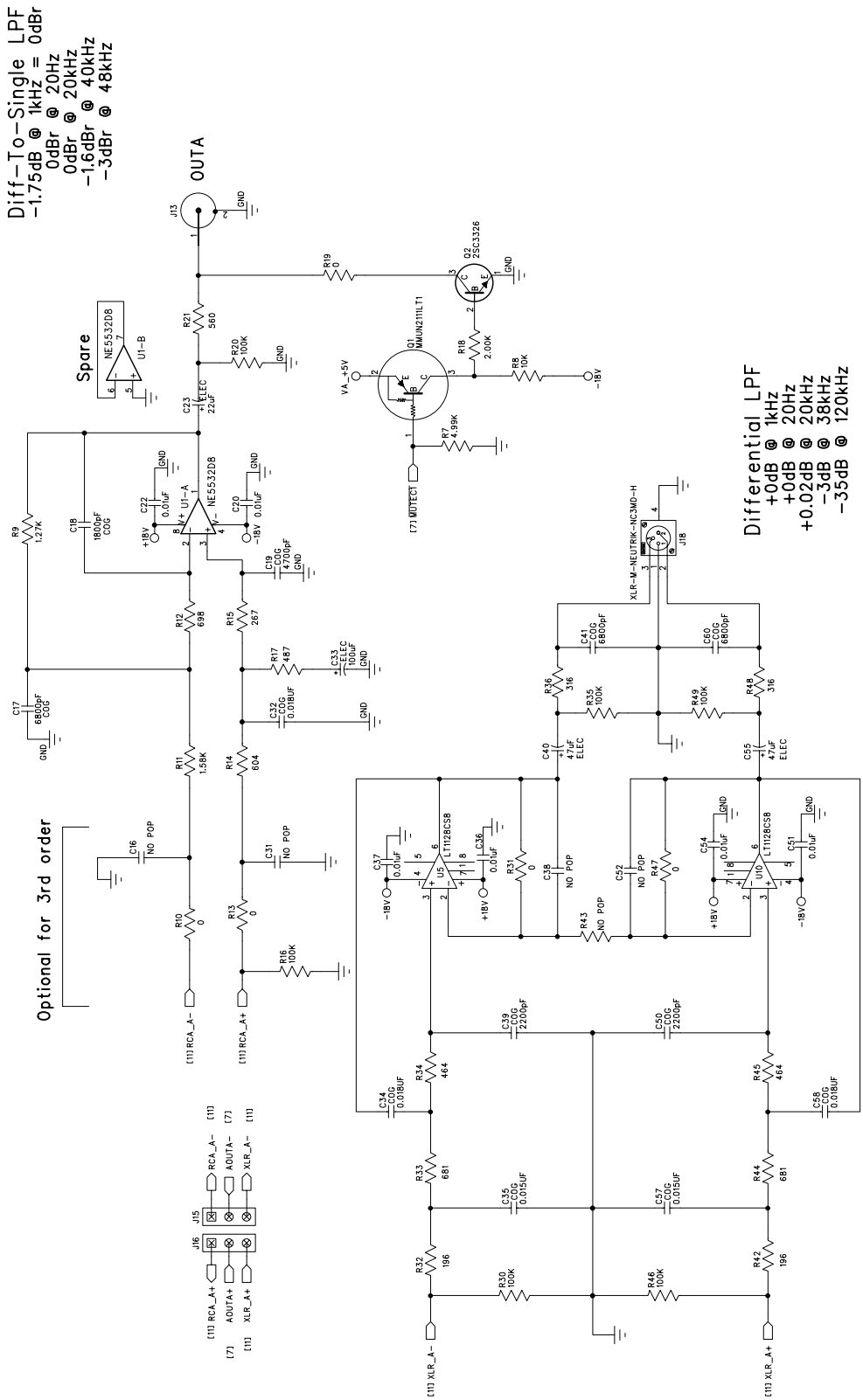

Figure 6. Channel A Outputs and Mute

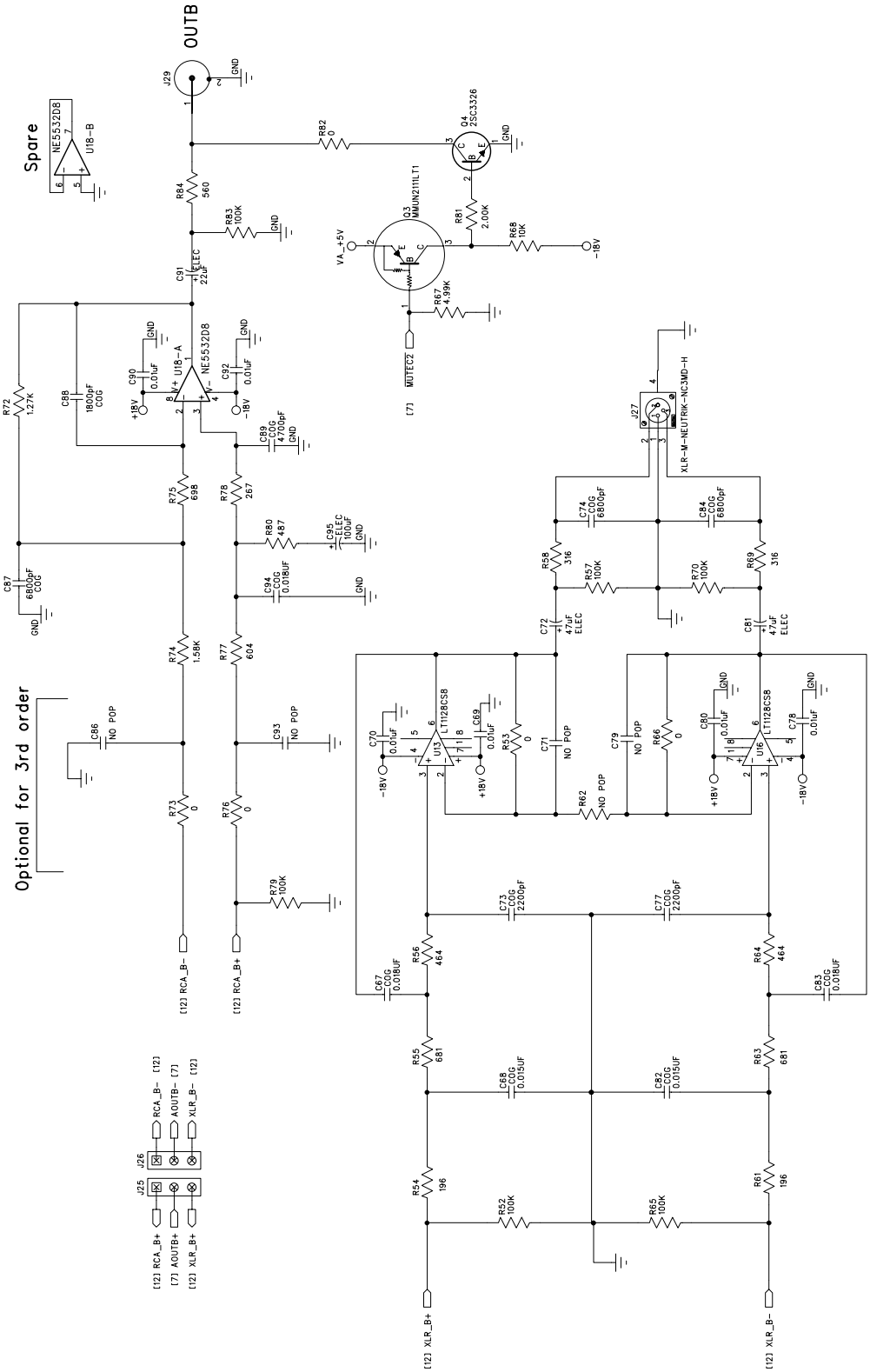

Figure 7. Channel B Outputs and Mute

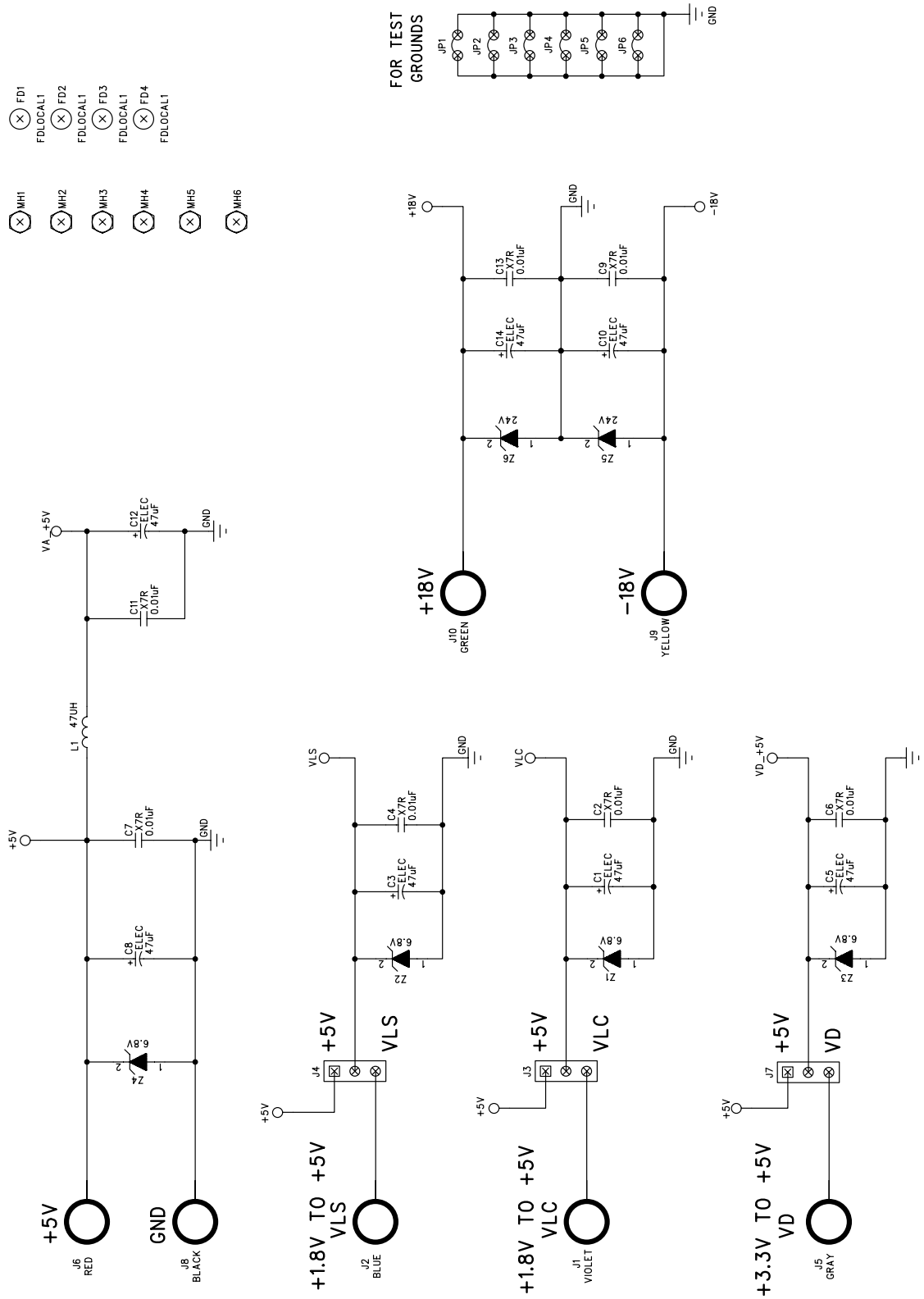

Figure 8. Power Supply Connections

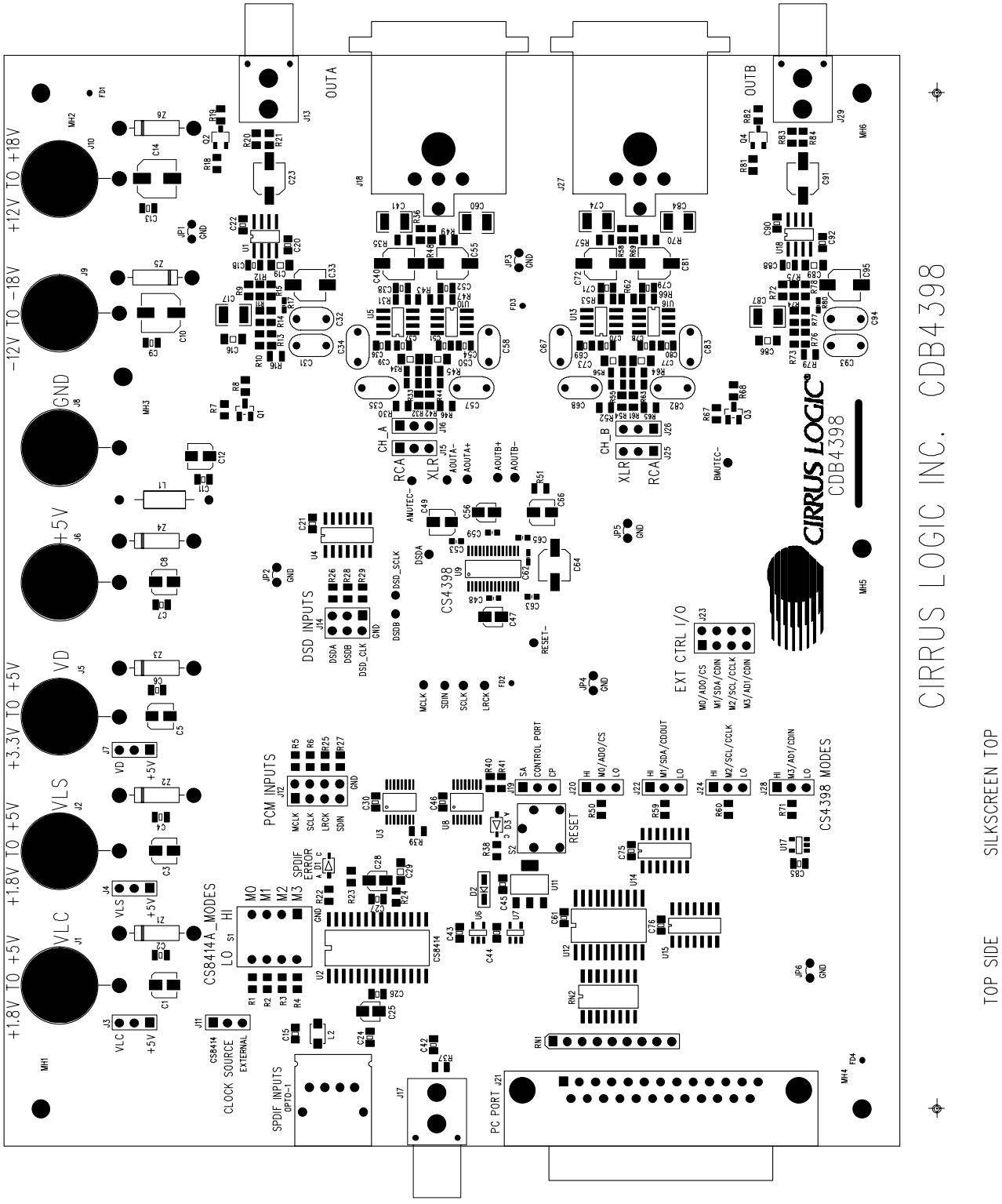

Figure 9. Silkscreen Top

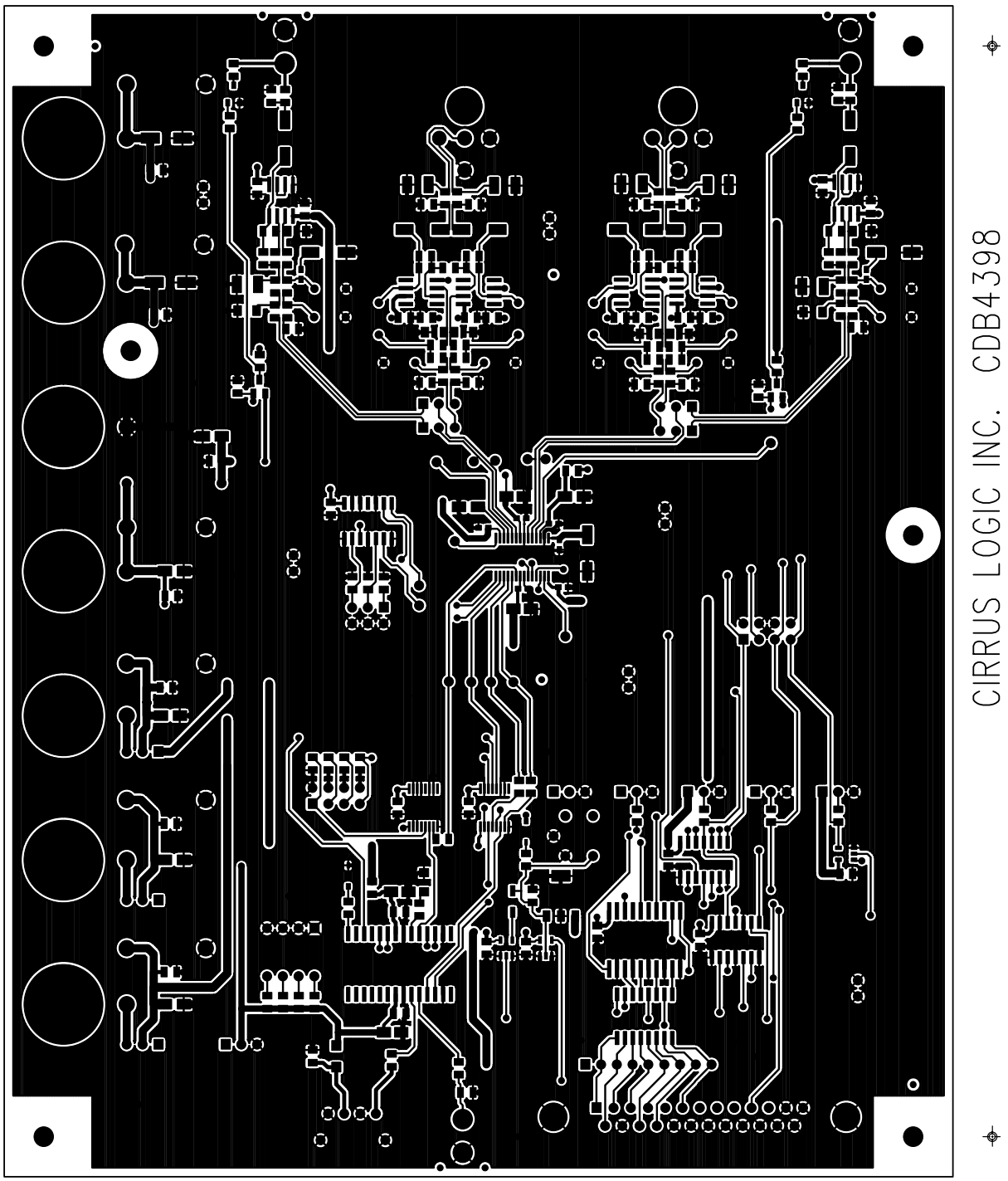

Figure 10. Top Side

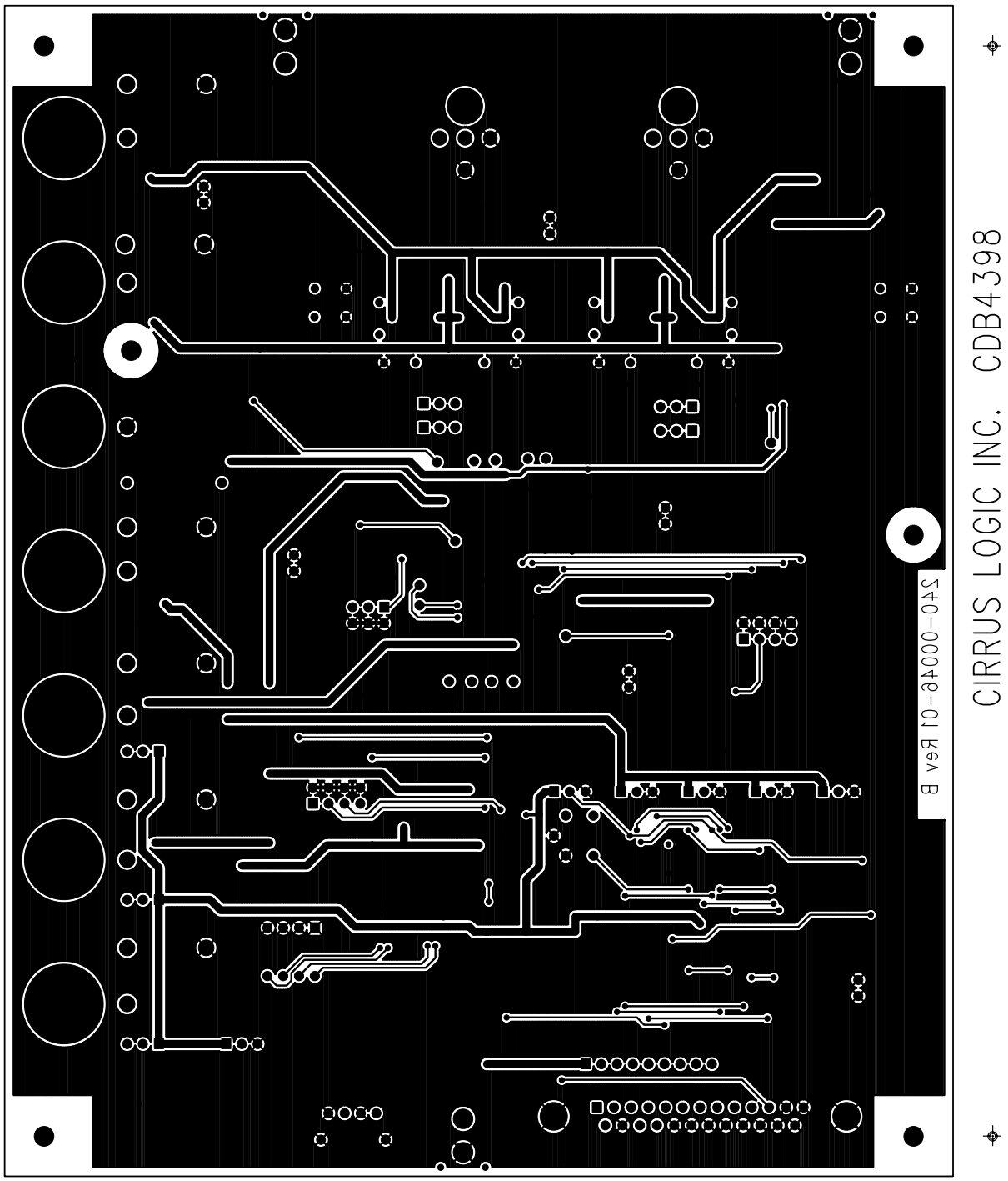

Figure 11. Bottom Side

Notes: